TOSHIBA Bi- CMOS Integrated Circuit Silicon Monolithic

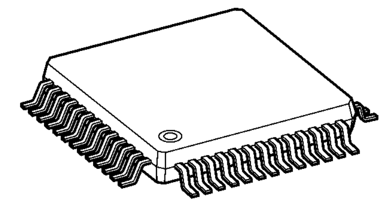
TB6572AFG

3-Phase Full-Wave Brushless Motor Controller Featuring Speed Control and Sine Wave PWM Drive

The TB6572AFG is a 3-phase full-wave brushless motor controller IC that employs a sine wave PWM drive mechanism with a speed control function.

Sine wave current driving with 2-phase modulation enables the IC to drive a motor with high efficiency and low noise.

It also incorporates a speed control circuit that can vary the motor speed using to an external clock.


QFP52-P-1010-0.65

Weight: 0.50 g (typ.)

Features

- Sine wave PWM drive
- 2-phase modulation with low switching loss
- Triangular wave generator
- Dead time function
- External clock input
- Speed discrimination +PLL speed control circuit
- Ready circuit output
- FG amplifier
- Automatic lead angle correction
- Forward/stop/reverse/brake functions
- Current limiter
- Lock protection

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

Pin with low withstand voltage: pin 33

Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause the device breakdown, damage and/or deterioration.

The TB6572AFG is a RoHS-compatible.

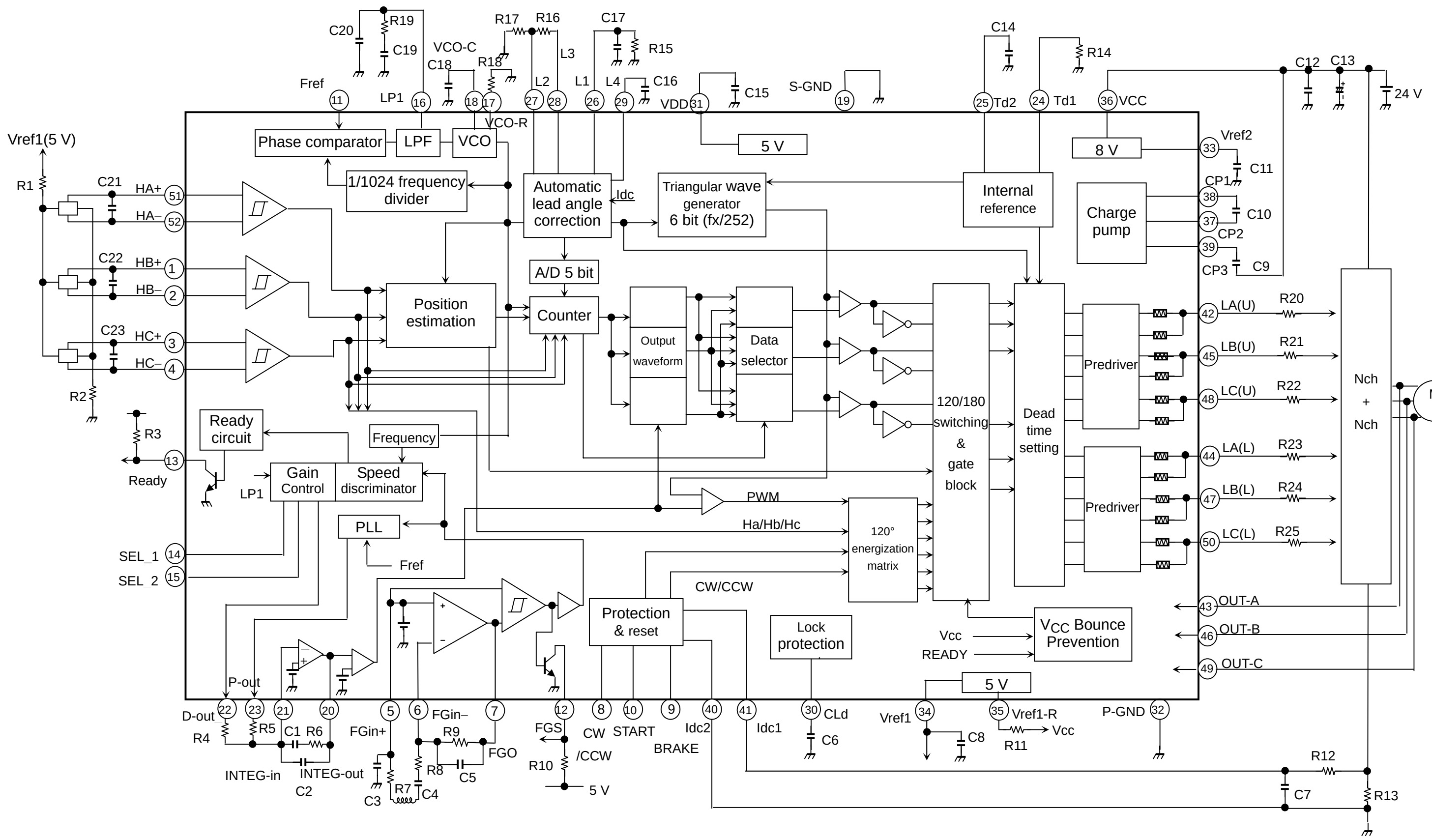
About solderability, following conditions were confirmed:

- Solderability

(1) Use of Sn-37Pb solder Bath
- · solder bath temperature = 230°C
- · dipping time = 5 seconds
- · the number of times = once
- · use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- · solder bath temperature = 245°C
- · dipping time = 5 seconds
- · the number of times = once
- · use of R-type flux

Block Diagram

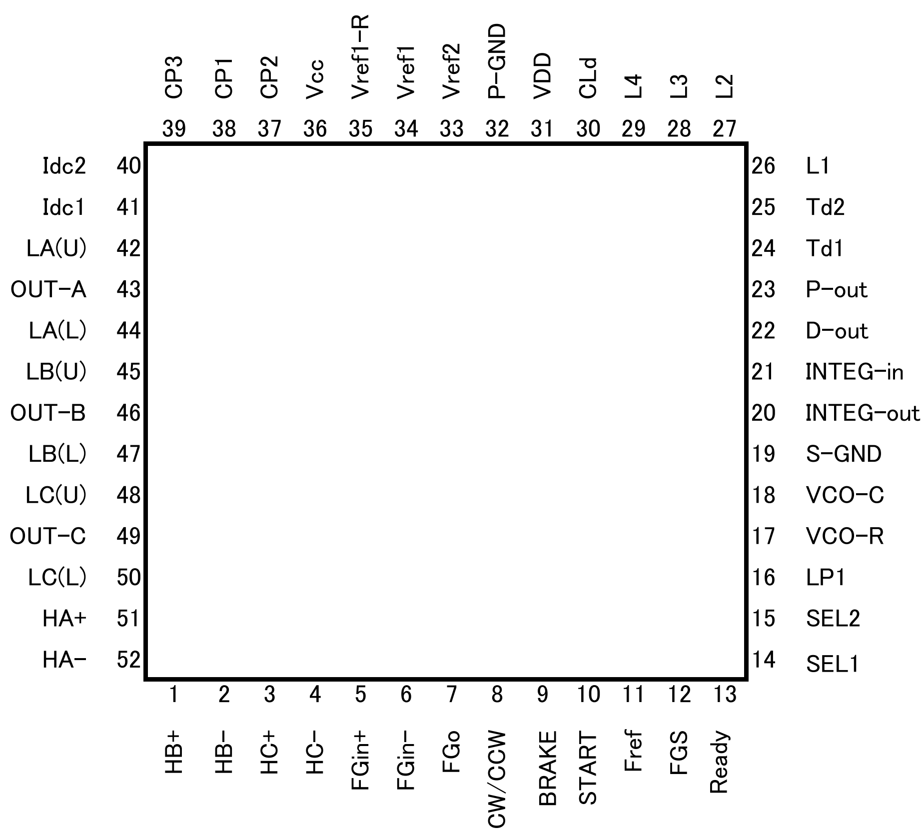


Pin Functions

Pin No.	Name	Pin Functions	Remarks
1	HB+	Phase-B hall signal input + pin	Input the positive phase-B Hall device signal.
2	HB–	Phase-B hall signal input – pin	Input the negative phase-B Hall device signal.
3	HC+	Phase-C hall signal input + pin	Input the positive phase-C Hall device signal.
4	HC–	Phase-C hall signal input – pin	Input the negative phase-C Hall device signal.
5	FGin+	FG amplifier input + pin	FG signal input
6	FGin–	FG amplifier input – pin	FG signal input
7	FGo	FG amplifier output pin	
8	CW/CCW	Forward/reverse switching pin	Pull-up resistor: 50 kΩ (typ.),H: Reverse/L: Forward
9	BRAKE	Brake	Pull-up resistor: 50 kΩ (typ.), L for braking (all-phase ON for lower circuit)
10	START	Start	Pull-up resistor: 50 kΩ (typ.), L for start, H for standby
11	Fref	External clock input	Pull-up resistor: 50 kΩ (typ.)
12	FGS	FG hysteresis comparator output pin	Open collector output, I_O = 1 mA (max)
13	Ready	Ready output pin	Open collector output Within ±6%: L, Otherwise: High impedance
14	SEL1	Gain Select 1	Selectable from four values. 25-kΩ pull-up resistor (typ.)
15	SEL2	Gain Select 2	Selectable from four values. 25-kΩ pull-up resistor (typ.)
16	LP1	For LPF	PLL form an external clock
17	VCO-R	Resistor pin for VCO	A resistor should be added between this pin and ground.
18	VCO-C	Capacitor pin for VCO	A capacitor should be added between this pin and ground.
19	S-GND	Ground pin	
20	INTEG-out	Integral amp output	
21	INTEG-in	Integral amp input	Negative pin
22	D-out	Speed discriminator deviation output	
23	P-out	Phase deviation output	
24	Td1	Frequency setting pin 1 for internal reference clock	Connect external CR to generate a reference clock.
25	Td2	Frequency setting pin 2 for internal reference clock	Connect external CR to generate a reference clock.
26	L1	Lead angle correction circuit	Connect an external capacitor.
27	L2	Lead angle correction circuit	Connect an external resistor for adjusting the correction gain.
28	L3	Lead angle correction circuit	Connect an external resistor for adjusting the correction gain.
29	L4	Lead angle correction circuit	Connect an external capacitor
30	CLd	Oscillation pin for lock protection circuit	A capacitor should be added between this pin and ground
31	VDD	Internal logic power supply pin	5-V output. A capacitor should be added between this pin and ground.
32	P-GND	Ground pin	
33	Vref2	8-V reference power supply	8-V output. A capacitor should be added between this pin and ground.
34	Vref1	5-V reference power supply	5-V output. A capacitor should be added between this pin and ground.
35	Vref1-R	5-V reference power supply	A resistor should be added between VCC and Vref1-R.
36	VCC	Voltage input pin for control power supply	V_{CC} (opr.) = 10 to 28 V
37	CP2	Charge pump pin	For generating upper N-ch FET gate voltage

Pin No.	Name	Pin Functions	Remarks
38	CP1	Charge pump pin	For generating upper N-ch FET gate voltage
39	CP3	Charge pump pin	For generating upper N-ch FET gate voltage
40	Idc2	Input pin for output current detection signal	GND sense pin
41	Idc1	Input pin for output current detection signal	Gate block operation when 0.25 V (typ.) or higher
42	LA (U)	Phase-A energization signal output (U1)	For source driving for phase-A output FET gate (upper N-ch)
43	OUT-A	Phase-A motor pin	
44	LA (L)	Phase-A energization signal output (L)	For phase-A output FET gate (lower N-ch)
45	LB (U)	Phase-B energization signal output (U)	For phase-B output FET gate (upper N-ch)
46	OUT-B	Phase-B motor pin	
47	LB (L)	Phase-B energization signal output (L)	For phase-B output FET gate (lower N-ch)
48	LC (U)	Phase-C energization signal output (U)	For source driving for phase-C output FET gate (upper N-ch)
49	OUT-C	Phase-C motor pin	
50	LC (L)	Phase-C energization signal output (L)	For phase-C output FET gate (lower N-ch)
51	HA+	Phase-A hall signal input + pin	Input the positive phase-A Hall device signal.
52	HA–	Phase-A hall signal input – pin	Input the negative phase-A Hall device signal.

Pin Layout



*: Device destruction caused by electrical shorts between adjacent pins
If pins 36 and 37, pins 37 and 38, or pins 39 and 40 are shorted together, the device may be permanently damaged, causing excessive current to flow, and consequently, smoke may result. To prevent overcurrent conditions or excessive current in case of an IC failure, an appropriate power supply fuse should be used. To minimize its effect, its capacitance and fusing time need to be adjusted.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	30 (Note 1)	V
Input voltage	V_{IN}	5.5 (Note 2)	V
Output voltage	V_{OUT}	5.5 (Note 3)	V
		30 (Note 4)	
		40 (Note 5)	
Output current	V_{OUT}	10 (Note 6)	mA
		20 (Note 7)	
		25 (Note 8)	
Power dissipation	P_D	1.3 (Note 9)	W
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note 1: V_{CC}

Note 2: CW/CCW, START, BRAKE, Idc2, F_{ref}, SEL1, SEL2,

Note 3: Ready, FGS

Note 4: OUT-A, OUT-B, OUT-C

Note 5: LA (U), LB (U), LC (U)

Note 6: Source current capability for LA (U), LB (U), LC (U), LA(L), LB(L), LC (L)

Note 7: Sink current capability for LA (U), LB (U), LC (U), LA(L), LB(L), LC (L)

Note 8: V_{ref1}

Note 9: When mounted on the board
(glass epoxy, 50 mm × 50 mm × 1.6 mm, copper foil 36%, thickness = 18 μm, single-sided)

The absolute maximum ratings are the limits that must not be exceeded, even for a moment, under worst possible conditions.

Exceeding the ratings may cause device breakdown, damage or deterioration, and may also lead to breakdown, damage or deterioration in other devices. This possibility should be fully considered in the design of the board.

The TB6572AFG should be operated within the specified operating range.

Operating Conditions (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	10 to 28	V
External clock frequency	F_{ref}	200 to 4000	Hz

*: The maximum F_{ref} value should be no greater than four times the minimum F_{ref} value.

Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

1. Sine Wave PWM Drive

< Energization Switching >

Upon start-up, the TB6572AFG drives the motor with square waves for 120° energization using phase detection signals (hall device signals).
If the frequency (f) of the position detection signal (hall device signal) for a single phase exceeds the specified value (f_H), the TB6572AFG switches to 180° energization.

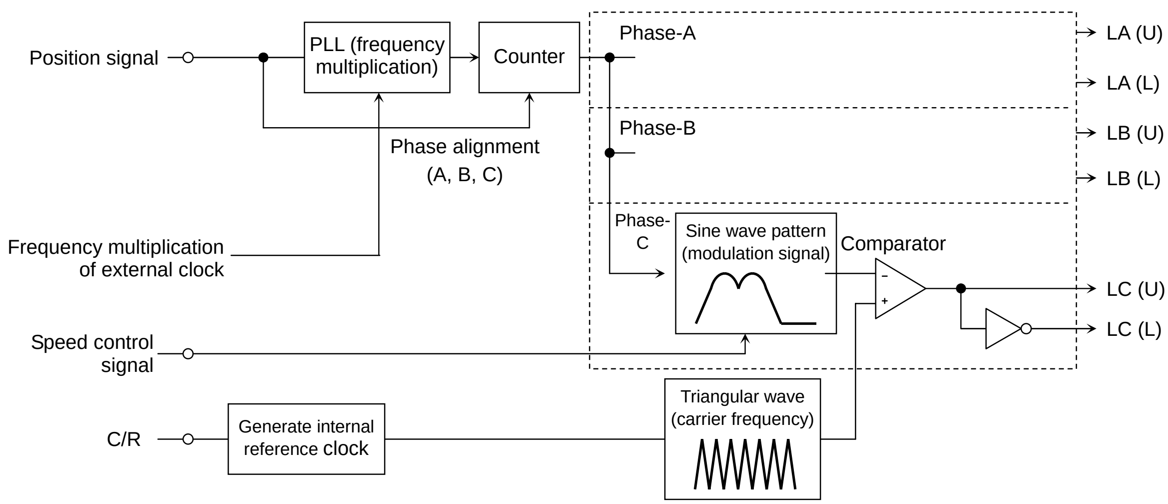
The following formula determines: $f_H = f_{x1} \div (2^{10} \times 32 \times 6)$

f_{x1}: The system clock frequency (f_{x1}) is obtained by multiplying the external clock frequency (f_{ref}).
$f_x 1 = 4 \times 1024 \times f_{ref}$
Thus, a transition from 120° energization to 180° energization occurs according to the external clock frequency.

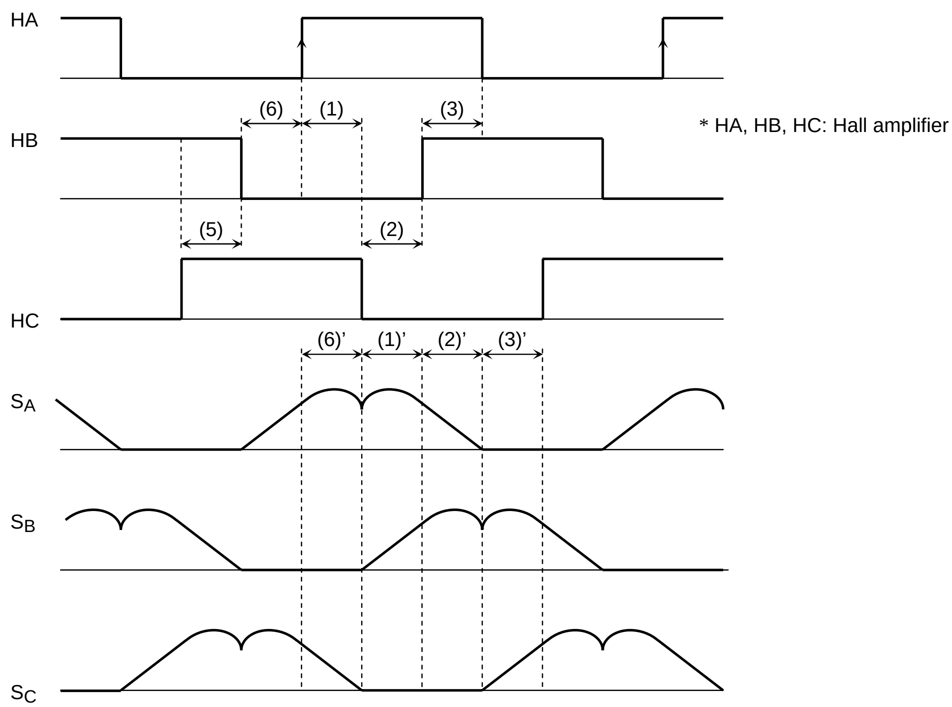
Mode Table

Rotation State	Drive Mode
$f_H > f$	Square wave drive (120°energization)
$f_H < f$	Sine wave PWM drive (180°energization)

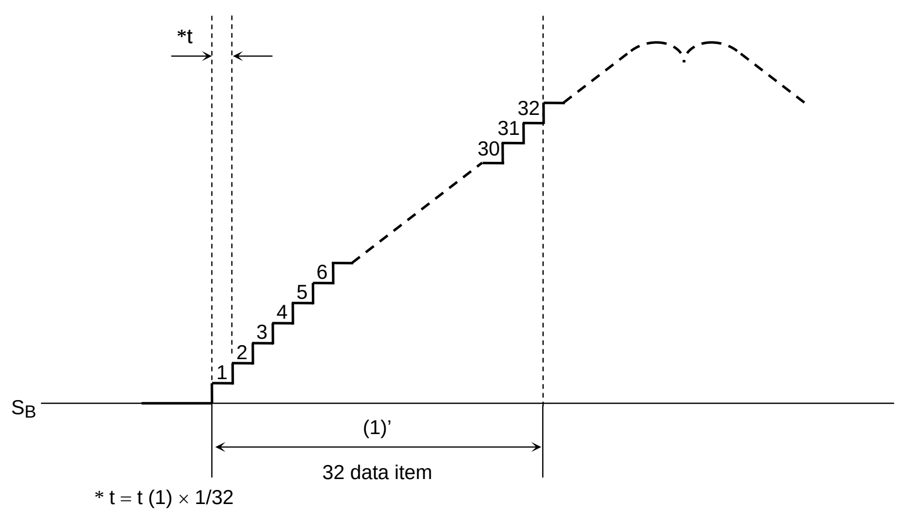
< Operation Flow >



The TB6572AFG uses position detection signals to create modulation waveforms, which it compares with triangular waves to generate sine wave PWM signals.
It counts the time between zero-crossing points for the three position detection signals (electrical angle: 60°) and uses the time as data for the next 60° phase of the modulation waveforms.
A 60° phase part of a modulation waveform consists of 32 data items. The time width for a single data item in a 60° phase part is 1/32 of that for the preceding 60° phase part. The modulation waveform proceeds with that width.

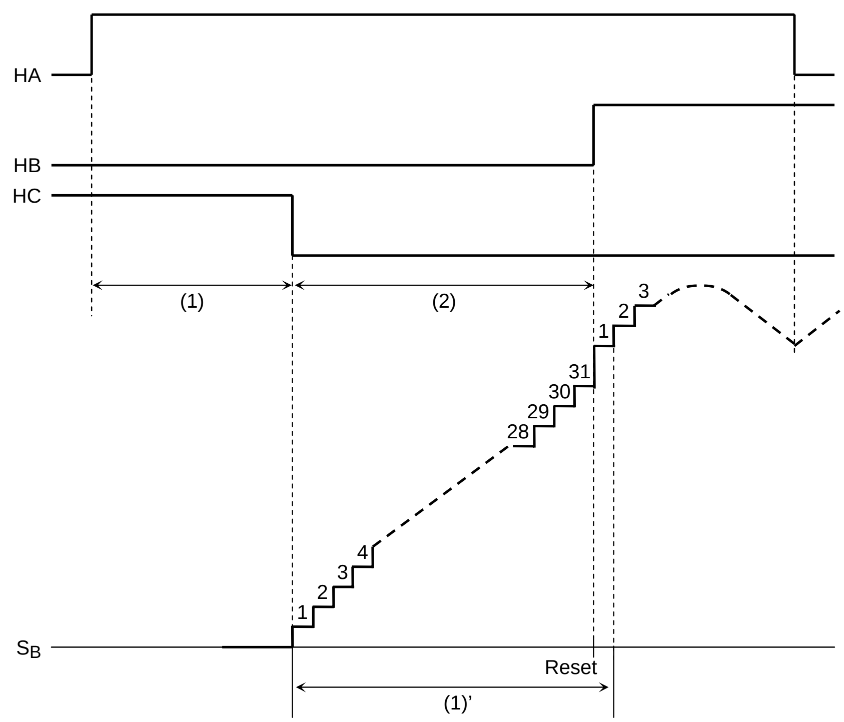


In the above chart, the time between HA rising and HC falling is marked (1). The modulation waveform within the (1)' period proceeds with a width that is 1/32 of (1). In the same way, the waveform within the (2)' period proceeds with 1/32 of (2), which is the time between HC falling and HB rising.
If next zero-crossing does not take place appear after 32 data items, the next 32 data items proceed with the same time width until next zero-crossing occurs.

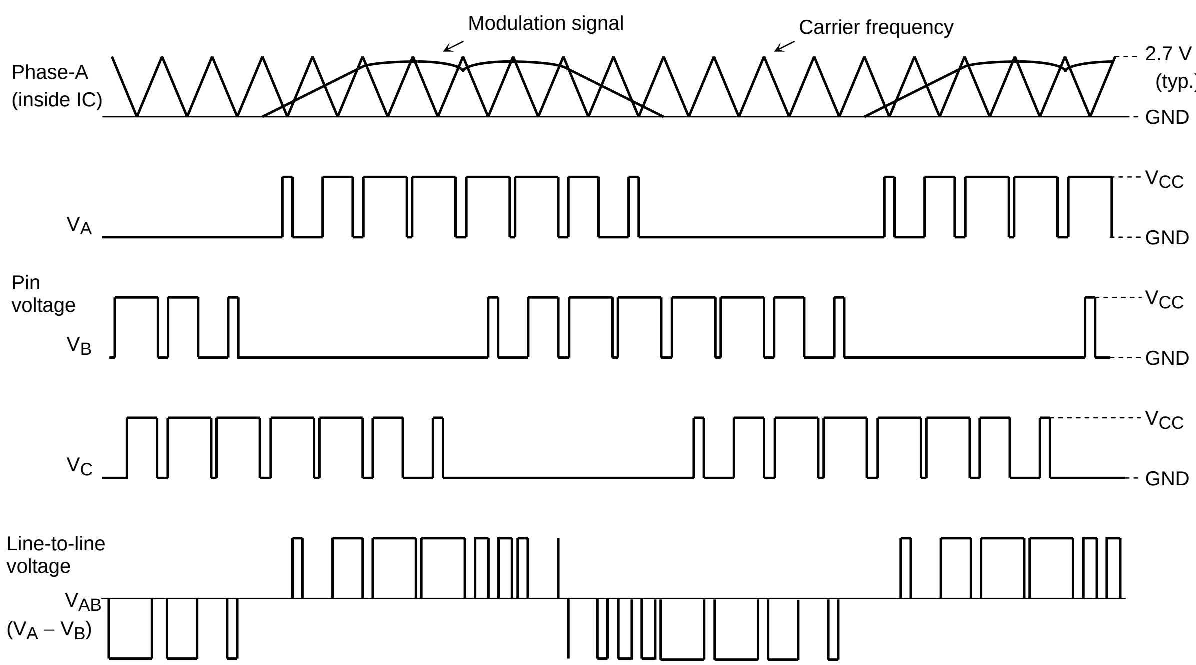


Timing charts may be simplified for explanatory purposes.

In addition, the TB6572AFG performs phase alignment with the modulation waveforms at each zero-crossing in the position detection signals.
For every 60° of electrical angle, it synchronizes with the rising and falling edges of the position detection signals (Hall amplifier output signals), thus resetting the modulation waveforms.
If zero-crossing timing is shifted in position detection signals, causing next zero-crossing to occur before 32 data items are reached for the 60° phase, the data is reset and data for the next 60° phase is started.
In that case, the modulation waveforms become discontinuous at a reset.

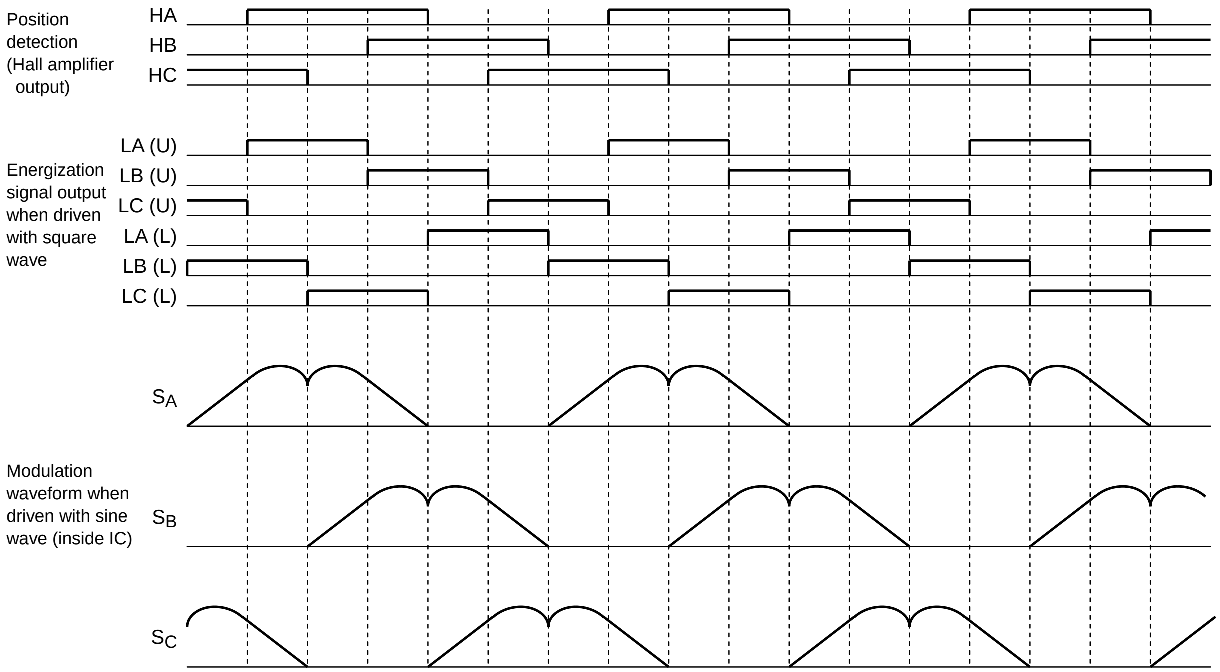


Operating Waveforms for Sine wave PWM Drive

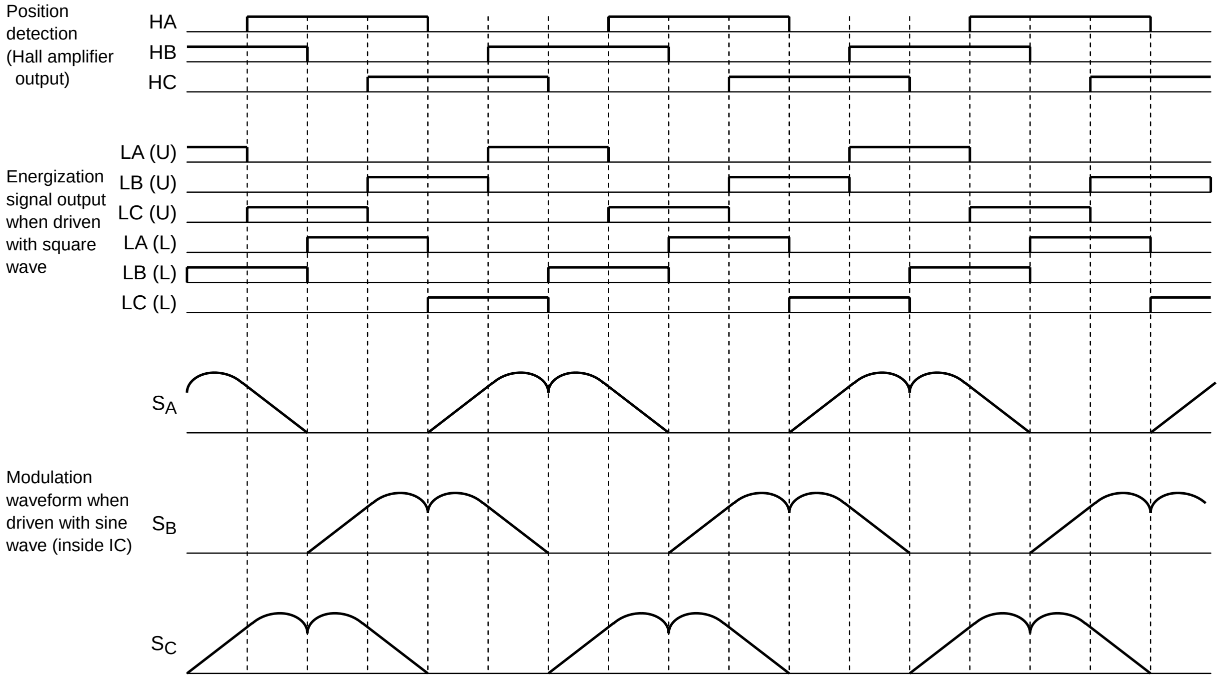


Timing charts may be simplified for explanatory purposes.

Timing Charts



Forward rotation



Reverse rotation

* HA, HB, HC: Hall amplifier outputs

Timing charts may be simplified for explanatory purposes.

2. Generating an Internal Reference Clock

The TB6572AFG uses external C and R to generate a reference clock internally.
It uses the reference clock to generate triangular waves, which determine the carrier frequency, and set a dead time.
The clock also functions as a reference clock for the charge pump (booster) and lead angle circuit ADC.

3. Generating Triangular Waves

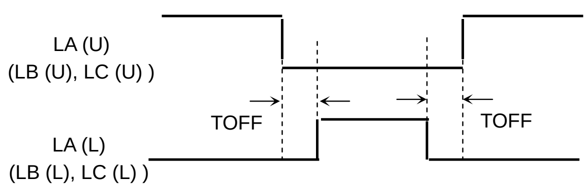
The TB6572AFG compares the modulation waveforms with triangular waves to generate PWM signals.
The carrier frequency for PWM control depends on the frequency of the triangular waves.
The triangular waves are switched according to the internal reference clock frequency.

The following formula obtains the PWM frequency, where f_{x2} is the internal reference clock frequency:
PWM frequency $f_{pwm} = f_{x2}/252$ (= triangular wave frequency)
For example: When f_{x2} = 5 MHz: fpwm = 19.8 kHz
When f_{x2} = 4 MHz: f_{pwm} = 15.8 kHz
When f_{x2} = 3 MHz: f_{pwm} = 11.9 kHz

4. Dead time Setup Circuit

To apply PWM control with synchronous regeneration for output FETs, the TB6572AFG sets a dead time for energization signal outputs, thus preventing the upper and lower output power FETs from turning on simultaneously.
It uses the internal reference clock, generated from external CR, to set a dead time.

Dead Time



The following formula obtains the dead time, where f_{x2} is the internal reference clock frequency:
Dead time td = $(1/f_{x2}) \times 4$
For example: When f_{x2} = 5 MHz: td = 1.2 μs
When f_{x2} = 4 MHz: td = 1.5 μs
When f_{x2} = 3 MHz: td = 2.0 μs

5. Charge Pump

The TB6572AFG incorporates a charge pump to drive two N-ch FETs in the external output FET configuration, in particular, to generate the gate voltage for the upper N-ch FET.
The booster voltage is V_{CC} = 8 V and the upper gate drive voltage is V_{CC} = 7.75 V.
The charge pump boosts the voltage using a frequency that is 1/16 of the internal reference clock frequency, f_{x2} (250 kHz when f_{x2} = 4 MHz).

6. Motor Output Pins

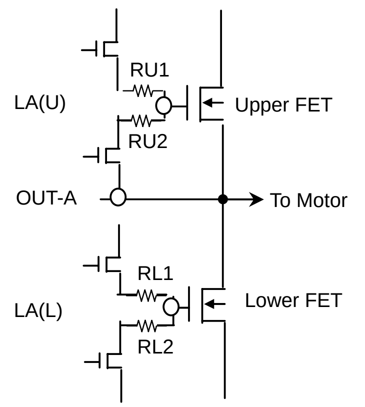
During PWM operation, the source voltage for the upper external N-ch FET swings between GND and V_M.
V_{GS} for the Nch-FET is clamped so that it does not exceed V_{GS} (max) = 20 V.

7. External FET Gate Drive Output

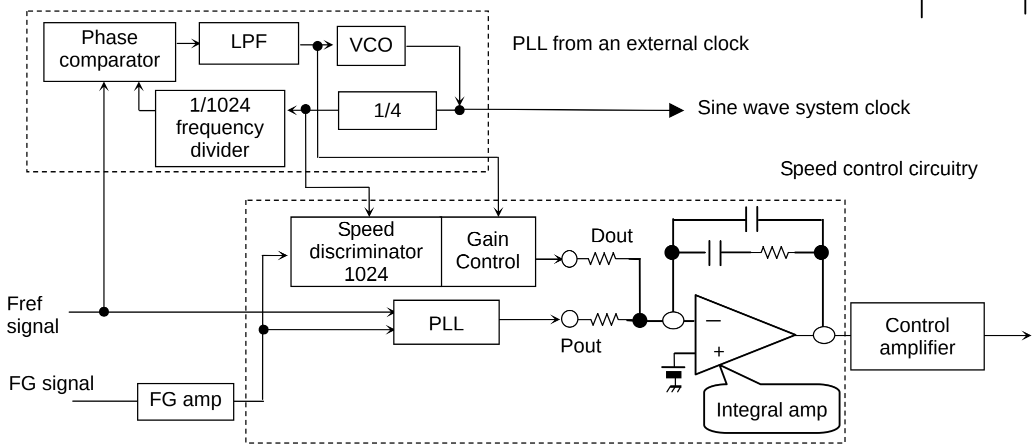
Impedance must be reduced when FETs are driven. To control impedance, source and sink outputs are configured as shown at right. Resistors are incorporated to control source and sink outputs of FETs, and each resistor value is shown below.

Incorporated resistors

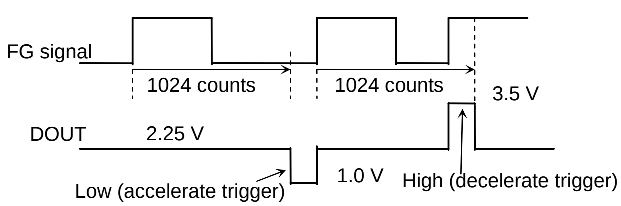
Source for upper FET: RU1 = 1 kΩ (typ.)
Sink for upper FET: RU 2 = 100 Ω (typ.)
Source for lower FET: RL1 = 1 kΩ (typ.)
Sink for lower FET: RL2 = 100 Ω (typ.)



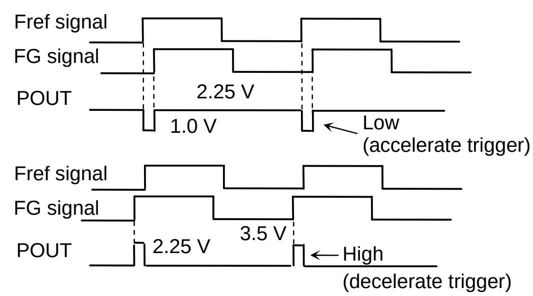
8. Speed Control



< Dout output >



< Pout output >

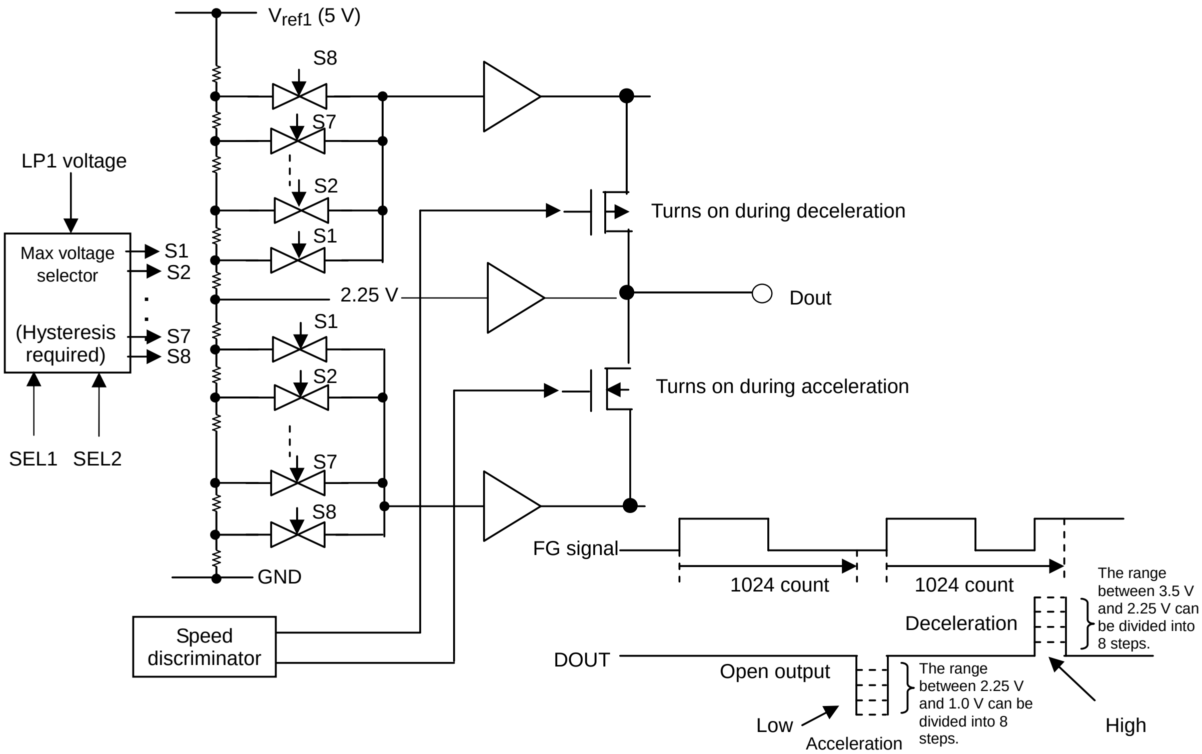


- The TB6572AFG uses a speed discriminator and PLL to control speed.
- The maximum F_{ref} value should be no greater than four times the minimum F_{ref} value.
- The speed discriminator has two counter stages, each of which alternately counts a single period of the FG signal. The resulting difference signal is output as two signals (accelerate and decelerate triggers).
- The PLL counts the phase difference between the 1/2 FG signal and reference signal. The resulting difference signal is output as two signals (accelerate and decelerate triggers). The phase difference is assumed to be zero when the FG frequency is outside the lock range (±6% of the specified value).
- FG frequency = speed control clock/speed discriminator
  → Speed control clock = FG frequency × speed discriminator
  FG frequency = 200 to 4000 k, speed discriminator = 1024
  Speed control clock = 0.2048 to 4.096 MHz
  System clock = speed control clock × 4 = 0.8192 to 16.38 MHz
- When the Fref input is open, the output is turned off.
- Note that a sudden variation in rotation speed may cause a motor current to be regenerated into the power supply, resulting in the rise of the motor voltage.

*: The internal system clock is generated by the on-chip PLL from an external clock. The system clock frequency may saturate, depending on the external LPF and VCO constants. The speed discriminator compares the reference frequency derived from the system clock against the FG frequency. If the system clock frequency saturates, the system clock is not synchronized to the FG signal. (Instead, the system clock is synchronized with the reference frequency.) At this time, the READY signal remains Low. The LPF and VCO constants should be optimized.

8.1 Gain Control Circuitry

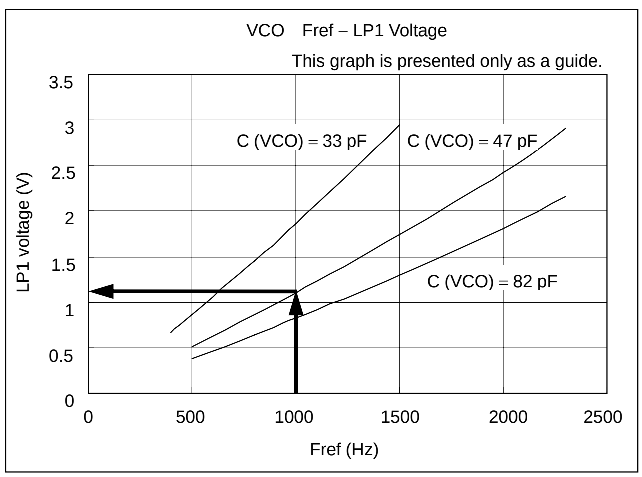
The gain control circuitry dynamically selects the gain of the speed discriminator, based on the rpm command (i.e., Fref frequency). The gain control circuitry is designed to change the peak voltage of the deviation signal from the speed discriminator, based on the Fref frequency.



The VCO input voltage (LP1 voltage) is a function of the frequency of the input clock (Fref), as shown below. The peak voltage of the DOUT signal is divided by a factor that is selected by the SEL1 and SEL2 inputs.

The thresholds for the eight analog switches are given below.

Threshold Voltage (typ.)		Analog Switch
V1	0.357 V	0 to V1: S1 ON
V2	0.714 V	V1 to V2: S2 ON
V3	1.071 V	V2 to V3: S3 ON
V4	1.429 V	V3 to V4: S4 ON
V5	1.786 V	V4 to V5: S5 ON
V6	2.143 V	V5 to V6: S6 ON
V7	2.5 V	V6 to V7: S7 ON
		V7 to 5V: S8 ON



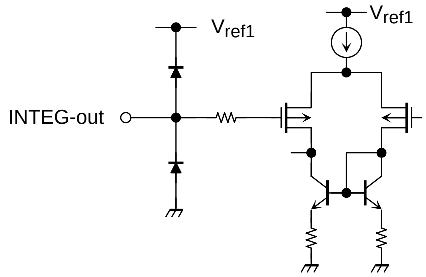
Each threshold point has a hysteresis of 20 mV.

The Dout resolution is selected by SEL1 and SEL2, as shown below.

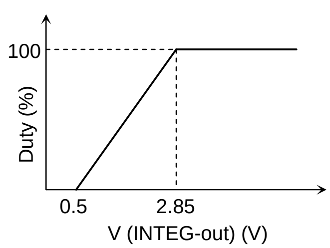
SEL1	SEL2	Selector Output	Resolution
H	H	S8 (max amplitude)	Output
H	L	S8/S4	1/2
L	H	S8/S6/S4/S2	1/4
L	L	S8 to S1	1/8

The SEL1 and SEL2 inputs have a 25-kΩ pull-up resistor. These inputs are held high when undriven.

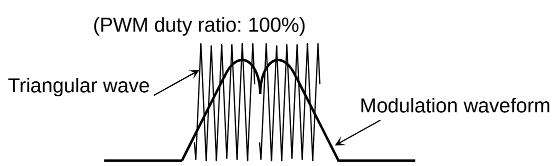
8.2 Control Amplifier



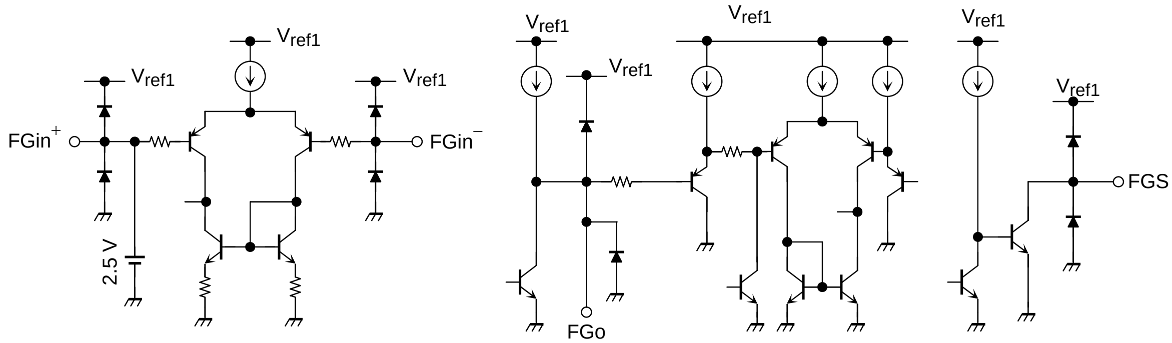
- The voltage integrated in the charge pump is input to the control amplifier.
  The input is placed in high-impedance state because it is a P-ch gate.
  The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.
- The control amplifier circuit has an offset of 0.45 V (typ.). If the INTEG-out pin voltage exceeds the offset value, the energization signal outputs become active. It incorporates a clamp circuit that saturates the PWM duty ratio for the energization signal outputs when the INTEG-out pin voltage becomes 2.85 V (typ.).



- The PWM duty ratio indicates the value at the peak of the modulation waveform. A duty ratio of 100% indicates that the peak value coincides with the peak of the triangular wave.



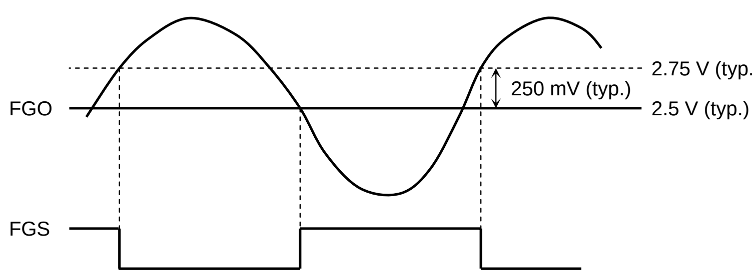
8.3 FG Amplifier/Hysteresis Comparator



- The FG amplifier supports pattern FG and incorporates an internal reference voltage of 2.5 V. Entering a sine wave of 50 mV_{pp} or greater results in a signal multiplied by the gain being output. The open loop gain is 45 dB (min) (design target value).

- The FG amplifier is followed by a hysteresis comparator, which compares the FG output and delivers it to the FGS.
  The comparator has a single-side hysteresis of 250 mV for the 2.5 V reference voltage. The square wave signal output from the FGS enters the internal counter.
  The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

- The FGO output dynamic range is as follows:
  1.0 V to V_{ref} − V at IFGO = ±200 μA



- The FGS has an open-collector output. Connect a pull-up resistor considering the following characteristics.
  The input current is 1 mA (max).
  VFGS = 0.7 V (max) at IFGS = 1 mA
- The FG comparator has a 1-μs filter to improve the noise immunity of FGO at the falling edge of FGS.

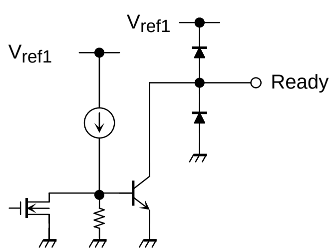
9. Hall Amplifier

- The Hall amplifier accepts Hall device output signals. If input signals contain noise, connect a capacitor between inputs.
- The common-mode input voltage range is: VCMRH = 0.5 to 3.4 V.
  The Hall amplifier has an input hysteresis of ±16 mV (typ).
- The Hall amplifier converts Hall device signals into square waves, which then enter the internal logic.
- Outputs from the Hall amplifier are pulled up with resistors. If positive/negative inputs are open, the output is recognized as high. If the Hall amplifier outputs are H: H: H or L: L: L, the energization outputs are as follows:
  LA (U) = LB (U) = LC (U) = L and LA (L) = LB (L) = LC (L) = L.

10. Ready Circuit

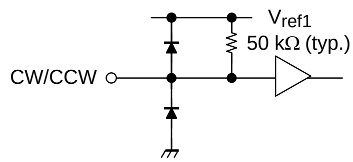
- The Ready circuit indicates the motor rotation speed state using two states (L and HZ) of an open-collector output.
  When the motor is rotating, the circuit counts FG signals and outputs the following states according to whether the frequency is within or outside ±6% of the specified value:
  The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.
  - Within ±6% of motor rotation speed: L output
  - Outside ±6% of motor rotation speed: HZ (high impedance)

- Connect a pull-up resistor to the Ready output pin. Determine the resistance considering the following characteristics. The input current is 2 mA (max).
  VCER = 0.5 V (max) at IR = 2 mA



*: The internal system clock is generated by the on-chip PLL from an external clock. The system clock frequency may saturate, depending on the external LPF and VCO constants. The speed discriminator compares the reference frequency derived from the system clock against the FG frequency. If the system clock frequency saturates, the system clock is not synchronized to the FG signal. (Instead, the system clock is synchronized with the reference frequency.) At this time, the READY signal remains Low. The LPF and VCO constants should be optimized.

11. Forward/Reverse Rotation Circuit



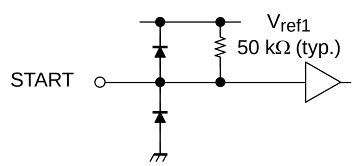
The circuit accepts a TTL input and incorporates a pull-up resistor.

CW/CCW Input	Mode
H	Reverse
L	Forwared

Forward: Hall device signals $HA^+ \rightarrow HB^+ \rightarrow HC^+$

Note that abrupt switching between forward and reverse rotation may result in an output FET being damaged due to reverse torque.

12. Start Circuit

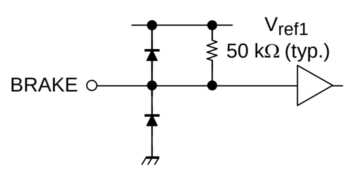


The circuit accepts a TTL input and incorporates a pull-up resistor.

START Input	Mode
H	Stop
L	Start

The START input should be asserted High after V_{CC} power-on. It is recommended to deassert the START input after the system clock, fx1, has stabilized. Keep in mind that the motor will not start if CLK, START and V_{CC} are applied in this order.

13. Brake

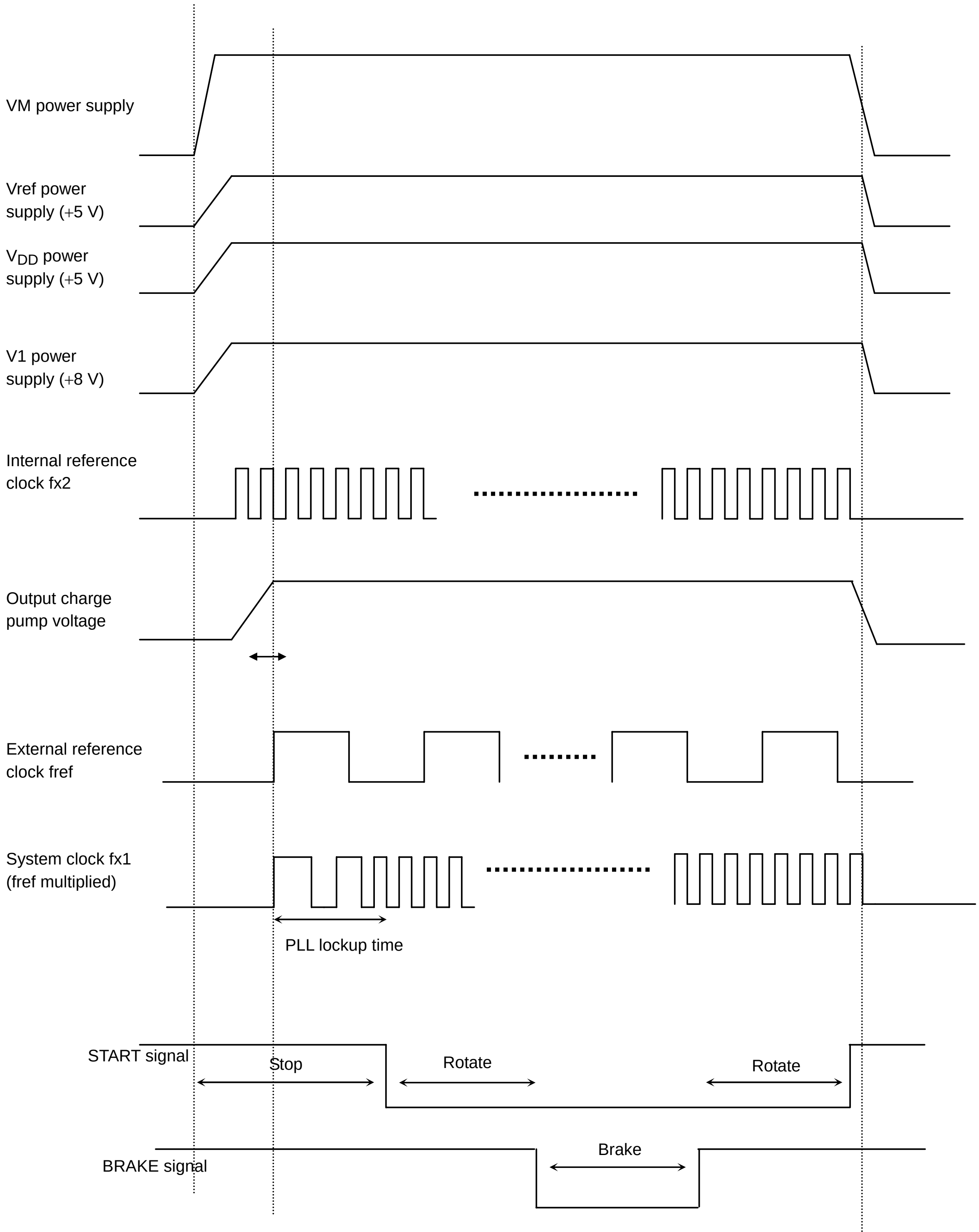


The circuit accepts a TTL input and incorporates a pull-up resistor.

BRAKE Input	Mode
H	OPERATION
L	BRAKE

Note that abrupt braking from high-speed rotation may result in an output FET being damaged.

14. Operation Sequence



START Signal	BRAKE Signal	Mode	Description
H	H or L	Stop	Turn all external FETs off.
L	H	Rotate	Energize
L	L	Brake	Turn all lower external FETs off.

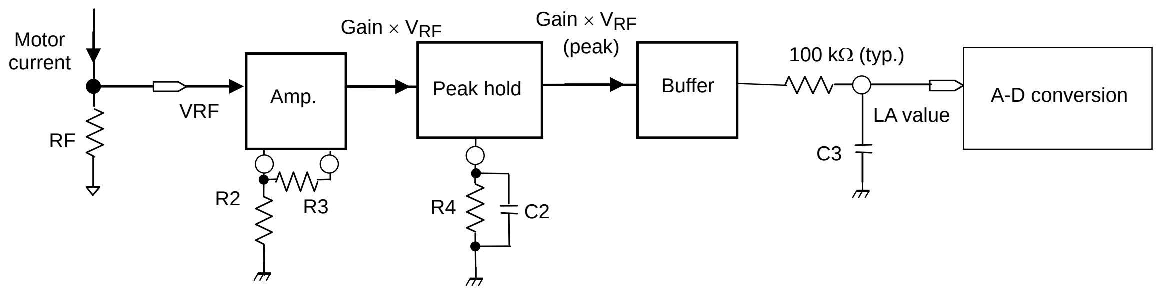
Timing charts may be simplified for explanatory purposes.

15. Automatic Phase Lead Angle Correction Circuit

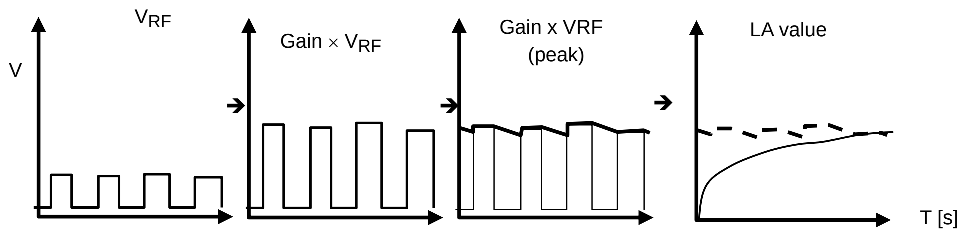
Timing charts may be simplified for explanatory purposes.

- The lead angle correction circuitry is incorporated, and the motor current value flows into the circuit.

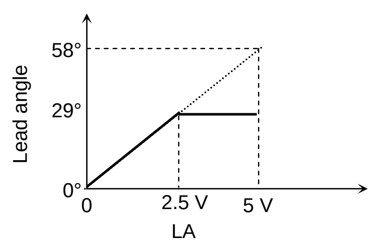
Automatic Lead angle Correction



*: Gain = (R2 + R3)/R2



- The circuit can advance the phase of an energization signal relative to the induced voltage for input of 0 to 2.5 V (16 steps).
  0 V → 0°
  2.5 V → 29° (29° for an input voltage higher than 2.5 V)



< This graph is presented only as a guide. >

- The circuit clamps the lead angle at 29°.
- It logically clamps the angle between 0° and 29°, rather than clamping the input voltage.

16. Lock Protection Circuit

- The circuit turns the output power FET off if the motor is locked.
- It turns off both upper and lower output power FETs if it detects the Ready signal with the following condition satisfied.
  The circuit latched state is terminated once the TB6572AFG is placed in the stop or brake state.

Detected Signal	Condition for Triggering Lock Protection
Ready signal	The Ready signal output remains high for at least 5 seconds (typ.).

- A reference oscillation waveform for lock protection is generated using an external capacitor connected to the CLD pin and counted with the internal 7-bit counter.
- When CLD = 0.1 μF, the oscillation frequency is approximately 25 Hz, so that the lock protection triggering time is 5.1 seconds (typ.).

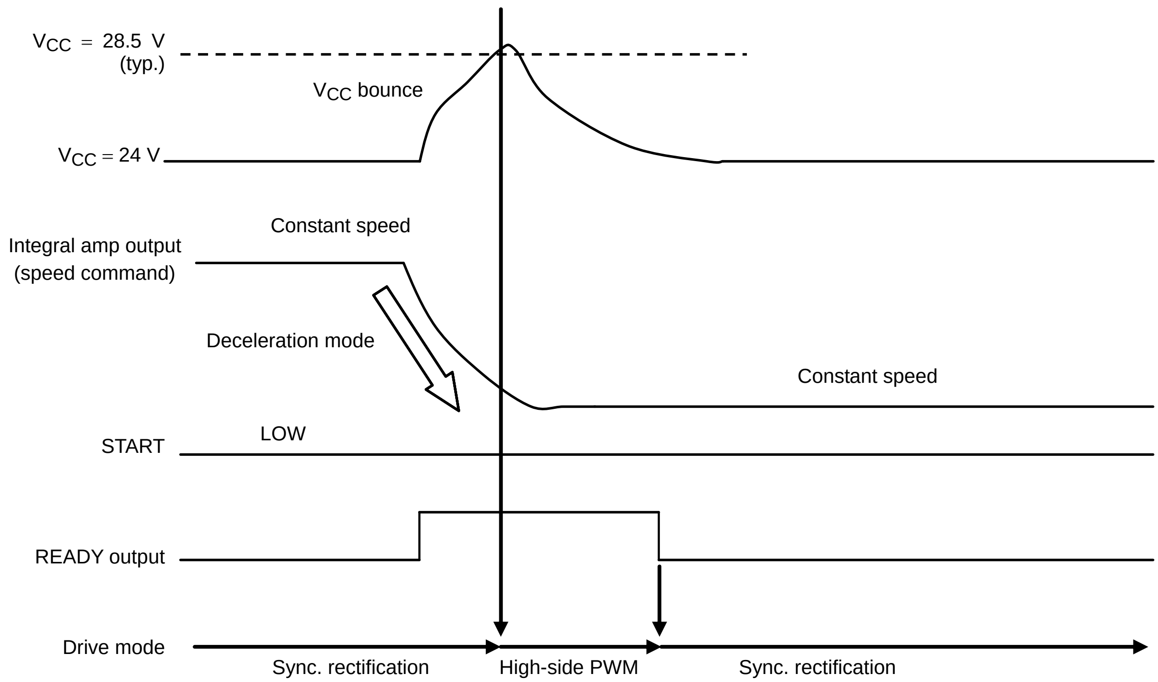
17. V_{CC} Bounce Prevention

The TB6572AFG contains a circuit to avoid the V_{CC} bounce caused by abrupt acceleration or deceleration. This is accomplished by switching the drive mode from synchronous rectification to high-side PWM.

(1) Switching from synchronous rectification to high-side PWM
The TB6572AFG continually monitors the V_{CC} voltage. If Vcc rises above 28.5 V (typ.), the drive mode changes to high-side PWM.

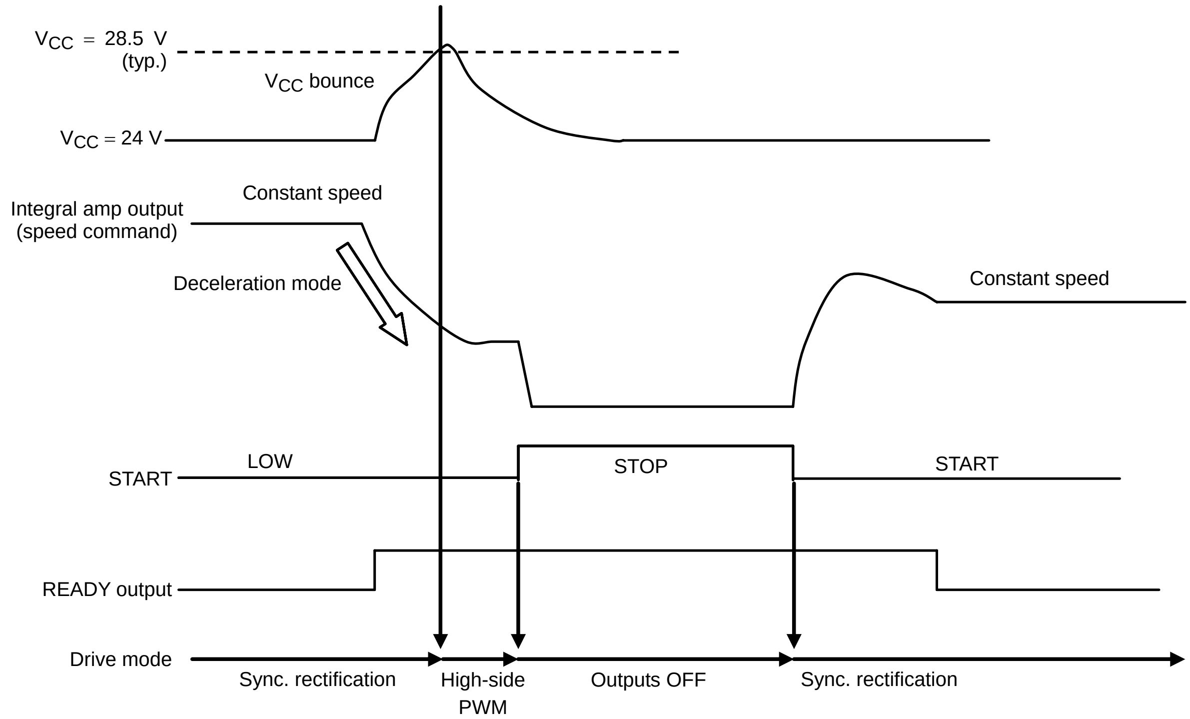
(2) Switching from high-side PWM to synchronous rectification
When the integral amp output levels off for a constant motor speed (with the READY output being Low), the drive mode changes to synchronous rectification.

< V_{CC} Bounce Prevention Mode (normal) >



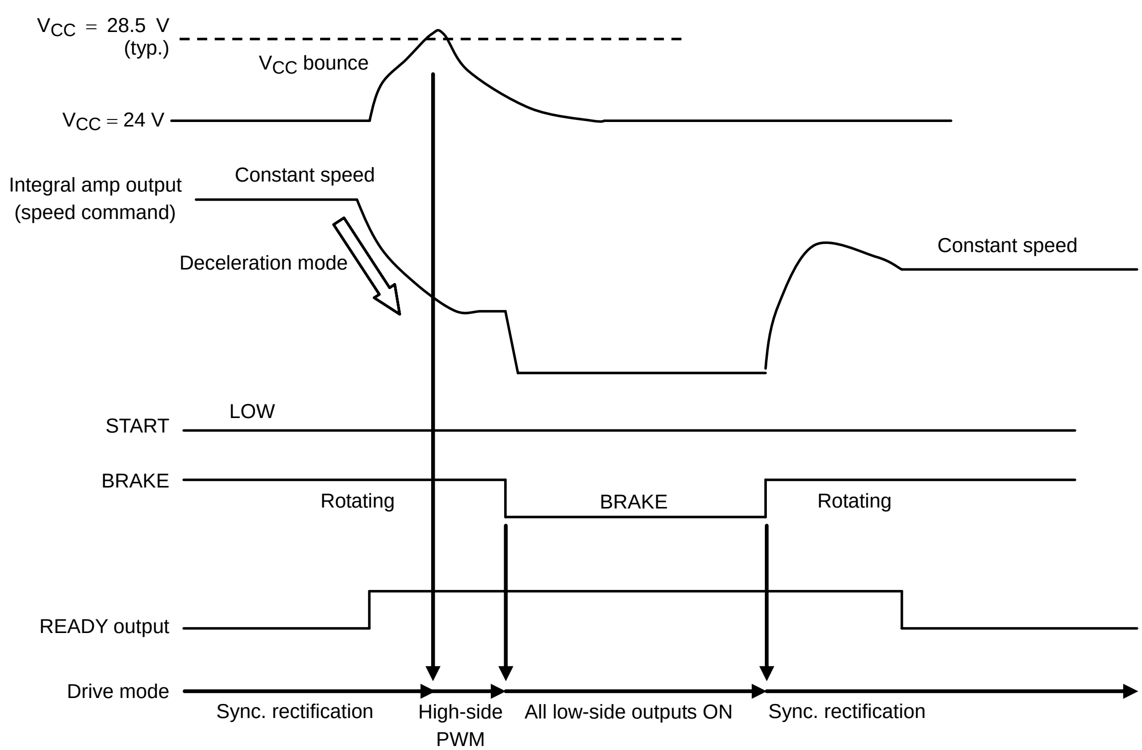
When the drive mode has changed to high-side PWM, the current waveform may be distorted. When the drive mode returns to synchronous rectification, sine-wave driving is used with 180° energization.
Normally, V_{CC} (max) should be kept below the minimum V_{CC} bounce prevention threshold of 27.6 V, V_K (min).
This feature does not guarantee that any V_{CC} bounce will be avoided. In cases where V_{CC} bounces due to a cause in the power supply circuit, a separate V_{CC} bounce filter should be added.

< V_{CC} Bounce Prevention Mode (when the TB6572AFG is put in STOP mode during deceleration) >



*: The READY output can not be driven Low when START = High (STOP mode). Thus the drive mode returns to synchronous rectification at the falling edge of START.

< V_{CC} Bounce Prevention Mode (when the TB6572AFG is put in BRAKE mode during deceleration) >



*: The READY output can not be driven Low when BRAKE = Low (BRAKE mode). Thus the drive mode returns to synchronous rectification at the rising edge of BRAKE.

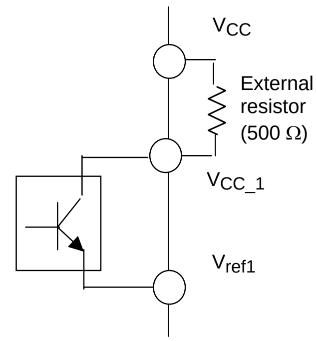
18. Constant Voltage Circuit

(1) V_{ref1}

The circuit creates 5 V for biasing the internal analog circuit and outputs it from the V_{ref} pin.
Connect a capacitor (0.1 μF to 1 μF) between the V_{ref1} pin and S-GND to prevent oscillation and absorb noise.
The output load current is 25 mA (tentative value).

V_{ref} = 5 V (typ.) ±0.5 V at Io = 20 mA

*: The Vref1 pin provides a Hall bias current to prevent an ill behavior from occurring when the V_{CC} supply voltage is removed. To reduce the chip's power consumption, an external resistor should be added as shown at right.



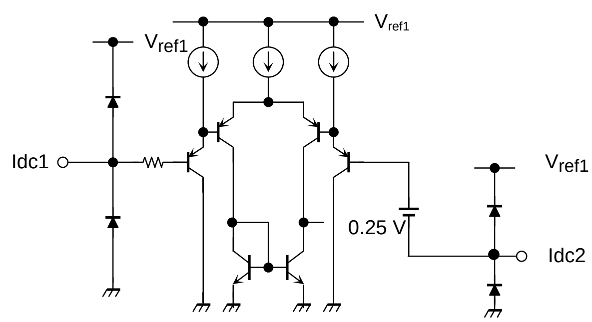
(2) V_{DD}

The circuit outputs 5 V for biasing the internal logic circuit from the V_{DD} pin.
Connect a capacitor (1 μF recommended) between the V_{DD} pin and S-GND to prevent oscillation and absorb noise.
Connect no load to the V_{DD} pin.

(3) V_{ref2}

The circuit creates 8 V for output FET gate driving and outputs it from the V_{ref2} pin.
Connect a capacitor (1 μF or larger) between the V_{ref2} pin and P-GND to prevent oscillation and absorb noise.

19. Overcurrent Protection Circuit



- The circuit turns the external output power FET off if the detected voltage is higher than 0.25 V (typ.). It re-activates the FET according to the carrier frequency.
  Note that the Idc pin accepts a direct analog comparator input and is highly sensitive. Use C and R, therefore, for filtering so that output current noise due to chopping does not activate the overcurrent protection circuit.

20. Power Supply Monitor Circuit

The circuit monitors the V_{ref} and V_{CC} voltages and turns the external power FET off if any of the following conditions are satisfied:

- V_{CC} (H) ≤ 9.5 V (typ.), V_{CC} (L) ≤ 9.0 V (typ.)
- V_{ref1} (H) ≤ 4.5 V (typ.), V_{ref1} (L) ≤ 4.0 V (typ.)
- V_{DD} (H) ≤ 3.2 V(typ.), V_{ref1} (L) ≤ 2.7 V(typ.)

21. Thermal Shutdown Circuit

The circuit turns the external output power FET off if the junction temperature TSD (ON) exceeds 160°C. The thermal shutdown state is terminated once the TB6572AFG is placed in the stop or brake state.

- The above protection features are only intended to temporarily protect the device against irregular conditions and do not provide an absolute protection of the device.

Electrical Characteristics (V_{CC} = 24 V, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Supply current		I_{CC1}		Start	10.5	16.5	22.5	mA
		I_{CC2}		Stop	8.0	12.7	16.0	
Hall amplifier	Common-mode input voltage range	V_{CMRH}			0.5	—	3.4	V
	Input amplitude range	V_H			50	—	—	mV_{pp}
	Input hysteresis	V_{hysH}	—	(design target value)	8	16	24	mV
	Input current	I_{inH}		VCMRH = 2.5 V, 1-phase	—	—	1	μA
Ready circuit	Remaining output voltage	V_{CER}		Open collector output, ICER = 2 mA	—	—	0.5	V
	Output leakage current	I_{LR}		Vready = 5 V	—	—	1	μA
FG amplifier	Input offset voltage	V_{OSFG}			—		±7	mV
	Remaining output voltage (upper)	$V_{OFG\ (H)}$		IFG = 100 μA (source current)	V_{ref1} −1.2	—	Vref1	V
	Remaining output voltage (lower)	$V_{OFG\ (L)}$		IFG = 100 μA (sink current)	—	—	1.2	
	Reference voltage	V_{refFG}			2.2	$V_{ref1/2}$	2.8	V
FG hysteresis comparator	Hysteresis width	V_{hysS}			0.20	0.25	0.30	V
	Remaining output voltage	V_{CES}		Open collector output, ICES = 1 mA	—	—	0.5	V
	Output leakage current	V_{LS}		V_{FGS} = 5 V	—	—	1	μA
Control input circuit	Input voltage (H)	$V_{IN\ (H)}$		CW/CCW, BRAKE, START, SEL1,SEL2	2.0	—	5.5	V
	Input voltage (L)	$V_{IN\ (L)}$			0	—	0.8	
	Input current (1H)	$I_{IN\ (H)}$		V_{IN} = 5 V	—	—	1	μA
	Input current (1L)	$I_{IN\ (L)}$		CW/CCW, BRAKE, START, V_{IN} = GND	70	100	150	
	Input current (2H)	$I_{IN\ (H)}$		V_{IN} = 5 V	—	—	1	
	Input current (2L)	$I_{IN\ (L)}$		SEL1,SEL2,V_{IN} = GND	140	200	300	
Fref input circuit	Input voltage (H)	$V_{IN\ (H)}$		F_{ref}	2.0	—	5.5	V
	Input voltage (L)	$V_{IN\ (L)}$		F_{ref}	0	—	0.8	
	Input current (H)	$I_{IN\ (H)}$		V_{IN} = 5 V	—	—	1	μA
	Input current (L)	$I_{IN\ (L)}$		V_{IN} = GND	60	100	150	
Charge pump voltage		V_G		CP1-CP2: 0.047 μF, CP3: 0.1 μF	V_{CC} + 7	V_{CC} + 8	V_{CC} + 9	V
Energization signal output voltage		$V_{O\ (U)\text{-}(H)}$		LA (U)/LB (U)/LC (U), I_O = 1 mA	V_G −1.5	—	V_G	V
		$V_{O\ (U)\text{-}(L)}$		LA (U)/LB (U)/LC (U), I_O = 5 mA	—	—	0.825	
		$V_{O\ (L)\text{-}(H)}$		LA (L) /LB (L) /LC (L), I_O = 1 mA	6.9	7.7	8.5	
		$V_{O\ (L)\text{-}(L)}$		LA (L) /LB (L) /LC (L), I_O = 5 mA	—	—	0.775	
Internal supply voltage output		V_{DD}			4.5	5.0	5.5	V
		V_{ref1}		R_{ref1} = 500 Ω, I_{ref1} = 20 mA	4.5	5.0	5.5	
		V_{ref2}			8.2	8.7	9.2	
Current limiter circuit reference voltage		V_{DC}			0.23	0.25	0.27	V
Internal reference clock frequency		fx2		R = 10 kΩ, C = 59 pF	3.1	3.5	3.9	MHz
Dead time (Note 4)		TOFF1		R = 10 kΩ, C = 51 pF	1.2	1.7	2.2	μs
		TOFF2		R = 10 kΩ, C = 51 pF	1.2	1.7	2.2	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Phase lead angle controller	Lower clamp limit	ACLH			—	29	—	°
Control amplifier	Rising voltage	VCR			0.3	0.5	0.6	V
	Saturation voltage	VCLP			2.6	2.85	3.0	
	Input current	I_{INCP}		(design target value)	—	0	—	μA
Integral amplifter	Reference voltage	V_r			2.1	2.25	2.4	V
	High-level output voltage	V_{INT} (H)			3.1	3.3	3.5	
	Low-level output voltage	V_{INT} (L)			—	—	0.3	
	Input bias current	IB (int)			−1	—	1	μA
	Open-loop gain			(design target value)	—	50	—	
Speed discrimina tor	Maximum output voltage	VP (H)			3.25	3.5	3.75	V
	Minimum output voltage	VP (L)			0.75	1.0	1.25	
Speed PLL output	Maximum output voltage	VP (H)			3.25	3.5	3.75	V
	Minimum output voltage	VP (L)			0.75	1.0	1.25	
V_K monitor	PWM drive monitor voltage	V_K			27.6	28.6	29.6	V
Lock protection circuit	Reference clock frequency	F_{Ld}		CLd = 0.1 μF	19	25	34	Hz
	Operating time	t_{Ld}		CLd = 0.1 μF	3.7	5.1	6.6	s

Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

1. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

2. Timing Charts

Timing charts may be simplified for explanatory purposes.

3. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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4. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

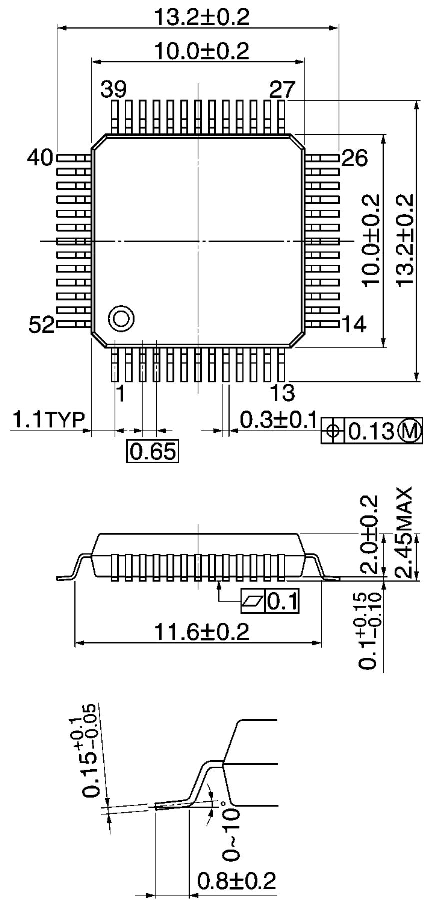
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

Package Dimensions

QFP52-P-1010-0.65 Unit: mm



Weight: 0.50 g (typ.)

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