CAT5127, CAT5129

32-Tap Digitally Programmable Potentiometer (DPP™)

DNDUCTOR, INC



FEATURES

- 32-position linear taper potentiometer
- Non-volatile EEPROM wiper storage
- Low standby current
- Single supply operation: 2.5V 5.5V
- Increment Up/Down serial interface
- Resistance values: 10kΩ, 50kΩ and 100kΩ
- CAT5127 in tiny 8-lead 2mm x 2.5mm TDFN and MSOP packages
- CAT5129 in the 6-lead TSOT23 package

APPLICATION

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

For Ordering Information details, see page 12.

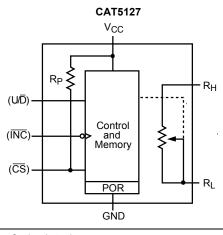
DESCRIPTION

The CAT5127/CAT5129 are single digitally programmable potentiometers (DPP[™]) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5127 contains a 32-tap series resistor array connected between two terminals R_H and R_L . The CAT5129 contains a 32-tap series resistor array connected between two terminals R_H and GND. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper. The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control the CAT5127/CAT5129 of is accomplished with three input control pins, \overline{CS} , U/ \overline{D} , and INC. The INC input increments the wiper in the direction which is determined by the logic state of the U/\overline{D} input. The \overline{CS} input is used to select the device and also store the wiper position prior to power down.

The devices are used as two-terminal variable resistors. DPPs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

FUNCTIONAL DIAGRAM



© Catalyst Semiconductor, Inc. Characteristics subject to change without notice CAT5129

V_{CC}

R_H



PIN CONFIGURATION

MSOP/TDFN			
		T5127	
INC	1	8	V_{CC}
U/D	2	7	ĊŚ
R_{H}	3	6	R_{L}
GND	4	5	NC
			•
		T23-6	
	CA	T5129	
ĊS	1	6	V_{CC}
GND	2	5	R_{H}
U/D	3	4	INC

PIN DESCRIPTIONS

Name	Function	CAT5127 MSOP/TDFN	CAT5129 SOT23
INC	Increment Control	1	4
U/D	Up/Down Control	2	3
R _H	Potentiometer High Terminal	3	5
GND	Ground	4	2
NC	No Connect	5	-
R_{L}	Potentiometer Low Terminal	6	-
ĊŚ	Chip Select	7	1
V_{CC}	Supply Voltage	8	6

DEVICE DESCRIPTION

INC: Increment Control Input

The $\overline{\text{INC}}$ input moves the wiper in the up or down direction determined by the condition of the U/D input.

U/D: Up/Down Control Input

The U/ \overline{D} input controls the direction of the wiper movement. When in a high state and \overline{CS} is low, any high-to-low transition on \overline{INC} will cause the wiper to move one increment toward the R_H terminal. When in a low state and \overline{CS} is low, any high-to-low transition on \overline{INC} will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

 R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_L: Low End Potentiometer Terminal (CAT5127 only)

 R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

CS: Chip Select

The chip select input is used to activate the control input of the device and is active low. When in a high state, activity on the \overline{INC} and U/\overline{D} inputs will not affect or change the position of the wiper. CAT5127 has an internal pull-up resistor on the \overline{CS} input pin.

V_{cc}: Supply Input for the device.



DEVICE OPERATION

The CAT5127 operates like a digitally controlled variable resistor with R_H and R_L equivalent to the high and low terminals. There are 32 available tap positions including the resistor end points, R_H and R_L . There are 31 resistor elements connected in series between the R_H and R_L terminals.

The CAT5129 operates like a digitally controlled variable resistor with R_H equivalent to the high terminal. There are 32 available tap positions including the resistor end points, R_H and GND. There are 31 resistor elements connected in series between the R_H and GND terminals.

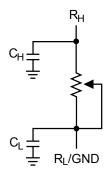
Operation is controlled by three inputs, \overline{INC} , U/\overline{D} and \overline{CS} . These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the \overline{INC} and \overline{CS} inputs.

With \overline{CS} set LOW, the device is selected and will respond to the U/D and \overline{INC} inputs. HIGH to LOW transitions on \overline{INC} wil increment or decrement the wiper (depending on the state of the U/D input and five-bit counter). The wiper, when at either end terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever \overline{CS} transitions HIGH while the \overline{INC} input is also HIGH. When the device is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With INC set low, the device may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

OPERATION MODES

INC	ls	U/D	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L/GND
High	Low to High	Х	Store Wiper Position
Low	Low to High	Х	No Store, Return to Standby
Х	High	Х	Standby



Variable Resistor Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Parameters	Ratings	Units
Supply Voltage		
V_{CC} to GND	-0.5 to +7V	V
Inputs		
CS to GND	-0.5 to V _{CC} +0.5	V
INC to GND	-0.5 to V _{CC} +0.5	V
U/D to GND	-0.5 to V _{CC} +0.5	V
H to GND	-0.5 to V _{CC} +0.5	V
L to GND	-0.5 to V _{CC} +0.5	V
W to GND	-0.5 to V _{CC} +0.5	V

Parameters	Ratings	Units
Operating Ambient Temperature		
Commercial ('C' or Blank suffix)	0 to 70	°C
Industrial ('l' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to 150	°C
Lead Soldering (10 sec max)	+300	°C

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Тур	Max	Units
$V_{ZAP}^{(2)}$	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
I _{LTH} ^{(2) (3)}	Latch-Up	JEDEC Standard 17	100			mA
T _{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N _{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

Notes:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} + 1V

(4) These parameters are periodically sampled and are not 100% tested.



DC ELECTRICAL CHARACTERISTICS

Vcc = +2.5V to +5.5V unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Тур	Max	Units
V _{CC}	Operating Voltage Range		2.5		5.5	V
	CAT5127	$V_{CC} = 5.5V, f = 1MHz, I_W = 0$			260	μA
	Supply Current (Increment)	$V_{CC} = 3.3V, f = 1MHz, I_W = 0$			150	μA
I _{CC1}	CAT5129	$V_{CC} = 5.5V, f = 1MHz, I_W = 0$			160	μA
	Supply Current (Increment)	$V_{CC} = 3.3V, f = 1MHz, I_W = 0$			50	μA
	Supply Current (Write)	Programming, V_{CC} = 5.5V		300	600	μA
I _{CC2}	Supply Current (write)	Programming, V_{CC} = 3.3V		150	400	μA
I _{SB1} ⁽¹⁾	Supply Current (Standby)	$\overline{CS} = V_{CC} - 0.3V$ U/D, INC = V _{CC} or GND		0.35	1	μA

Logic Inputs

Symbol	Parameter	Conditions	Min	Тур	Max	Units
	CAT5127 Input Leakage Current	U/\overline{D} , $\overline{INC} = V_{CC}$			1	μA
I _{IH}	CATST27 Input Leakage Current	$\overline{\text{CS}} = V_{\text{CC}} - 0.3 \text{V}$			1	μA
	CAT5129 Input Leakage Current	$V_{IN} = V_{CC}$			1	μA
	CAT5127 Input Leakage Current	$U/\overline{D}, \overline{INC} = 0$			-1	μA
IIL	CATST27 Input Leakage Current	$\overline{CS} = 0$			-120	μA
	CAT5129 Input Leakage Current	V _{IN} = 0V			-1	μA
V _{IH2}	CMOS High Level Input Voltage	2.5V ≤ V _{CC} ≤ 5.5V	V _{CC} x 0.7		V _{CC} + 0.3	V
V _{IL2}	CMOS Low Level Input Voltage	$2.5V \le V_{\rm CC} \le 5.5V$	-0.3		V _{CC} x 0.2	V
V _{IH1}	CAT5129 TTL High Level Input Voltage	3.6V ≤ V _{CC} ≤ 5.5V	2		V _{cc}	V
V _{IL1}	CAT5129 TTL Low Level Input Voltage		0		0.8	V

POTENTIOMETER CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Тур	Max	Units
		-10 Device		10		
R _{POT}	Potentiometer Resistance	-50 Device		50		kΩ
		-00 Device		100		
R _{TOL}	Pot Resistance Tolerance				± 20	%
V _{RH}	Voltage on R _H pin		0		V _{CC}	V
V _{RL}	Voltage on R _L pin		0		V _{CC}	V
RES	Resolution			3.2		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
Б	Winer Registeres	$V_{\rm CC}$ = 5V		70	100	Ω
R _{wi}	Wiper Resistance	V _{CC} = 2.5V		150	200	Ω
TC _{RPOT} ⁽³⁾	TC of Pot Resistance			±30	±300	ppm/ºC
TC _{RATIO} ⁽³⁾	Ratiometric TC			±3	20	ppm/ºC
V _N ⁽³⁾	Noise	100kHz / 1kHz		8/24		nV/√Hz
$C_{\rm H}/C_{\rm L}/C_{\rm W}^{(3)}$	Potentiometer Capacitances			8/8/25		pF
Fc ⁽³⁾	Frequency Response	Passive Attenuator, $10k\Omega$		1.7		MHz

Notes:

(1) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} + 1V

(2) I_w = source or sink

(3) These parameters are periodically sampled and are not 100% tested.



AC TEST CONDITIONS

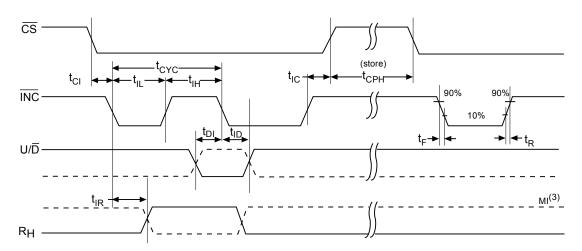
V _{CC} Range	$2.5 V \leq V_{CC} \leq 5.5 V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	0.5V _{CC}

AC OPERATING CHARACTERISTICS

 V_{CC} = +2.5V to +5.5V, V_{H} = $V_{\text{CC}},$ V_{L} = 0V, unless otherwise specified

Symbol	Parameter	Min	Typ(1)	Max	Units
t _{CI}	CS to INC Setup	100			ns
t _{DI}	U/\overline{D} to \overline{INC} Setup	50			ns
t _{ID}	U/\overline{D} to \overline{INC} Hold	100			ns
t _{IL}	INC LOW Period	250			ns
t _{IH}	INC HIGH Period	250			ns
t _{IC}	INC Inactive to CS Inactive	1			μs
t _{CPH}	CS Deselect Time (NO STORE)	100			ns
t _{CPH}	CS Deselect Time (STORE)	10			ms
t _{IR}	INC to R _H Change		1	5	μs
t _{CYC}	INC Cycle Time	1			μs
$t_{R}, t_{F}^{(2)}$	INC Input Rise and Fall Time			500	μs
t _{PU} ⁽²⁾	Power-up to Wiper Stable			1	ms
t _{WR}	Store Cycle		2	5	ms

A.C. TIMING



Notes:

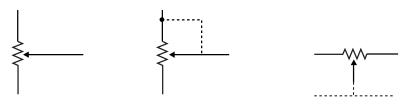
- (1) Typical values are for $T_A = 25^{\circ}C$ and nominal supply voltage.
- (2) This parameter is periodically sampled and not 100% tested.
- (3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

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APPLICATION INFORMATION

Potentiometer Configurations

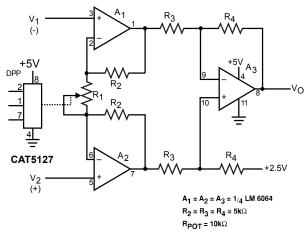


(a) resistive divider

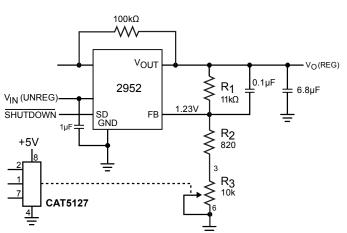
(b) variable resistance



Applications



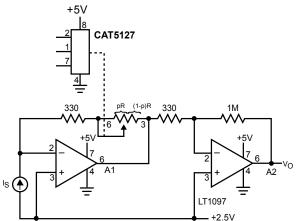
Programmable Instrumentation Amplifier



Programmable Voltage Regulator

+5V +5V 8 RA R 'pR_{POT} (1-p)R_{POT} 4 R_B 3 CAT5127 R 555 С 0.01µF 0.01µF 0.003µF

Programmable Sq. Wave Oscillator (555)

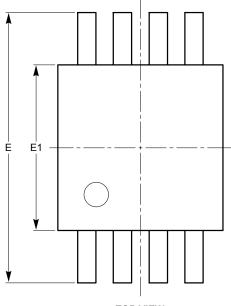


Programmable I to V convertor



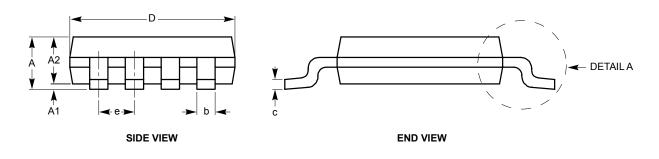
PACKAGE OUTLINE DRAWING

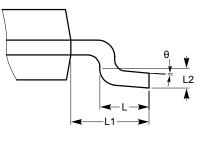
MSOP 8-Lead 3.0 x 3.0mm (Z)



TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
с	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
е		0.65 BSC	
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		6°





DETAIL A

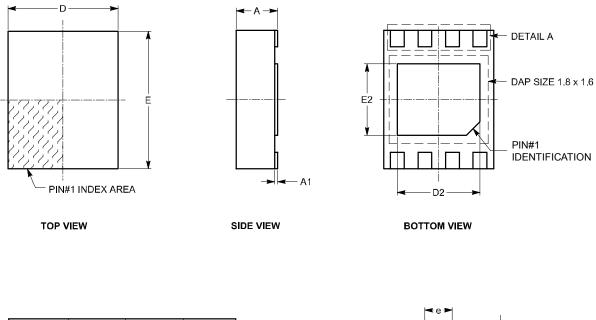
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

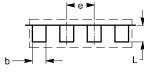
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC Specification MO-187.



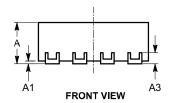
TDFN 8-Lead 2.5 x 2.0mm



SYMBOL	MIN	NOM	MAX
Α	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
E	2.40	2.50	2.60
E2	1.20	1.30	1.40
е		0.50 TYP	
L	0.20	0.30	0.40



DETAIL A



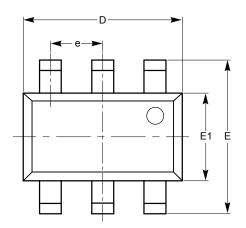
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC specification MO-229.

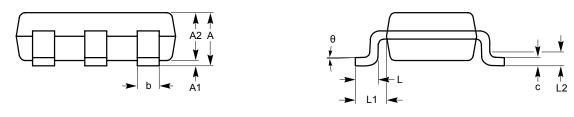


TSOT-23 6-Lead (TD)



TOP VIEW

SYMBOL	MIN	NOM	МАХ
А			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
с	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
е		0.95 TYP	
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
θ	0°		8°



SIDE VIEW



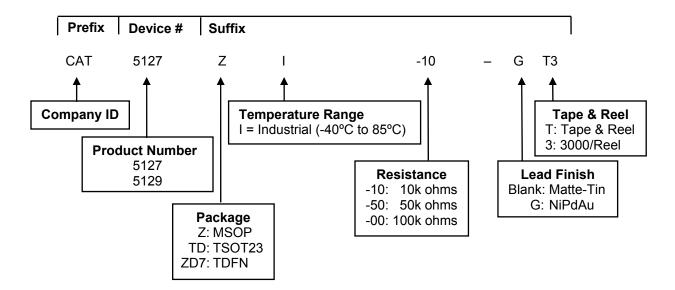
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC specification MO-193.



EXAMPLE OF ORDERING INFORMATION



ORDERING INFORMATION

Device	Ordering Part Number	Resistor [kΩ]	Top Marking	Pin/Package	Part Per Reel
CAT5127	CAT5127ZI-10-T3	10	ABPU	MSOP-8	3000
	CAT5127ZI-50-T3 ⁽⁵⁾	50	ABPV	MSOP-8	3000
	CAT5127ZI-00-T3 ⁽⁵⁾	100	ABPY	MSOP-8	3000
	CAT5127ZI-10-GT3	10	ABNA	MSOP-8	3000
	CAT5127ZI-50-GT3 ⁽⁵⁾	50	ABNB	MSOP-8	3000
	CAT5127ZI-00-GT3 ⁽⁵⁾	100	ABNK	MSOP-8	3000
	CAT5127ZD7I-10-GT3	10	HB	TDFN-8	3000
	CAT5127ZD7I-50-GT3 ⁽⁵⁾	50	HC	TDFN-8	3000
	CAT5127ZD7I-00-GT3 ⁽⁵⁾	100	HD	TDFN-8	3000
CAT5129	CAT5129TDI-10-T3	10	SWym ⁽⁶⁾	TSOT23-6	3000
	CAT5129TDI-50-T3 ⁽⁵⁾	50	SXym ⁽⁶⁾	TSOT23-6	3000
	CAT5129TDI-00-T3 ⁽⁵⁾	100	SYym ⁽⁶⁾	TSOT23-6	3000
	CAT5129TDI-10-GT3	10	SJym ⁽⁶⁾	TSOT23-6	3000
	CAT5129TDI-50-GT3 ⁽⁵⁾	50	SUym ⁽⁶⁾	TSOT23-6	3000
	CAT5129TDI-00-GT3 ⁽⁵⁾	100	SVym ⁽⁶⁾	TSOT23-6	3000

Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT5127ZI-10-GT3 (MSOP, Industrial Temperature range, 10kΩ, NiPdAu, Tape & Reel).
- (4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.
- (5) Contact factory for availability.
- (6) y = Production year (digit), m = Production month (digit).

REVISION HISTORY

Date	Rev.	Reason
12/18/06	Α	Initial Issue
02/23/07	В	Updated the Functional Diagram Updated the DC Electrical Characteristics table
08/03/07	С	Updated Package Outline Drawing Updated Ordering Information

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