MN3012

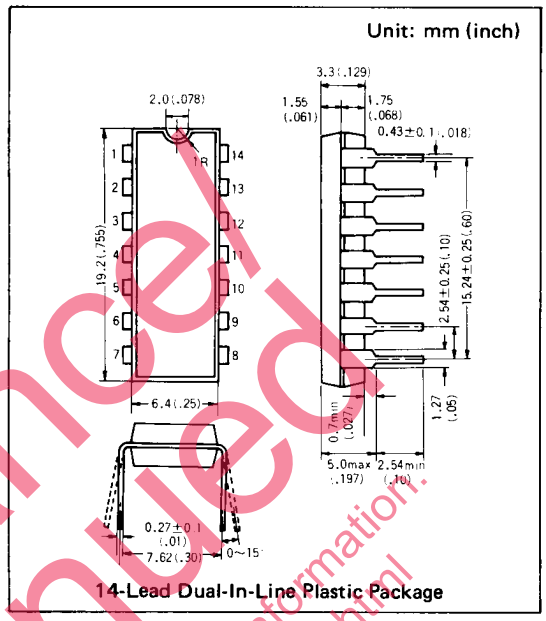
BBD with 3 outputs (190-STAGE, 5-STAGE, 3-STAGE)

■ General description

The MN3012 is a BBD comprised of 190,5 and 3-stages in parallel with 3 outputs incorporating a clock generator suitably designed for sound effect generator such as chorus, fading, vibrato and reverberation effects of audio equipments.

Clock generating frequency can be freely controlled by the value of external resistors and capacitors connected to CG_1, CG_2 and CG_3 terminals. Also delay time can be set by changing the clock frequency.

Output signal of differernt delay time can be obtained simultaneously from 3 output terminals (OUT1, OUT2, OUT3) against input sinal.



■ Features

- Single power supply (V_{DD} terminal): −8.5 ~ −16V.
- Dynamic range: S/N = 98dB typ.
- No insertion loss: L_i = 0dB typ.
- Low distortion: THD = 0.4% typ.
- Built-in clock genrator.
- Clock frequency range %: 10 ~ 200KHz.
- Built-in clock component cancellation circuit.
- P channel silicon gate process.
- 14-Lead Dual-In-Line Plastic Package.

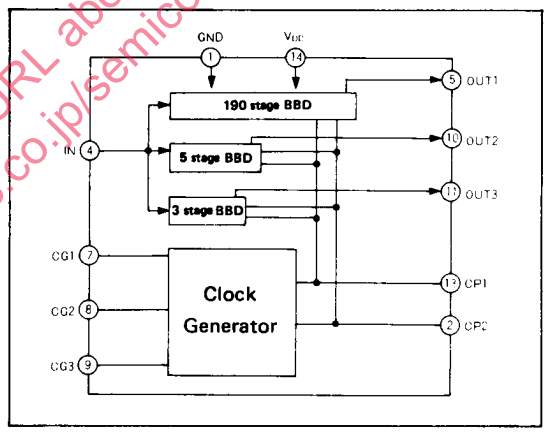
■ Applications

- Chorus, fading, vibrato and reverberation effects of audio equipments.
- Sound effect of electronic musical instruments.

■ Maximum Delay Time by Tap Output

Terminal of the Tap Output	OUT 1	OUT 2	OUT 3
Stages of BBD (Stage)	190	5	3
Maximum Delay Time (mS)	0.475 ~9.5	0.0125 ~0.25	0.0075 ~0.15

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Remarks
Terminal Voltage	V_{DD}	−18～+0.3	V	GND = 0V
Input Terminal Voltage	V_I	−18～+0.3	V	〃
Output Terminal Voltage	V_O, V_{CP}	−18～+0.3	V	〃
Operating Ambient Temperature	Topr	−20～+70	℃	
Storage Temperature	Tstg	−55～+125	℃	

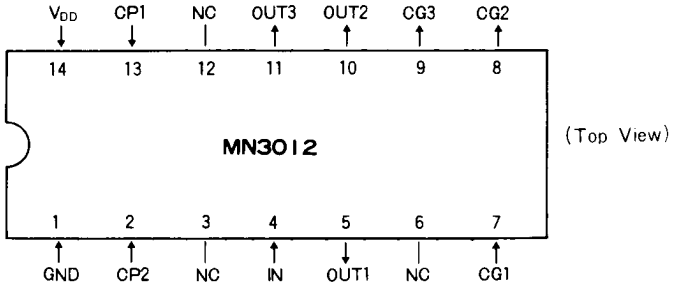
■ Operating Condition (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−8.5	−15	−16	V
Clock Voltage "H" Level	V_{CPH}		0		−0.4	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Frequency	f_{CP}		10		200	kHz
Clock Input Capacitance	C_{CP}				180	pF
Input DC Bias	V_{Bias}		−3		−12	V

■ Electrical Characteristics ($Ta = 25°C$, $V_{DD} = -15V$, $V_{CPL} = -15V$, $V_{CPH} = 0V$, $R_L = 56k\Omega$, $C = 100pF$, $R_2 = R_3 = 22k\Omega$, $R_4 = R_5$ 2.2kΩ, $f_{cp} = 1/2f_{OSC}$ (Adjusted by R1))

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time						
OUT 1 Terminal	t_{D1}	f_{CP}=10kHz～200kHz	0.475		9.5	ms
OUT 2 Terminal	t_{D2}		0.0125		0.25	ms
OUT 3 Terminal	t_{D3}		0.0075		0.15	ms
Input Signal Frequency						
OUT 1 Terminal	f_{i1}	f_{cp} = 40kHz Output −3dB	12			kHz
OUT 2 Terminal	f_{i2}		12			kHz
OUT 3 Terminal	f_{i3}		12			kHz
Input Signal Voltage	V_i	THD≦2.5%	1.2			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i=1 kHz	−4	0	4	dB
Total Harmonic Distortion	THD	V_i=0.775Vrms		0.4	2.5	%
Noise Voltage						
OUT 1 Terminal	V_{no1}	f_{cp} = 100kHz Weighted by "A" curve			0.14	mVrms
OUT 2 Terminal	V_{no2}				0.14	mVrms
OUT 3 Terminal	V_{no3}				0.14	mVrms
Signal to Noise Ratio						
OUT 1 Terminal	S/N_1	f_{cp} = 100kHz Weighted by "A" curve		90		dB
OUT 2 Terminal	S/N_2			97		dB
OUT 3 Terminal	S/N_3			98		dB

■ Terminal Assignments



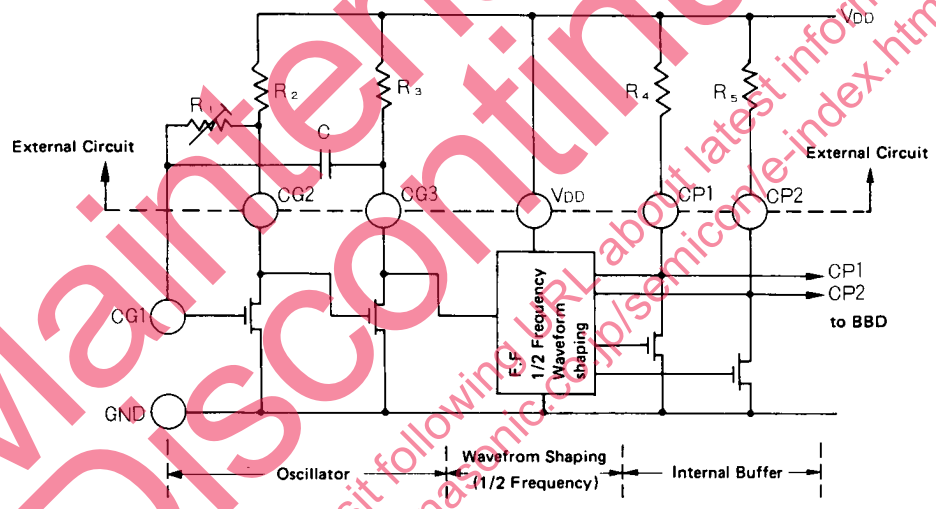
(Top View)

■ Terminal Description

Terminal No.	Symbol	Terminal name	Description
1	GND	Earth terminal	Connected to GND of the circuit.
2	CP2	Clock 2	Load resistor connection terminal of the driver that drives basic clock pulse to transfer electron of BBD.
4	IN	Signal input terminal	Analog signal to be delayed is input. Most suitable DC bias is applied to this terminal.
5	OUT 1	Output terminal 1	BBD output of 190 and 191 stages are composed and output is obtained by cancelling the clock components.
7	CG1	Clock osc. terminal 1	Input terminal for clock oscillator. Note) Refer to clock generating circuit.
8	CG2	Clock osc. terminal 2	
9	CG3	Clock osc. terminal 3	
10	OUT 2	Output terminal 2	Composed output of 5 and 6-stage BBD.
11	OUT 3	Output terminal 3	Composed output of 3 and 4-stage BBD.
13	CP1	Clock 1	Load resistor connection terminal of the driver to drive reverse clock pulse against CP 2.
14	V_{DD}	V_{DD} apply terminal	−15 volt is applied.

Note) No connection for the terminal No. 3, 6 and 12.

■ Clock Generator Circuit



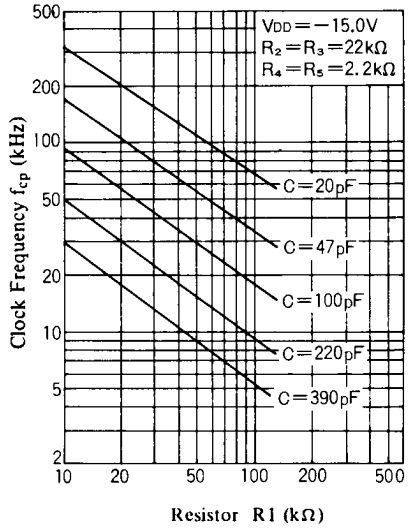
Note: when external clock is used, remove R_1 and C_1, and apply clock input to CGI.

$R_2 = R_3 = 22k\Omega$

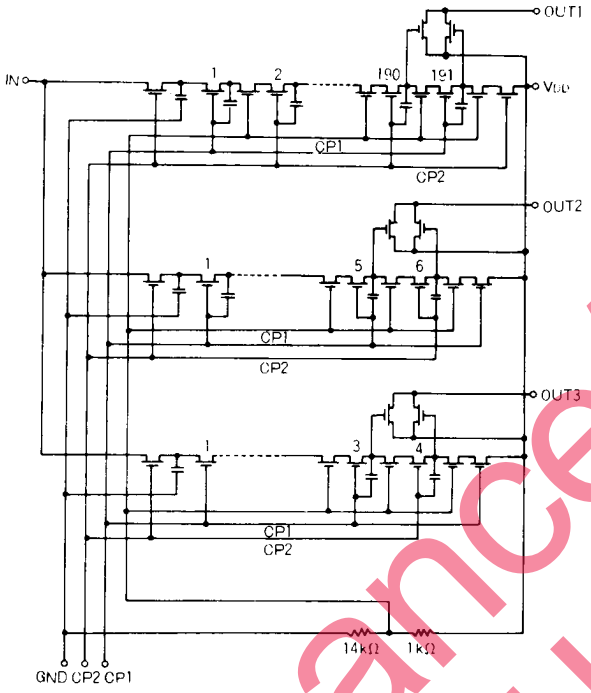
$R_4 = R_5 = 2.2k\Omega$

Adjusted by C, R1. $f_{cp} = 1/2\ f_{osc}$
Self-oscillation example should be refered to attached figure.

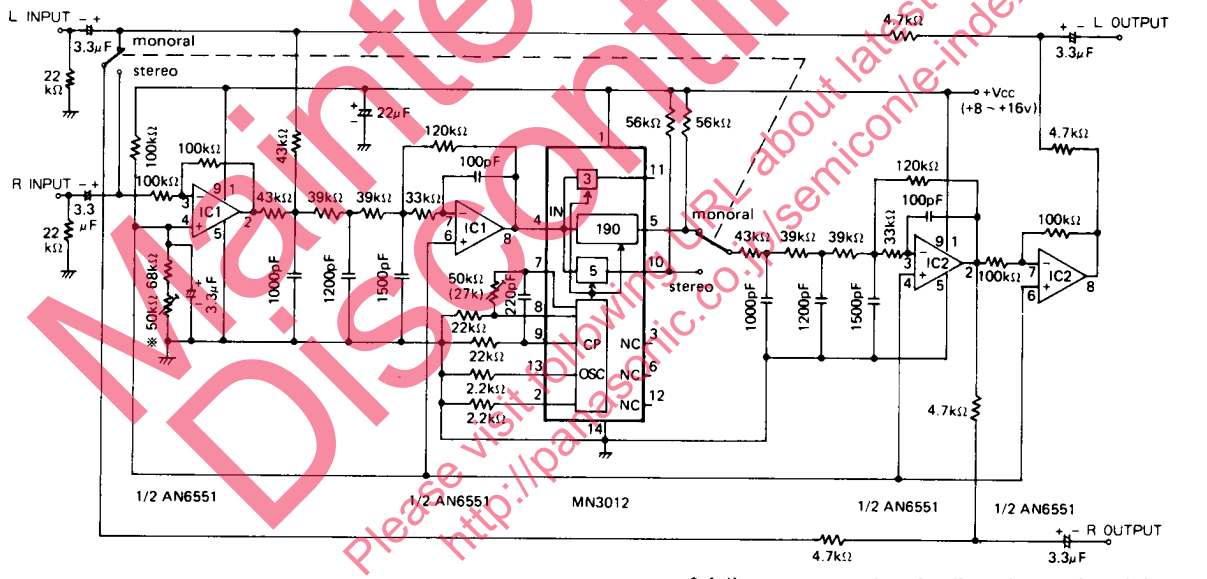
Attached Figure Example of Self-Oscillation



■ B B D Circuit Diagram



■ Example of application circuit



* Adjust so as to reduce its distortion to the minimum.

Sound field magnifying effect generating circuit (Stereo input)

Sound field magnifying effect generating circuit

Isn't it really wonderful if the speaker reproduction of sound for a grand hall can be got in the listening room or the car? Application of the sound image control technology and the delay characteristic of the BBD makes it possible to realize the above effect easily.

In listening through a speaker in the soom, the listener feels the distance and direction up to the speaker. As to the directional sense, for instance, there occurs some difference in the time for both direct and indirect sounds to reach his left and right ears depending on the position of the sound source, as well as the difference in the sound level, and from these differences the listener feels the "direction of sound". Further he feels the "distance of sound" from the energy ratio of the direct sound to the indirect sound (reverberation sound). The circuit for generating a sound field magnifying effect reproduces electronically the delicate time lag of these sounds, thereby makes it possible for the listener to feel as if he hears sounds from his surroundings other than the position of the speaker, and thus producing such effect that he is listening sounds in a large hall. Also the fatigue from listening for a long time through a conventional headphone is eliminated, and the effect similar to that of listening through an ordinary speaker is obtained.

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