International
IOR Rectifier

Not recommended for new design
Please refer to IRS20957

Data Sheet No. PD60303

IRS20955(S)PbF

PROTECTED DIGITAL AUDIO DRIVER

Features

- Floating PWM input enables easy half-bridge implementation
- Programmable bidirectional over-current protection with self-reset function
- Programmable preset deadtime for improved THD performances
- High noise immunity
- ±100 V ratings deliver up to 500 W in output power
- 3.3 V/5 V logic compatible input
- Operates up to 800 kHz
- RoHS compliant

Product Summary

V_{OFFSET} (max)		± 100 V
Gate driver	I_{o+}	1.0 A
	I_{o-}	1.2 A
Selectable deadtime		15 ns, 25 ns, 35 ns, 45ns
Propagation delay		90 ns
OC protection delay		500 ns (max)
Shutdown propagation delay		250 ns (max)

Description

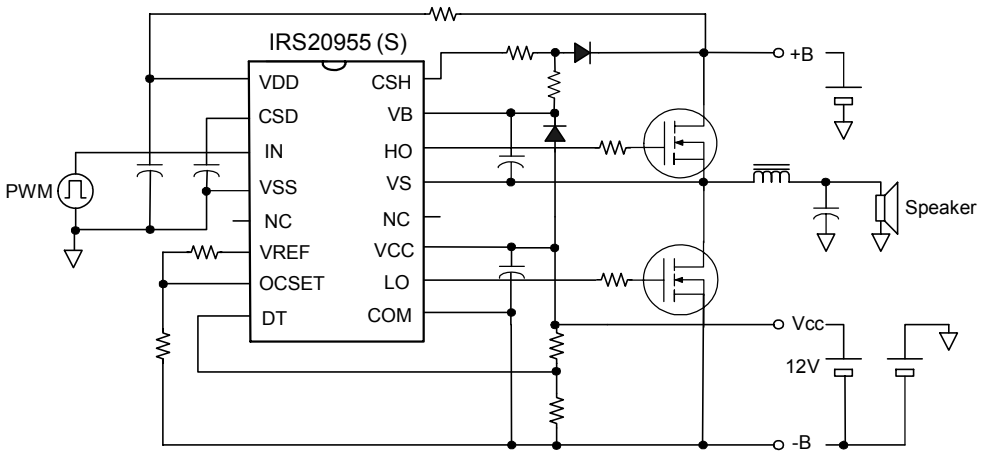
The IRS20955 is a high voltage, high speed MOSFET driver with a floating PWM input designed for Class D audio amplifier applications.

Bi-directional current sensing detects over-current conditions during positive and negative load currents without any external shunt resistors. A built-in protection control block provides a secure protection sequence against over-current conditions and a programmable reset timer.

The internal deadtime generation block enables accurate gate switching and optimum deadtime setting for better audio performance, such as lower THD and lower audio noise floor.

Package

Typical Connection



(Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only)

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply voltage	-0.3	220	V
V_S	High-side floating supply voltage (Note1)	V_B-20	V_B+0.3	
V_{HO}	High-side floating output voltage	Vs-0.3	V_B+0.3	
V_{CSH}	CSH pin input voltage	Vs-0.3	V_B+0.3	
V_{CC}	Low-side fixed supply voltage (Note1)	-0.3	20	
V_{LO}	Low-side output voltage	-0.3	V_{CC} +0.3	
V_{DD}	Floating input supply voltage	-0.3	210	
V_{SS}	Floating input supply voltage (Note1)	(See I_{DDZ})	V_{DD}+0.3	
V_{IN}	PWM input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC} +0.3	
V_{REF}	VREF pin voltage	-0.3	V_{CC} +0.3	
I_{DDZ}	Floating input supply Zener clamp current (Note1)	-	10	mA
I_{CCZ}	Low side supply Zener clamp current (Note1)	-	10	
I_{BSZ}	Floating supply Zener clamp current (Note1)	-	10	
I_{OREF}	Reference output current	-	5	
d V_S /dt	Allowable V_S voltage slew rate	-	50	V/ns
d V_{SS} /dt	Allowable V_{SS} voltage slew rate (Note2)	-	50	
d V_{SS} /dt	Allowable V_{SS} voltage slew rate upon power-up (Note3)	-	50	V/ms
P_D	Maximum power dissipation	-	1.0	W
$R_{th,JA}$	Thermal resistance, junction to ambient	-	115	°C/W
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

Note1: $\mathbf{V_{DD}}$ - $\mathbf{V_{SS}}$, $\mathbf{V_{CC}}$ -COM and $\mathbf{V_B}$ - $\mathbf{V_S}$ contain internal shunt Zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.
Note2: For the rising and falling edges of step signal of 10 V. V_{ss}=15 V to 200 V.
Note3: V_{ss} ramps up from 0 V to 200 V.

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Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. All voltage parameters are absolute voltages referenced to COM. The V_S and COM offset ratings are tested with supplies biased at I_{DD}=5 mA, V_{CC}=12 V and V_B-V_S=12 V.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S+10	V_S+18	V
V_S	High-side floating supply offset voltage	Note 1	100	
I_{DDZ}	Floating input supply zener clamp current	1	5	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High-side floating output voltage	Vs	V_B	
V_{CC}	Low-side fixed supply voltage	10	18	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	PWM input voltage	V_{SS}	V_{DD}	
V_{CSD}	CSD pin input voltage			
V_{DT}	DT pin input voltage	0	V_{CC}	
I_{OREF}	Reference output current to COM (Note 2)	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
T_A	Ambient temperature	-40	125	°C
I_{PW}	Input pulse width	10 (note 3)	-	ns

Note 1: Logic operational for V_S equal to –5 V to +200 V. Logic state held for V_S equal to –5 V to –V_{BS}.
Note 2: Nominal voltage for V_{REF} is 5 V. I_{OREF} of 0.3 mA – 0.8 mA dictates total external resistor value on V_{REF} to be 6.3 kΩ to 16.7 kΩ.
Note 3: Output logic status may not respond correctly if input pulse width is smaller than the minimum pulse width

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Electrical Characteristics

V_{CC} ,V_{BS}= 12 V, I_{DD}=5 mA, V_{SS}=20 V, V_S=0 V,C_L=1 nF and T_A=25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low-Side Supply						
UV_{CC+}	V_{CC} supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	V_{CC} supply UVLO negative threshold	8.2	8.7	9.2		
I_{QCC}	Low-side quiescent current	-	-	3	mA	$V_{DT} = V_{CC}$
V_{CLAMPL}	Low-side Zener diode clamp voltage	19.6	20.4	21.6	V	I_{CC}=5 mA
High-Side Floating Supply						
UV_{BS+}	High-side well UVLO positive threshold	8.0	8.5	9.0	V	
UV_{BS-}	High-side well UVLO negative threshold	7.8	8.3	8.8		
I_{QBS}	High-side quiescent current	-	-	1	mA	
I_{LKH}	High-side to low-side leakage current	-	-	50	µA	V_B=V_S =200 V
V_{CLAMPH}	High-side Zener diode clamp voltage	19.6	20.4	21.6	V	I_{BS}=5 mA
Floating Input Supply						
UV_{DD+}	V_{DD}, V_{SS} floating supply UVLO positive threshold	8.2	8.7	9.2	V	V_{SS} =0 V
UV_{DD-}	V_{DD}, V_{SS} floating supply UVLO negative threshold	7.7	8.2	8.7		V_{SS} =0 V
I_{QDD}	Floating input quiescent current	-	-	1	mA	V_{DD}=9.5 V +V_{SS}
V_{CLAMPM}	Floating input Zener diode clamp voltage	9.8	10.2	10.8	V	I_{DD}=5 mA
I_{LKM}	Floating input side to low-side leakage current	-	-	50	µA	V_{DD}=V_{SS} =200 V
Floating PWM Input						
V_{IH}	Logic high input threshold voltage	2.3	1.9	-	V	
V_{IL}	Logic low input threshold voltage	-	1.9	1.5		
I_{IN+}	Logic “1” input bias current	-	-	40	µA	V_{IN} =3.3 V
I_{IN-}	Logic “0” input bias current	-	-	1		V_{IN} = V_{SS}
Protection						
V_{REF}	Reference output voltage	4.8	5.1	5.4	V	I_{OREF} =0.5 mA
$V_{th,OCL}$	Low-side OC threshold in V_S	1.1	1.2	1.3		OCSET=1.2 V, Fig. 3
$V_{th,OCH}$	High-side OC threshold in V_{CSH}	1.1+ V_S	1.2+ V_S	1.3+ V_S		V_S=200 V, Fig. 4
$V_{th,1}$	CSD pin shutdown release threshold	0.62 x V_{DD}	0.70 x V_{DD}	0.78 x V_{DD}		V_{SS} =0 V
$V_{th,2}$	CSD pin self reset threshold	0.26 x V_{DD}	0.30 x V_{DD}	0.34 x V_{DD}		
I_{CSD+}	CSD pin discharge current	70	100	130	µA	V_{SD} = V_{SS} +5 V
I_{CSD-}	CSD pin charge current	70	100	130		
t_{SD}	Shutdown propagation delay from V_{CSD} > V_{SS} + $V_{th,OCH}$ to shutdown	-	-	250	ns	Fig. 2
t_{OCH}	Propagation delay time from V_{CSH} > $V_{th,OCH}$ to shutdown	-	-	500		Fig. 4
t_{OCL}	Propagation delay time from V_S> $V_{th,OCL}$ to shutdown	-	-	500		Fig. 3
Gate Driver						
I_{o+}	Output high short circuit current (source)	-	1.0	-	A	V_O =0 V, PW≤10 µs
I_{o-}	Output low short circuit current (sink)	-	1.2	-		V_O =12 V, PW≤10 µs
V_{OL}	Low level output voltage LO – COM, HO – VS	-	-	0.1	V	

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Electrical Characteristics (cont.)

V_{CC} ,V_{BS}= 12 V, I_{DD}=5 mA, V_{SS}=20 V, V_S=0 V,C_L=1 nF and T_A=25 °C unless otherwise specified.

V_{OH}	High level output voltage VCC – LO, VB – HO	-	-	1.4	V	I_O=0 A
t_r	Turn-on rise time	-	15	-	ns	
t_f	Turn-off fall time	-	10	-		
$t_{on,1}$	High-side and low-side turn-on propagation delay, floating inputs	-	105	-		V_{DT} = V_{CC}, V_S = 100 V, V_{SS} = 100 V
$t_{off,1}$	High-side and low-side turn-off propagation delay, floating inputs	-	90	-		
$t_{on,2}$	High-side and low-side turn-on propagation delay, non-floating inputs	-	105	-		V_{DT} = V_{CC}, V_S = 100V, V_{SS} = COM
$t_{off,2}$	High-side and low-side turn-off propagation delay, non-floating inputs	-	90	-		
DT1	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	8	15	22		V_{DT}>V_{DT1}, V_{SS} = COM
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	15	25	35		V_{DT1}>V_{DT}> V_{DT2}, V_{SS} = COM
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	20	35	50		V_{DT2}>V_{DT}> V_{DT3}, V_{SS} = COM
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})V_{DT}= V_{DT4}	25	45	60		V_{DT3}>V_{DT}, V_{SS} = COM
V_{DT1}	DT mode select threshold 1	0.51(V_{cc})	0.57(V_{cc})	0.63(V_{cc})	V	
V_{DT2}	DT mode select threshold 2	0.32(V_{cc})	0.36(V_{cc})	0.40(V_{cc})		
V_{DT3}	DT mode select threshold 3	0.21(V_{cc})	0.23(V_{cc})	0.25(V_{cc})		

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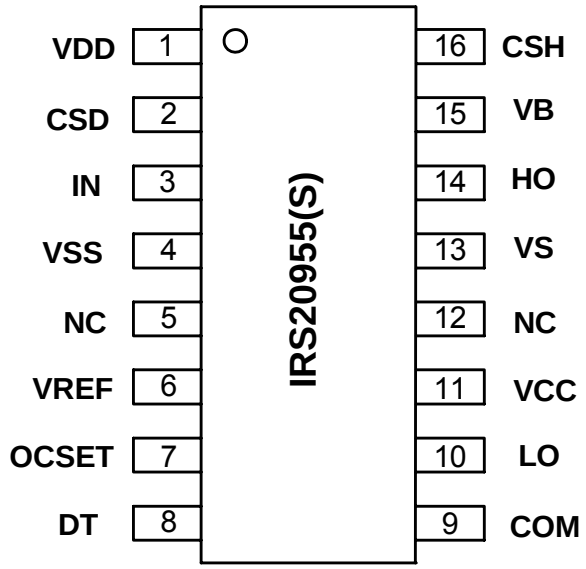
Lead Definitions

Pin #	Symbol	Description
1	VDD	Floating input positive supply
2	CSD	Shutdown timing capacitor, referenced to VSS
3	IN	PWM non-inverting input, in phase with HO
4	VSS	Floating input supply return
5	NC	
6	VREF	5 V reference output for setting OCSET
7	OCSET	Low-side over-current threshold setting, referenced to COM
8	DT	Input for programmable deadtime, referenced to COM
9	COM	Low-side supply return
10	LO	Low-side output
11	VCC	Low-side logic supply
12	NC	
13	VS	High-side floating supply return
14	HO	High-side output
15	VB	High-side floating supply
16	CSH	High-side over-current sensing input, referenced to VS



IRS20955(S)

16-Lead SOIC (narrow body)

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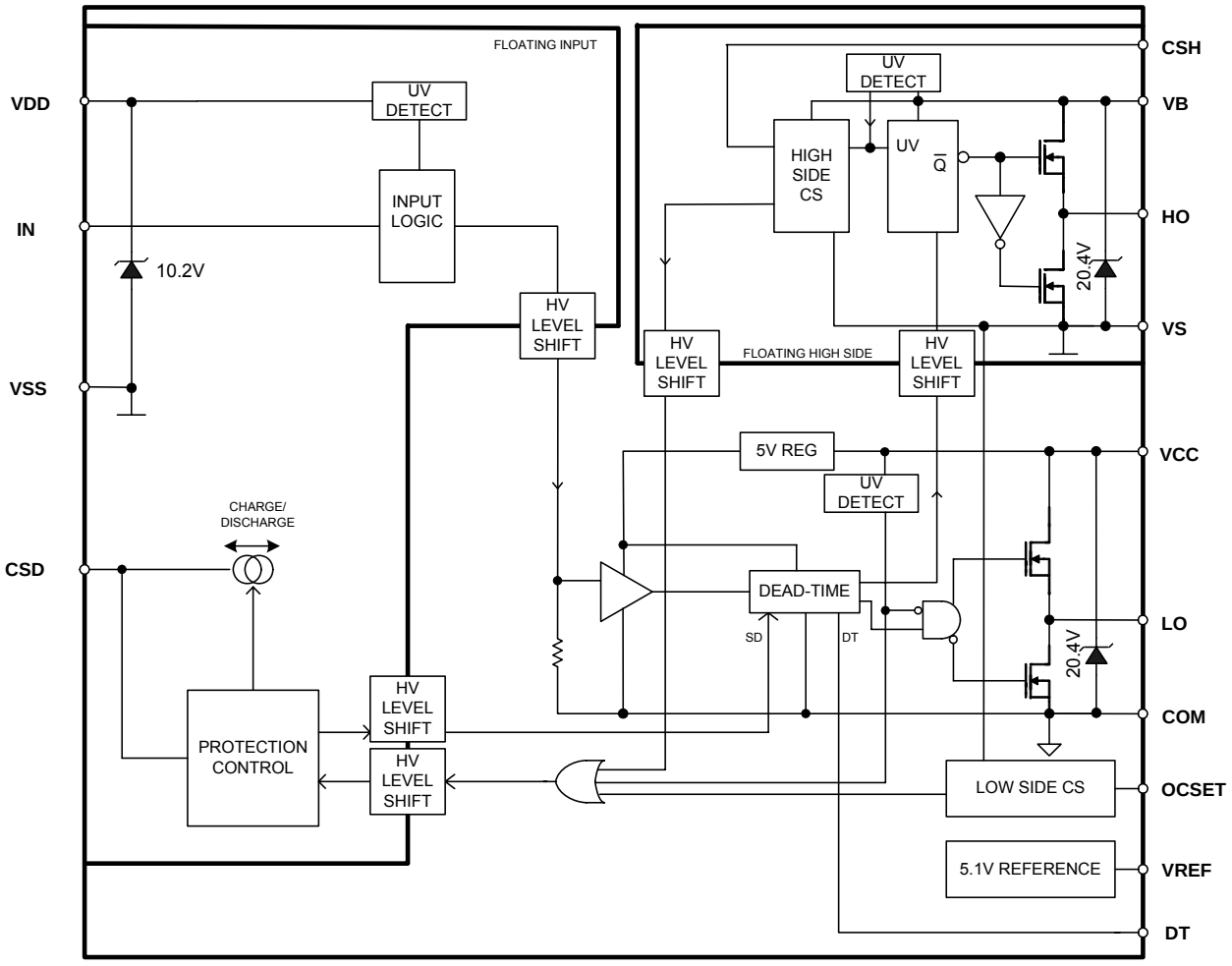
Block Diagram



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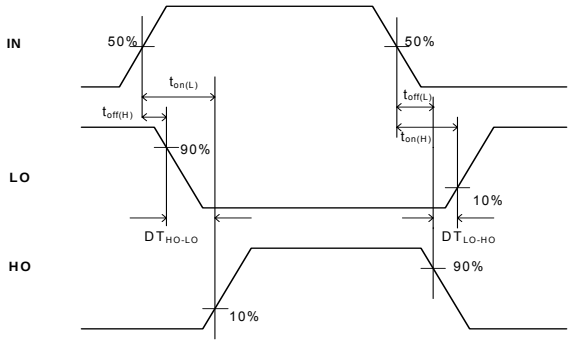

Figure 1. Switching Time Waveform Definitions

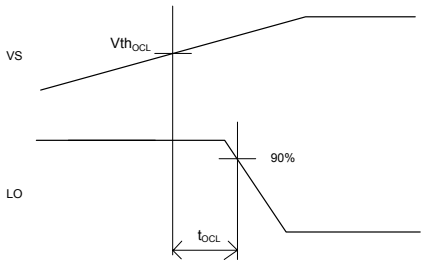

Figure 3. V_S > $V_{TH,OCL}$ to Shutdown Waveform

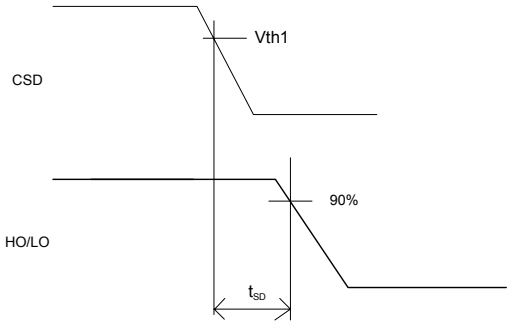

Figure 2. CSD to Shutdown Waveform Definitions

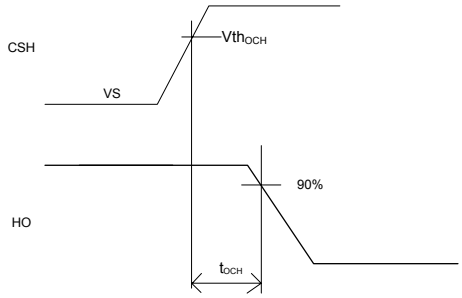

Figure 4. V_{CSH} > $V_{th,\,OCH}$ to Shutdown Waveform

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Functional Description

Floating PWM Input

The IRS20955S accepts floating inputs, enabling easy half-bridge implementation. V_{DD}, CSD and IN refer to V_{SS}. As a result, the PWM input signal can directly feed into IN while referencing V_{SS}, which is typically the midpoint between the positive and negative DC bus voltages in a half-bridge configuration.
The IRS20955S also accepts a non-floating input when V_{SS} is tied to COM.

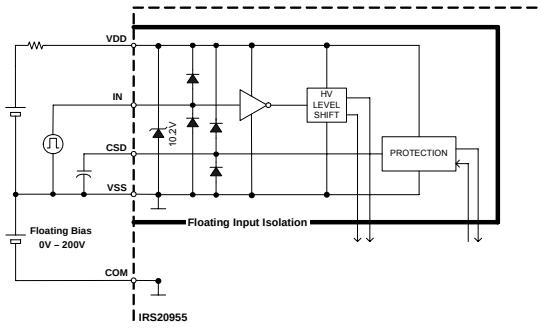

Figure 5. Floating PWM Input Structure

Over-Current Protection (OCP)

The IRS20955S features over-current protection to protect the power MOSFETs during abnormal load conditions. The IRS20955S engages a sequence of events when it detects the over-current condition during high-side or low-side turn on.
As soon as either the high-side or low-side current sensing block detects over-current:

1. The OC Latch (OCL) flips logic states and shutdowns the outputs LO and HO.
2. The CSD pin starts discharging the external capacitor C_t.
3. When V_{CSD}, the voltage across C_t, falls below the lower threshold V_{th2}, an output signal from COMP2 resets OCL.
4. The CSD pin starts charging the external capacitor C_t.
5. When V_{CSD} goes above the upper threshold V_{th1}, the logic on COMP1 flips and the IC resumes operation.

As long as the over-current condition exists, the IC will repeat the over-current protection sequence.

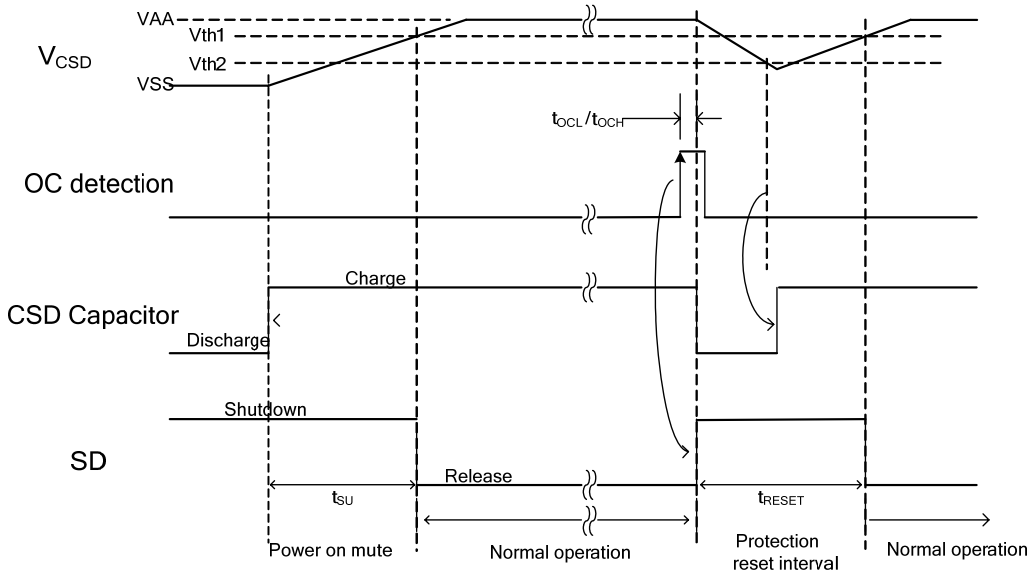

Figure 6. Over-Current Protection Timing Chart

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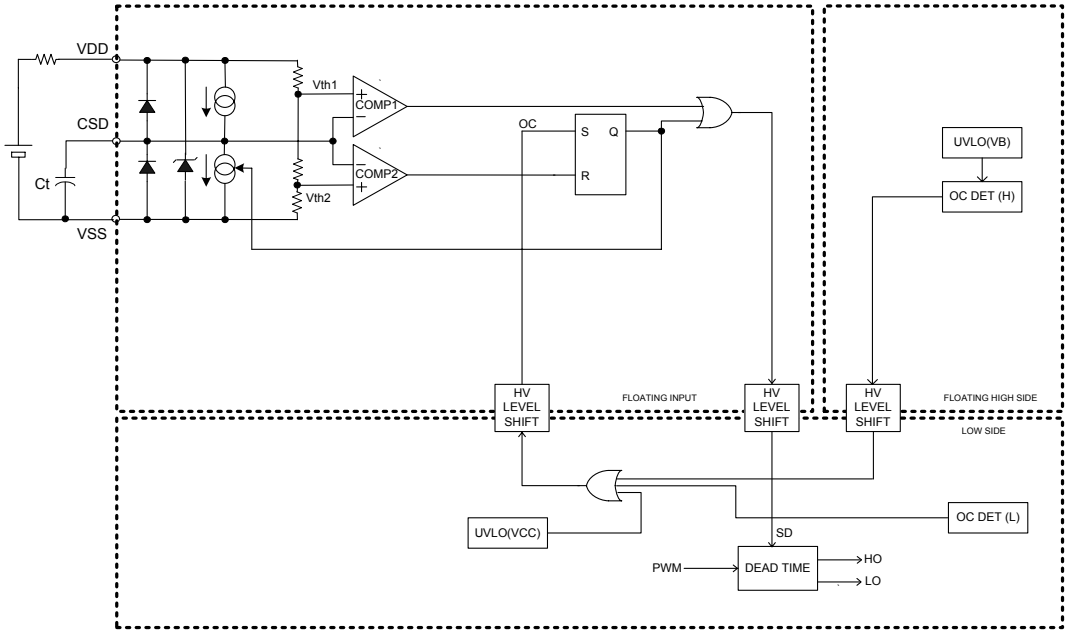

Figure 7. Shutdown Functional Block Diagram

Protection Control

The internal protection control block dictates the operational mode-normal, or shutdown, using the input of the CSD pin. The IC functions as expected in the normal mode. In shutdown mode, the IC forces LO and HO to output 0 V with respect to COM and VS to turn off the power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

Self Reset Protection

By putting a capacitor between CSD and VSS, the IRS20955S can reset itself after entering shutdown mode.

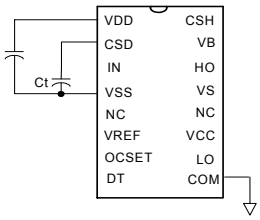

Figure 8. Self Reset Protection Configuration

Designing C_t

The timing capacitor, C_t, is used to program t_{RESET} and t_{SU}.

- t_{RESET}, is the amount of time that elapses from when the IC enters shutdown mode to the time when the IC resumes operation. t_{RESET} should be long enough to avoid over heating the MOSFET from the repetitive sequence of shutting down and resuming operation during over-current conditions. In most of applications, the minimum recommended time for t_{RESET} is 0.1.
- t_{SU} is the amount of time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation.

The values chosen for t_{RESET} and t_{SU} will determine the capacitance of C_t using the given equations:

$$C_t = \frac{t_{RESET} \cdot I_{CSD}}{1.1 \cdot V_{DD}} \quad [F]$$

$$C_t = \frac{t_{SU} \cdot I_{CSD}}{0.7 \cdot V_{DD}} \quad [F]$$

where I_{CSD} = the charge/discharge current at the CSD pin
V_{DD} = the supply voltage with respect to V_{SS}.

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Shutdown Input

When V_{CSD} falls below V_{th2}, the IRS20955S begins to charge C_t in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, V_{th1}, the IC begins to operate normally again.

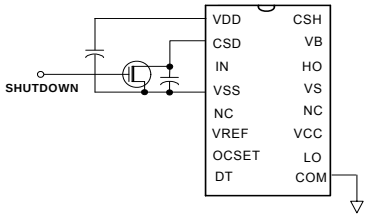

Figure 9. Shutdown Input

Latched Protection

Connecting CSD to V_{DD} through a 10 kΩ or less resistor configures the over-current protection latch. The latch locks the IC in shutdown mode after over-current is detected. An external reset switch can be used to bring CSD below the lower threshold V_{th2} for a minimum of 200 ns to properly reset the latch. After the power up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

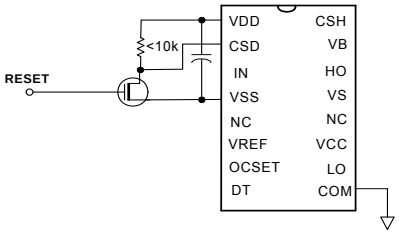

Figure 10. Latched Protection Configuration

Interfacing with System Controller

The IRS20955S can communicate with an external system controller through a simple interfacing circuit such as the one shown in Figure 11. A generic PNP transistor, shown as U1, can detect the sink current at the CSD pin during an OCP event and output a shutdown signal to an external system controller. Another generic NPN transistor, shown as U2, can then reset the internal protection logic by pulling the CSD voltage below V_{th2} for a minimum of 200 ns. Note that the CSD pin is configured to operate in latched OCP. After the power up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

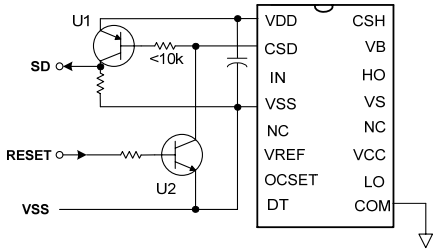

Figure 11. Interfacing with System Controller

Programming OCP Trip Level

In a Class D audio amplifier, the direction of the load current alternates with the audio input signal. An over-current condition can therefore occur during either a positive current cycle or a negative current cycle. The IRS20955 uses the $R_{DS(ON)}$ of the output MOSFETs as current sensing resistors. Due to the structural constraints of high voltage ICs, current sensing is implemented differently for high side and low side. If the measured current exceeds a predetermined threshold, the OCP block outputs a signal to the protection block to shutdown the MOSFET to protect the switching devices.

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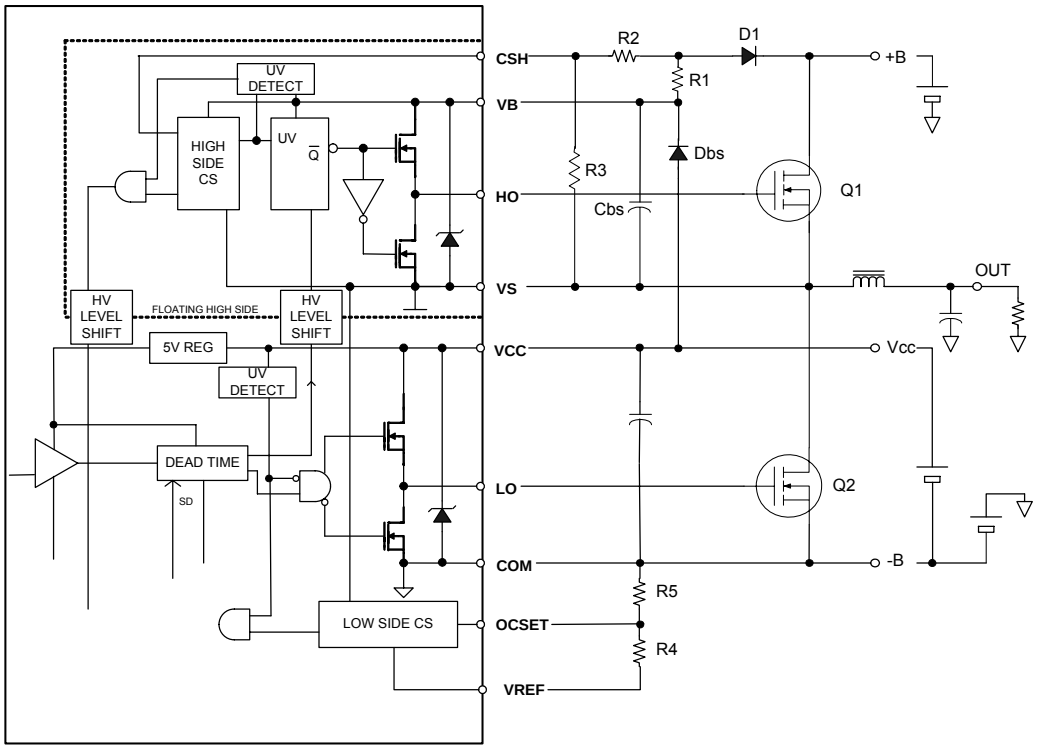

Figure 12. Bi-Directional Over-Current Protection

Low-side Over-Current Sensing

For negative load currents, low-side over-current sensing monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level.

Low-side current sensing is based on the measurement of V_{DS} across the low side MOFET during low-side turn on. In order to avoid triggering OCP from overshoot, a blanking interval inserted after LO turn on disables over-current detection for 450 ns.

The OCSET pin is used to program the threshold for low-side over-current sensing. When the V_{DS} measured across the low-side MOSFET exceeds the voltage at the OCSET pin with respect COM, the IRS20955S begins the OCP sequence described earlier.

Since the voltage from V_S to COM is compared to the voltage at the OCSET pin, the voltage at OCSET determines the trip level for over-current detection. By selecting the trip level for over-current, the voltage at OCSET can be calculated using the equation below.

$$V_{OCSET} = V_{DS(LOW\ SIDE)} = I_{TRIP+} \times R_{DS(ON)}$$

In order to minimize the effect of the input bias current at the OCSET pin, select resistor values for R4 and R5 such that the current through the voltage divider is 0.5 mA or more.

* Note: Using V_{REF} to generate an input to OCSET through a resistive divider provides improved immunity from fluctuations in V_{CC}.

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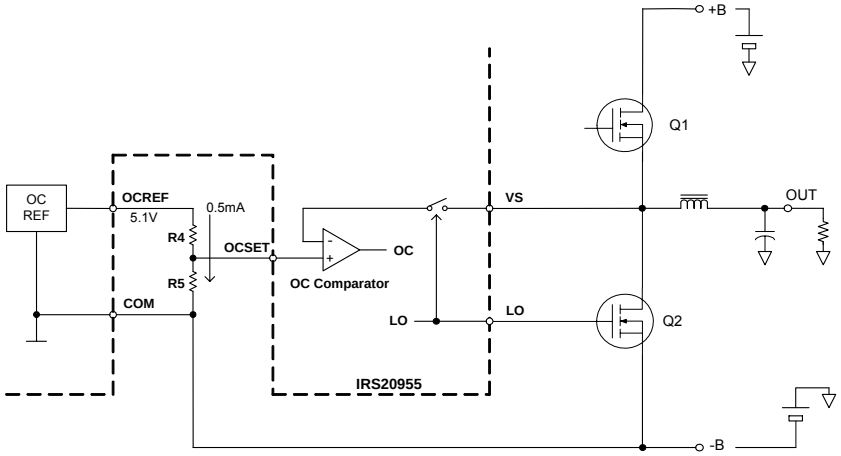

Figure 13. Low-Side Over-Current Sensing

Low-Side Over-Current Setting

Let the low-side MOSFET have an $R_{DS(ON)}$ of 100 mΩ and set the current trip level to 30 A. V_{OCSET} is given by:

$V_{OCSET} = I_{TRIP+} \times R_{DS(ON)} = 30\ A \times 100\ m\Omega = 3.0\ V$

Choose R4+R5=10 kΩ to properly load the VREF pin.

$$R_S = \frac{V_{OCSET}}{V_{REF}} \cdot 10\,k\Omega$$
$$= \frac{3.0\,V}{5.1\,V} \cdot 10\ k\Omega$$
$$= 5.8\ k\Omega$$

where $V_{REF} = 5.1\ V$

Based on the E-12 series of resistor values, choose R5 to be 5.6 kΩ and R4 to be 3.9 kΩ to complete the design.

In general, $R_{DS(ON)}$ has a positive temperature coefficient that needs to be considered when setting the threshold level. Variations in $R_{DS(ON)}$ will affect the selection of external or internal component values.

High-Side Over-Current Sensing

For positive load currents, high-side over-current sensing also monitors the load condition and shuts down the switching operation if the load current exceeds the preset trip level.

High-side current sensing is based on the measurement of V_{DS} across the high-side MOFET during high-side turn on through pins CSH and VS. In order to avoid triggering OCP from overshoot, a blanking interval inserted after HO turn on disables over-current detection for 450 ns.

In contrast to low-side current sensing, the threshold at which the CSH pin engages OC protection is internally fixed at 1.2 V. An external resistive divider R2 and R3 can be used to program a higher threshold.

An external reverse blocking diode, D1, is required to block high voltages from feeding into the CSH pin while the high-side is off. Due to a forward voltage drop of 0.6 V across D1, the minimum threshold required for high-side over-current protection is 0.6 V.

$$V_{CSH} = \frac{R3}{R2+R3} \cdot \left(V_{DS(HIGHSIDE)} + V_{F(D1)}\right)$$

where $V_{DS(HIGH\ SIDE)}$ = the drain to source voltage of the high-side MOSFET during high-side turn on
$V_{F(D1)}$ = the forward drop voltage of D1

Since $V_{DS(HIGH\ SIDE)}$ is determined by the product of drain current I_D and $R_{DS(ON)}$ of the high-side MOSFET. V_{CSH} can be rewritten as:

$$V_{CSH} = \frac{R3}{R2+R3} \cdot \left(R_{DS(ON)} \cdot I_D + V_{F(D1)}\right)$$

Note: The reverse blocking diode D1 is forward biased by a 10 kΩ resistor R1 when the high-side MOSFET is on.

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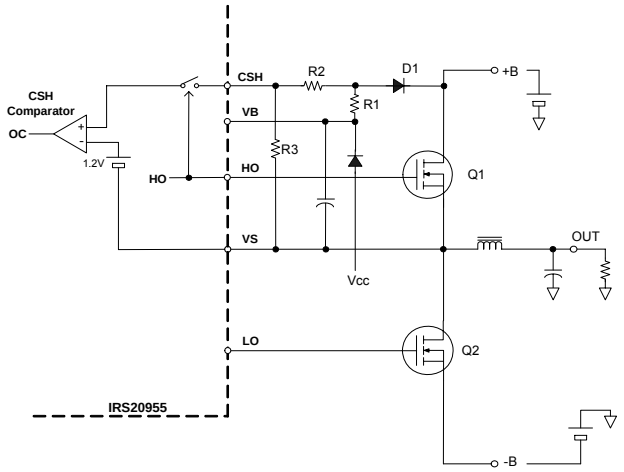

Figure 14. Programming High-Side Over-Current Threshold

High-Side Over-Current Setting

Figure 14 demonstrates the typical circuitry used for high-side current sensing. In the following example, the over-current protection level is set to trip at 30 A using a MOSFET with an $R_{DS(ON)}$ of 100 mΩ. The component values of R2 and R3 can be calculated using the following formula:

Let R2 + R3=10 kΩ.

$$R_3 = 10\ k\Omega \cdot \frac{Vth_{OCH}}{V_{DS} + V_F}$$

where $V_{th,OCL}$ = 1.2 V

V_F = the forward voltage of reverse blocking diode D1 = 0.6 V.

$V_{DS@ID=30A}$ = the voltage drop across the high-side MOSFET when the MOSFET current is 30 A.

Therefore, $V_{DS@ID=30A} = I_D \times R_{DS(ON)}$ = 30 A x 100 mΩ = 3 V

Based on the formulas above, R2 = 6.8 kΩ and R3 = 3.3 kΩ.

Choosing the Right Reverse Blocking Diode

The selection of the appropriate reverse blocking diode used in place of D1 depends on its voltage rating and speed. To effectively block bus voltages, the reverse voltage must be higher than the voltage difference between +B and -B and the reverse recovery time must be as fast as the boot strap charging diode. A diode such as the Philips BAV21 W, a 200 V, 50 ns high speed switching diode, is more than sufficient.

Deadtime Generator

Deadtime is a blanking period inserted between high-side turn on and low-side turn on to prevent shoot through. In the IRS20955S, an internal dead-time generation block allows the user to select the optimum deadtime from a range of preset values. Selecting a preset deadtime through the DT/SD pin voltage can easily be done through an external voltage divider. This way of setting deadtime prevents outside noise from modulating the switching timing, which is critical to the audio performances.

How to Determine Optimal Deadtime

The effective deadtime in an actual application differs from the deadtime specified in this datasheet due to the switching fall time, t_f.. The deadtime value in this datasheet is defined as the time period between the beginning of turn-off on one side of the switching stage and the beginning of turn-on on the other side as shown in Figure 15. The fall time of MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective deadtime of a Class D audio amplifier.

(Effective deadtime) = (Deadtime in datasheet) – t_f.

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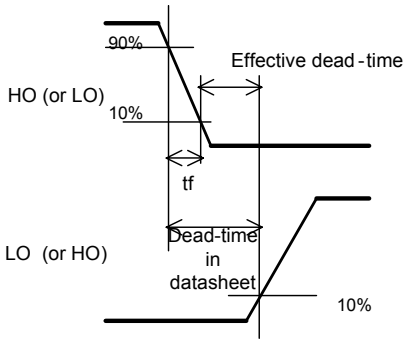

Figure 15. Effective Deadtime

A longer deadtime period is required for a MOSFET with a larger gate charge value because of the longer t_f.. Although a shorter effective deadtime setting is beneficial to achieving better linearity in Class D amplifiers, the likelihood of shoot-through current increases with narrower deadtime settings. Negative values of effective deadtime may cause excessive heat dissipation in the MOSFETs, leading to potentially serious damage.

To calculate the optimal deadtime in a given application, the fall time t_f for both HO and LO in the actual circuit need to be taken into account. In addition, variations in temperature and device parameters could also affect the effective deadtime in the actual circuit. Therefore, a minimum effective deadtime of 10 ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

Programming Deadtime

The IRS20955S selects the deadtime from a range of preset deadtime values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined dead-time by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using $V_{CC.}$ The relationship between the operation mode and the voltage at DT pin is illustrated in the Figure16 below.

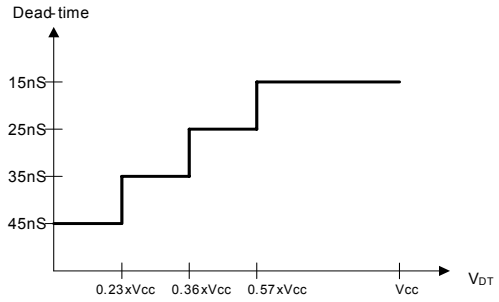

Figure 16. Deadtime vs. V_{DT}

Table 1 suggests pairs of resistor values used in the voltage divider for selecting deadtime. Resistors with up to 5% tolerance are acceptable when using these values.

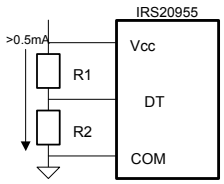

Figure 17. External Voltage Divider

Table 1 Recommended Resistor Values for Deadtime Selection

Deadtime Mode	R1	R2	DT/SD Voltage
DT1	<10 kΩ	Open	V_{CC}
DT2	5.6 kΩ	4.7 kΩ	0.46(V_{CC})
DT3	8.2 kΩ	3.3 kΩ	0.29(V_{CC})
DT4	Open	<10 kΩ	COM

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Supplying V_{DD}

V_{DD} is designed to be supplied with an internal Zener diode clamp. I_{DD}, the supply current for V_{DD}, can be estimated by:

I_{DD} ≈ *1.5 mA x 300 x* 10^{-9} *x switching frequency + 0.5 mA + 0.5 mA*
(Dynamic power consumption) (Static) (Zener bias)

The value of R_{DD} used to supply I_{DD} should meet the following requirement:

$$R_{DD} \le \frac{V_{+B} - 10.2\,V}{I_{DD}} \quad [\Omega]$$

Example: In the case where the average PWM switching frequency is 400 kHz, the required I_{DD} is 1.18 mA. Based on this calculation, a 50 V power supply voltage would require R_{DD} to be 33 kΩ or less.

Furthermore, make sure I_{DD} is below the maximum zener diode bias current, I_{DDZ}, during static state conditions.

$$I_{DDZ} \ge \frac{V_{+B} - 10.2\,V}{Rdd} - 0.5\,mA$$

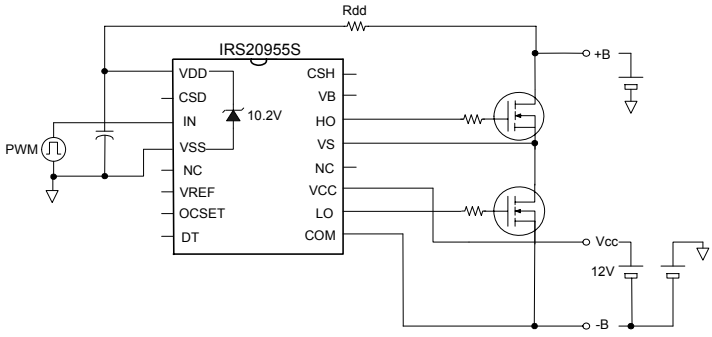

Figure 18. Supplying V_{DD}

Charging V_{BS} Prior to Start

The high-side bootstrap capacitor can be charged through a resistor from the positive supply bus to the V_B pin by utilizing an internal 20.4 V Zener diode between V_B and V_S. This scheme eliminates the need to charge the boot strap capacitor through low-side turn on during start-up.

The value of this charging resistor is subject to several constraints:

- The minimum value of R_{CHARGE} is limited by the leakage current of the bootstrap voltage supply through $_{RCHARGE}$, which would limit the maximum PWM modulation index of the system.
- The maximum value of R_{CHARGE} is limited by the current charge capability of the resistor during startup:
  $I_{CHARGE} > I_{QBS}$
  where I_{CHARGE} = the current through R_{CHARGE}
  I_{QBS} = the high side quiescent current.

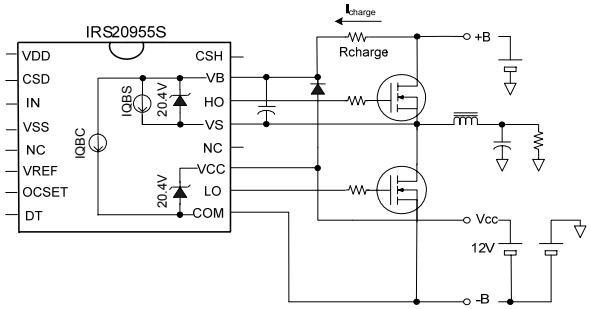

Figure 19. Boot Strap Supply Pre-charging

Start-up Sequence (UVLO)

The protection control block in the IRS20955S monitors the status of V_{DD} and V_{CC} to ensure that both voltage supplies are above the UVLO (under-voltage lockout) threshold before beginning normal operation. If either V_{DD} or V_{CC} is below the under voltage threshold, LO and HO are disabled in shutdown mode until both V_{DD} and V_{CC} rise above the voltage threshold.

Power-down Sequence

As soon as V_{DD} or V_{CC} falls below the UVLO threshold, protection logic in the IRS20955S turns off LO and HO, shutting off the power MOSFETs.

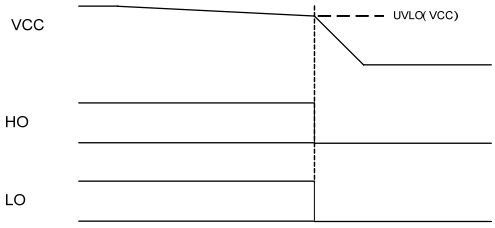

Figure 20. IRS20955 UVLO Timing Chart

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Power Supply Decoupling

As the IRS20955S contains analog circuitry, careful attention must be given to decoupling the power supplies for proper operation. Ceramic capacitors of 0.1 µF or more should be placed close to the power supply pins of the IC on the board.

Please refer to the application note AN-978 for general design considerations of a high voltage gate driver IC.

V_{SS} Negative Bias Clamping

V_{SS} can go below COM when a negative supply is missing in a dual supply configuration. In this case, excessive negative V_{SS} voltage with respect to COM could damage the IRS20955S. Having a diode to clamp potential negative biases to V_{SS} is recommended to protect the IC. A standard recovery diode with a current rating of 1 A such as the 1N4002 is sufficient for this purpose.

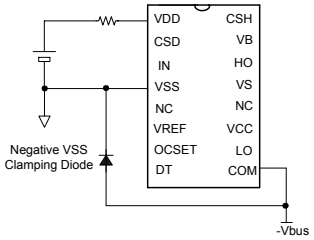

Figure 21. Negative V_{SS} Clamping

Junction Temperature Estimation

The power dissipation in the IRS20955S is dominated by the following items:

- P_{MID}: Power dissipation of the floating input logic and protection circuitry
- P_{LSM}: Power dissipation of the input level shifter
- P_{LOW}: Power dissipation in low-side
- P_{LSH}: Power dissipation of the high-side level shifter
- P_{HIGH}: Power dissipation in high-side

1. P_{MID}: Power Dissipation of the Floating Input Logic and Protection Circuitry

The power dissipation of the floating input section is given by:

$$P_{MID} = P_{ZDD} + P_{LDD} \approx \frac{V_{+BUS} - V_{DD}}{R_{DD}} \cdot V_{DD}$$

where
P_{ZDD} = the power dissipation from the internal Zener diode clamping V_{DD}

P_{LDD} = the power dissipation from the internal logic circuitry

V_{+BUS} = the positive bus voltage feeding V_{DD}

R_{DD} = the resistor feeding V_{DD} from V_{+BUS}

*For obtaining the value of R_{DD}, refer to the section “Supplying V_{DD}.”

2. P_{LSM}: Power Dissipation of the Input Level Shifter

P_{LSM} = 2 nC x f_{sw} x $V_{SS,BIAS}$

where
f_{SW} = the PWM switching frequency

$V_{SS,BIAS}$ = the bias voltage of V_{SS} with respect to COM

3. P_{LOW}: Power Dissipation in Low-Side

The power dissipation in low-side comes from the losses of the logic circuitry and the losses of driving LO.

$$P_{LOW} = P_{LDD} + P_{LO}$$
$$= \left(I_{QCC} \cdot V_{CC}\right) + \left(Vcc \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}} \right)$$

where
P_{LDD} = the power dissipation from the internal logic circuitry

P_{LO} = the power dissipation from the gate drive stage to LO

R_O = the output impedance of LO, typically 10 Ω for the IRS20955S

$R_{g(int)}$ = the internal gate resistance of the low side MOSFET driver, typically 10 Ω for the IRS20955S

R_g = the external gate resistance of the low side MOSFET

Q_g = total gate charge of the low side MOSFET

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4. P_{LSH}: Power Dissipation of the High-Side Level Shifter

P_{LSH} = 0.4 nC x f_{sw} x V_{BUS}

where
f_{SW} = the PWM switching frequency

V_{BUS} = the difference between the positive bus voltage and negative bus voltage

5. P_{HIGH}: Power Dissipation in High-side

The power dissipation in high-side comes from the losses of the logic circuitry and the losses of driving LO.

$$P_{HIGH} = P_{LDD} + P_{HO}$$
$$= \left(I_{QBS} \cdot V_{BS}\right) + \left(V_{BS} \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}} \right)$$

where

P_{LDD} = the power dissipation from the internal logic circuitry

P_{LO} = the power dissipation from the gate drive stage to HO

R_O = equivalent output impedance of HO, typically 10 Ω for the IRS20955S

$R_{g(int)}$ = the internal gate resistance of the high-side MOSFET driver, typically 10 Ω for the IRS20955S

R_g = external gate resistance of the high-side MOSFET

Q g = total gate charge of the high- side MOSFET

Total power dissipation, P_d, is given by

$$P_d = P_{MID} + P_{LSM} + P_{LOW} + P_{HSM} + P_{HIGH} \cdot$$

Given $R_{th,JA}$, the thermal resistance between the ambient and junction temperature, T_J, the junction temperature, can be calculated from the formula provided below.

$$T_J = R_{th,JA} \cdot P_d + T_A < 150\ ^\circ C$$

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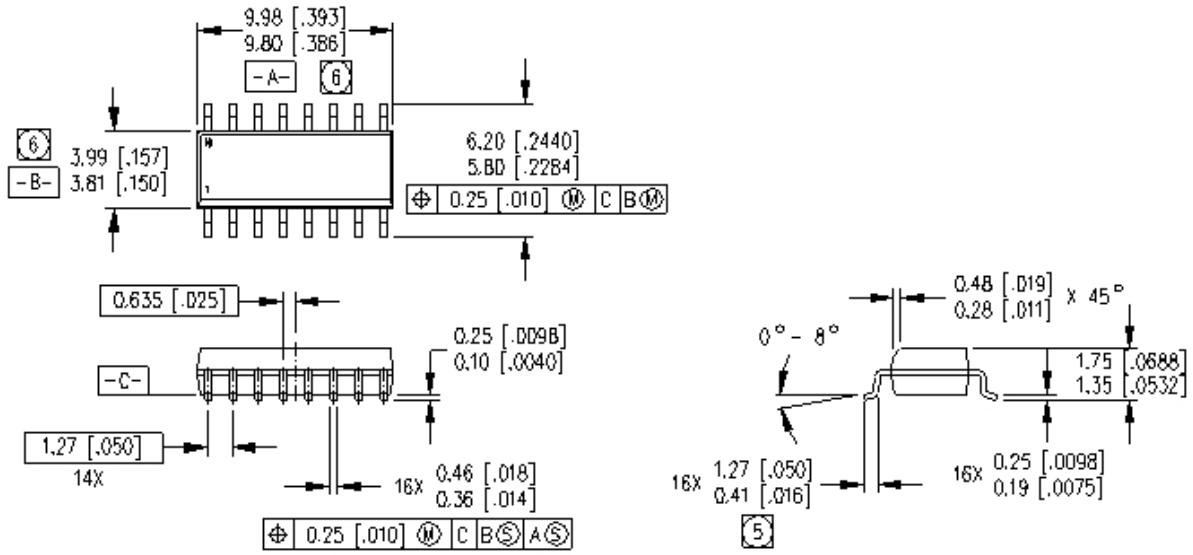
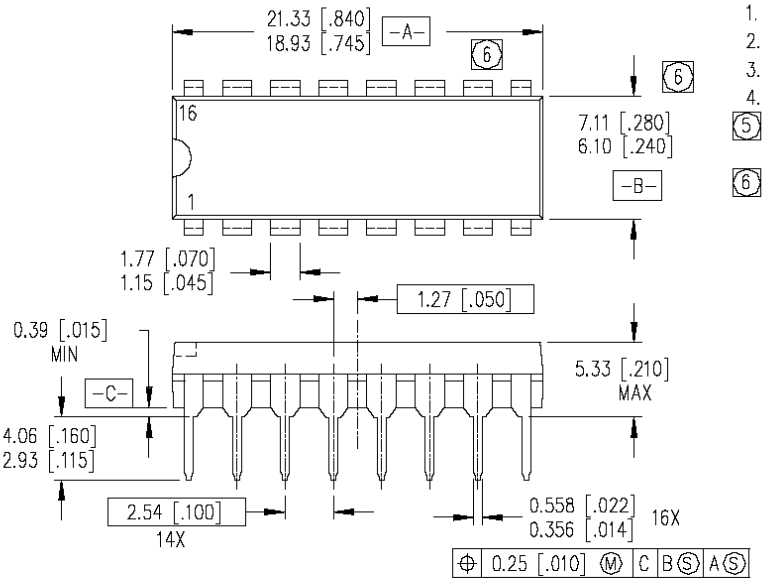


NOTES:

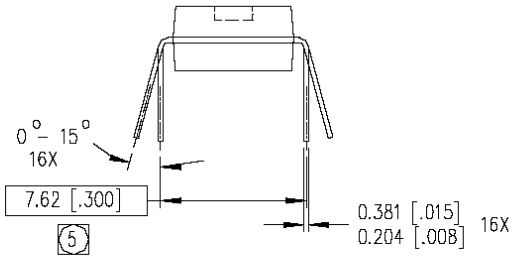
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5W-1982
2. CONTROLLING DIMENSION. MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETER [INCHES]
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006]

16-Lead SOIC (narrow body)



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



16-Lead PDIP

01-6015
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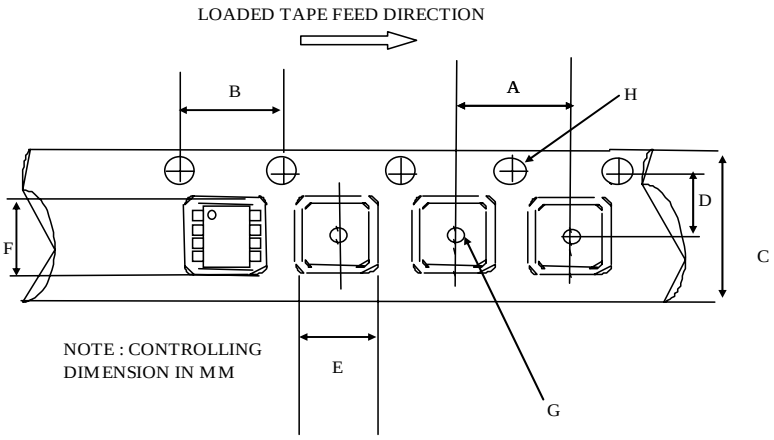
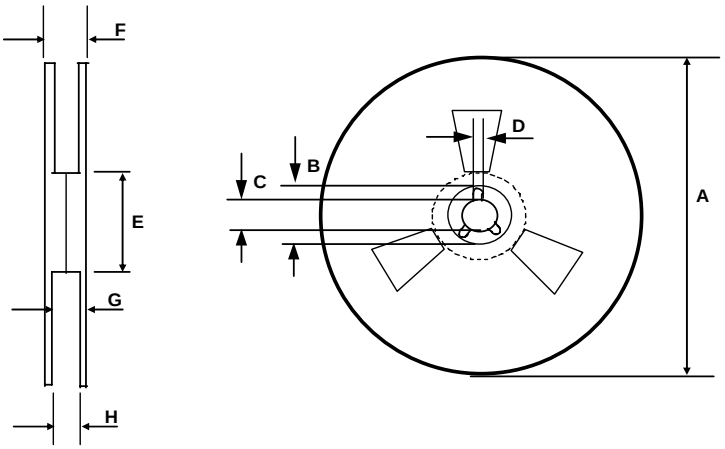


CARRIER TAPE DIMENSION FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

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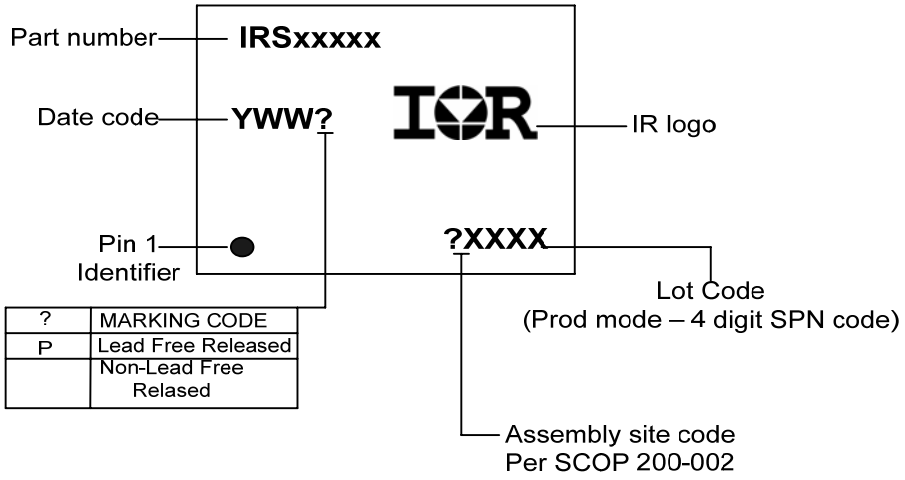
LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
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16-Lead SOIC Tape & Reel IRS20955STRPbF

Revision History

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