4-Mbit (512K x 8) Static RAM

Features

- **Temperature Ranges**
  - — **Commercial: 0°C to 70°C**
  - — **Industrial: –40°C to 85°C**
  - — **Automotive: –40°C to 125°C**
- **High speed**
  - — t_{AA} = 10 ns
- **Low active power**
  - — **324 mW (max.)**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description[1]

The CY7C1049CV33 is a high-performance CMOS Static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049CV33 is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram and Pin Configuration
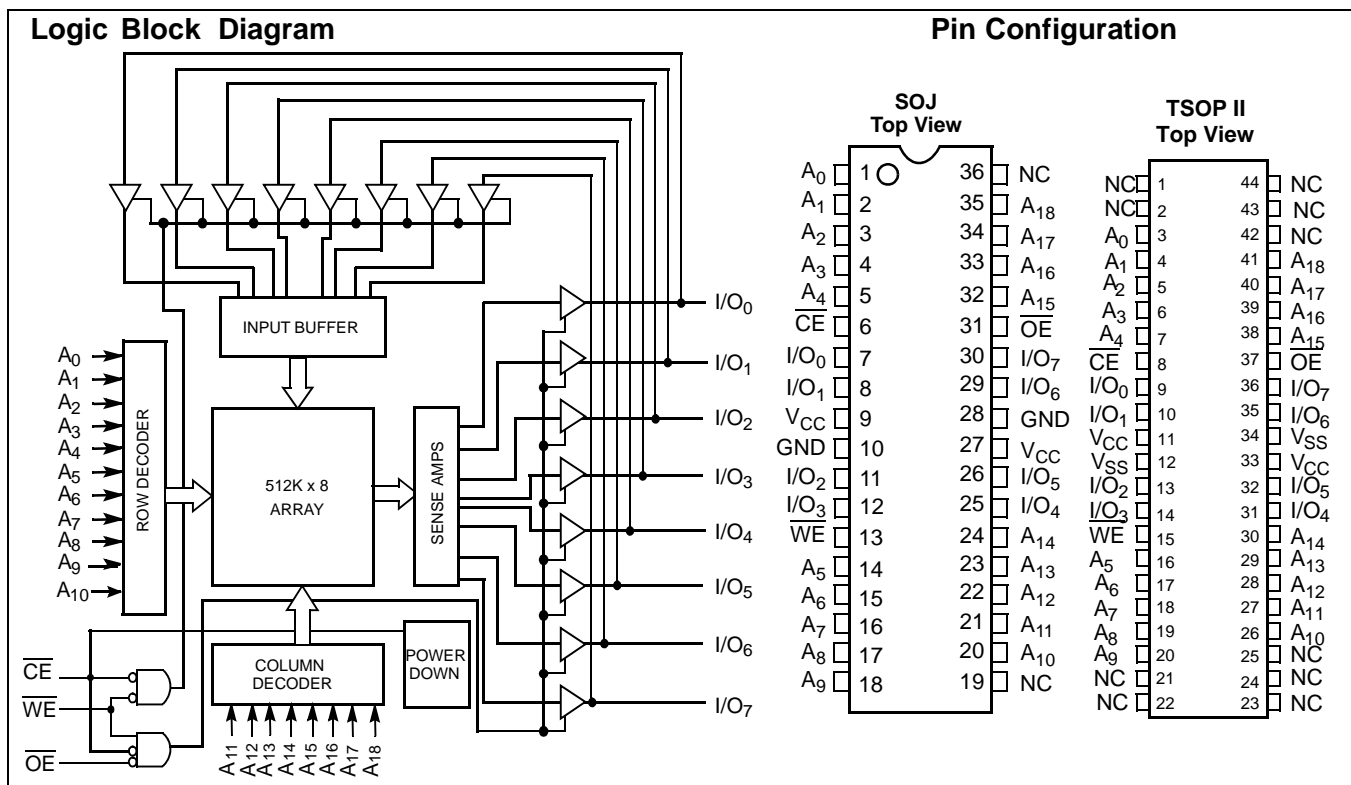
Notes:
1. For guidelines on SRAM system design, please refer to the *System Design Guidelines* Cypress application note, available on the internet at www.cypress.com.

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Selection Guide

		-8	-10	-12	-15	-20	Unit
Maximum Access Time		8	10	12	15	20	ns
Maximum Operating Current	Commercial	100	90	85	80	80	mA
	Industrial	110	100	95	90	90	mA
	Automotive	-	-	-	95	-	mA
Maximum CMOS Standby Current	Commercial / Industrial	10	10	10	10	10	mA
	Automotive	-	-	-	15	-	mA

Shaded areas contain advance information.

Pin Definitions

Pin Name	36-SOJ Pin Number	44 TSOP-II Pin Number	I/O Type	Description
A_0–A_{18}	1–5,14–18, 20–24,32–35	3–7,16–20, 26–30,38–41	Input	**Address Inputs used to select one of the address locations.**
I/O_0–I/O_7	7,8,11,12,25, 26,29,30	9,10,13,14, 31,32,35,36	Input/Output	**Bidirectional Data I/O lines.** Used as input or output lines depending on operation
NC[2]	19,36	1,2,21,22,23, 24,25,42,43, 44	No Connect	**No Connects.** This pin is not connected to the die
$\overline{WE}$	13	15	Input/Control	**Write Enable Input, active LOW.** When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
$\overline{CE}$	6	8	Input/Control	**Chip Enable Input, active LOW.** When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	31	37	Input/Control	**Output Enable, active LOW.** Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V_{SS}, GND	10,28	12,34	Ground	**Ground for the device.** Should be connected to ground of the system.
V_{CC}	9,27	11,33	Power Supply	**Power Supply inputs to the device.**

Notes:
2. NC pins are not connected on the die.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3]–0.5V to +4.6VDC

Voltage Applied to Outputs
in High-Z State[3] ....–0.5V to V_{CC} + 0.5V

Input Voltage[3] ....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW).. 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	
Automotive	–40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.; I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.,; I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	Com'l/Ind'l	–1	+1	–1	+1	–1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	Com'l/Ind'l	–1	+1	–1	+1	–1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = 1/t_{RC}	Com'l		100		90		85	mA
			Ind'l		110		100		95	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}; V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l		40		40		40	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		10		10		10	mA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.; I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.,; I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	Com'l / Ind'l	–1	+1	–1	+1	μA
			Automotive	–20	+20	-	-	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	Com'l / Ind'l	–1	+1	–1	+1	μA
			Automotive	–20	+20	-	-	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = 1/t_{RC}	Com'l		80		80	mA
			Ind'l		90		90	mA
			Automotive		95		-	mA

Note:
3. V_{IL} (min.) = –2.0V and V_{IH} (max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.

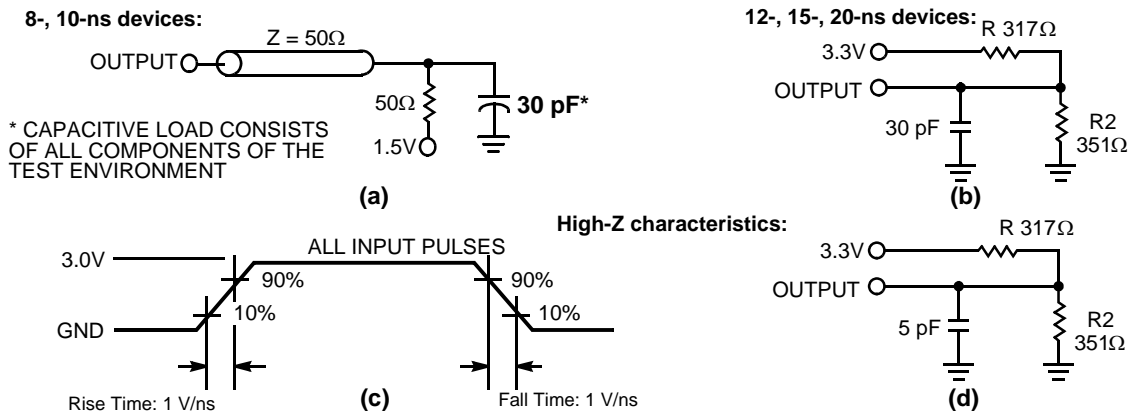## Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$; $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l / Ind'l		40		40	mA
			Automotive		45		-	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, f = 0	Com'l/Ind'l		10		10	mA
			Automotive		15		-	mA

Thermal Resistance[4]

Parameter	Description	Test Conditions	36-pin SOJ (Non Pb-Free)	36-pin SOJ (Pb-Free)	44-TSOP-II (Non Pb-Free)	44-TSOP-II (Pb-Free)	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	46.51	46.51	41.66	41.66	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		18.8	18.8	10.56	10.56	°C/W

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 3.3V$	8	pF
C_{OUT}	I/O Capacitance		8	pF

AC Test Loads and Waveforms[5]

8-, 10-ns devices:
OUTPUT — Z = 50Ω — 50Ω / **30 pF*** / 1.5V
* CAPACITIVE LOAD CONSISTS OF ALL COMPONENTS OF THE TEST ENVIRONMENT
(a)

12-, 15-, 20-ns devices: R 317Ω
3.3V — OUTPUT — 30 pF — R2 351Ω
(b)

ALL INPUT PULSES
3.0V — 90% / 10% — GND
90% / 10%
Rise Time: 1 V/ns
Fall Time: 1 V/ns
(c)

High-Z characteristics: R 317Ω
3.3V — OUTPUT — 5 pF — R2 351Ω
(d)

Notes:
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) for all 8-ns and 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

AC Switching Characteristics Over the Operating Range [6]

Parameter	Description	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
Read Cycle								
t_{power}[7]	V_{CC}(typical) to the first access	1		1		1		μs
t_{RC}	Read Cycle Time	8		10		12		ns
t_{AA}	Address to Data Valid		8		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	CE LOW to Data Valid		8		10		12	ns
t_{DOE}	OE LOW to Data Valid		4		5		6	ns
t_{LZOE}	OE LOW to Low-Z	0		0		0		ns
t_{HZOE}	OE HIGH to High-Z[8, 9]		4		5		6	ns
t_{LZCE}	CE LOW to Low-Z[9]	3		3		3		ns
t_{HZCE}	CE HIGH to High-Z[8, 9]		4		5		6	ns
t_{PU}	CE LOW to Power-up	0		0		0		ns
t_{PD}	CE HIGH to Power-down		8		10		12	ns
Write Cycle[10, 11]								
t_{WC}	Write Cycle Time	8		10		12		ns
t_{SCE}	CE LOW to Write End	6		7		8		ns
t_{AW}	Address Set-up to Write End	6		7		8		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	6		7		8		ns
t_{SD}	Data Set-up to Write End	4		5		6		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	WE HIGH to Low-Z[9]	3		3		3		ns
t_{HZWE}	WE LOW to High-Z[8, 9]		4		5		6	ns

Shaded areas contain advance information.

## AC Switching Characteristics Over the Operating Range [6]

| Parameter	Description	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
Read Cycle						
t_{power}[7]	V_{CC}(typical) to the first access	1		1		μs
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address to Data Valid		15		20	ns
t_{OHA}	Data Hold from Address Change		3		3	ns
t_{ACE}	CE LOW to Data Valid		15		20	ns
t_{DOE}	OE LOW to Data Valid		7		8	ns

Notes:
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
7. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. The internal Write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

## AC Switching Characteristics Over the Operating Range (continued)[6]

Parameter	Description	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		7		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		15		20	ns
Write Cycle[10, 11]						
t_{WC}	Write Cycle Time	15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		10		ns
t_{AW}	Address Set-up to Write End	10		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		10		ns
t_{SD}	Data Set-up to Write End	7		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8, 9]		7		8	ns

Switching Waveforms

Read Cycle No. 1[12, 13]
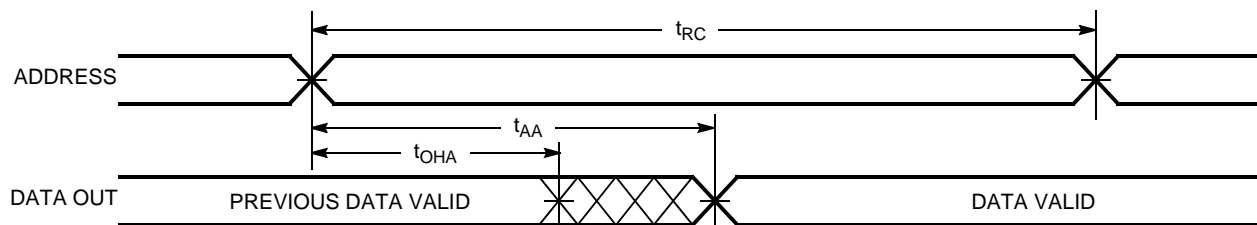
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)[13, 14]
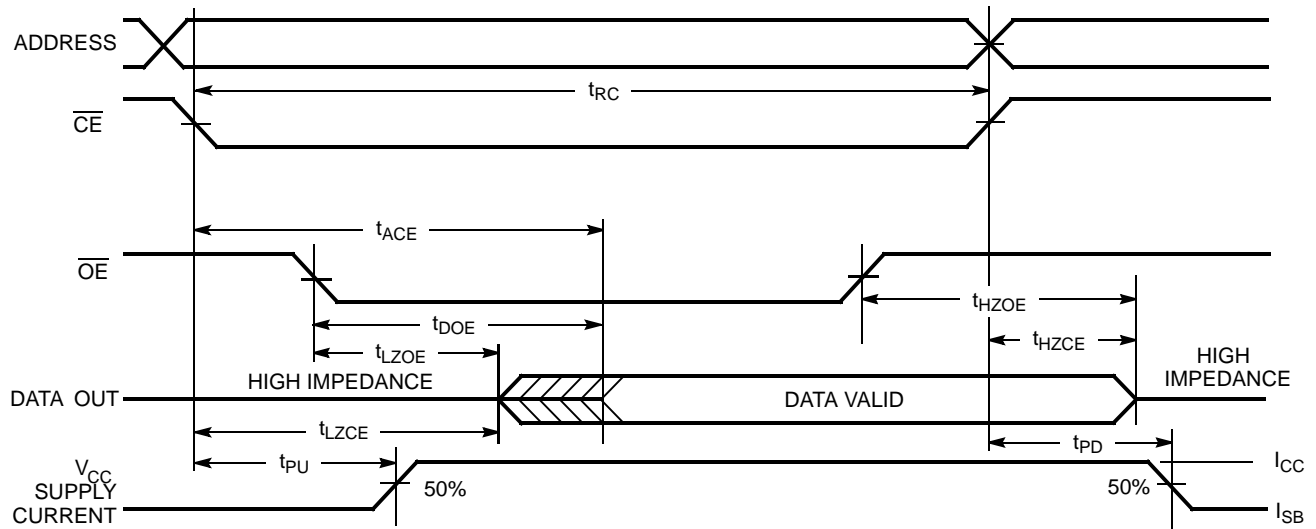
Write Cycle No. 1($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)[15, 16]
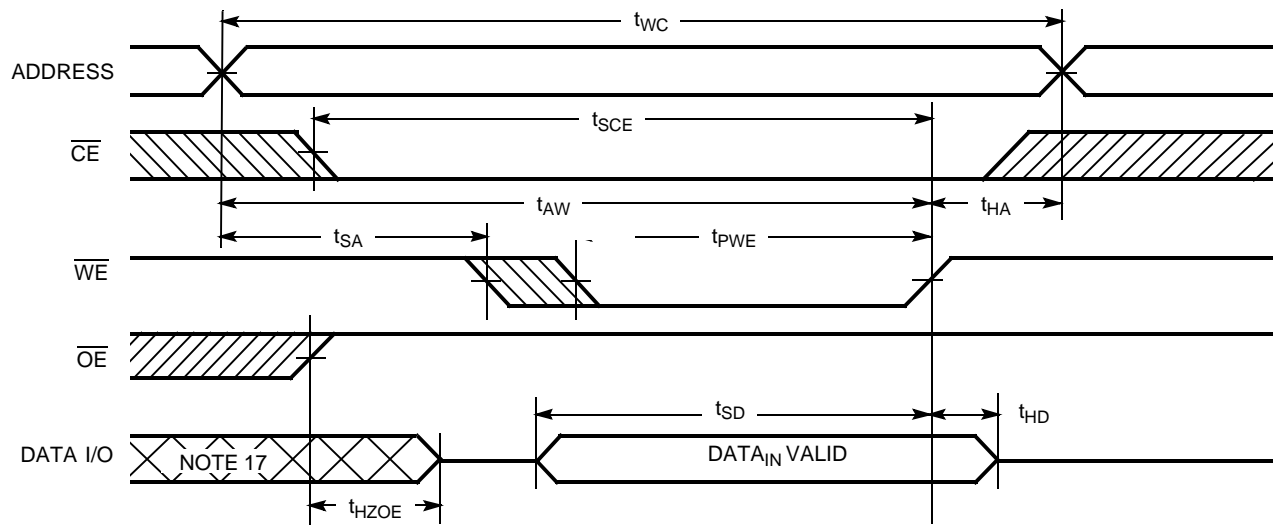
Notes:
14. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
15. Data I/O is high-impedance if $\overline{\text{OE}} = V_{IH}$.
16. If CE goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
17. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16]
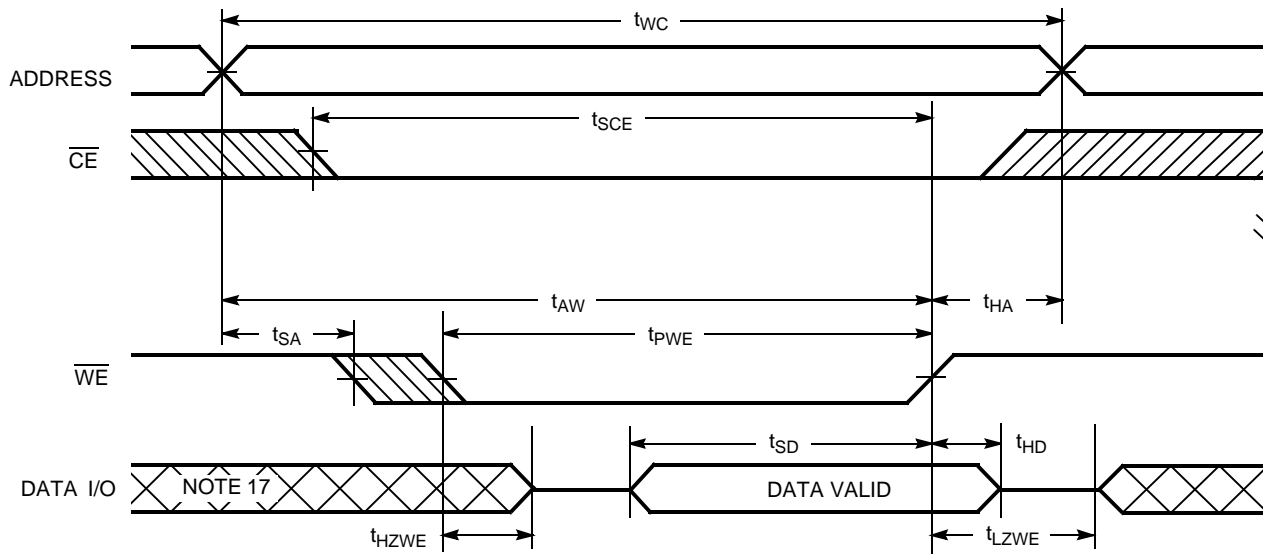
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O$_0$–I/O$_7$	Mode	Power
H	X	X	High-Z	Power-down	Standby (I$_{SB}$)
L	L	H	Data Out	Read	Active (I$_{CC}$)
L	X	L	Data In	Write	Active (I$_{CC}$)
L	H	H	High-Z	Selected, Outputs Disabled	Active (I$_{CC}$)

Ordering Information

| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1049CV33-10VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-10ZC	Z44	44-pin TSOP II	
	CY7C1049CV33-10VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
	CY7C1049CV33-10ZI	Z44	44-pin TSOP II	
12	CY7C1049CV33-12VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-12ZC	Z44	44-pin TSOP II	
	CY7C1049CV33-12VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
	CY7C1049CV33-12ZI	Z44	44-pin TSOP II	
15	CY7C1049CV33-15VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-15ZC	Z44	44-pin TSOP II	
	CY7C1049CV33-15VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
	CY7C1049CV33-15ZI	Z44	44-pin TSOP II	
	CY7C1049CV33-15VE	V36	36-lead (400-Mil) Molded SOJ	Automotive
	CY7C1049CV33-15ZSE	Z44	44-pin TSOP II	
20	CY7C1049CV33-20VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-20VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
10	CY7C1049CV33-10VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049CV33-10ZXC	Z44	44-pin TSOP II (Pb-Free)	
	CY7C1049CV33-10VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049CV33-10ZXI	Z44	44-pin TSOP II (Pb-Free)	Industrial
12	CY7C1049CV33-12VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049CV33-12ZXC	Z44	44-pin TSOP II (Pb-Free)	
	CY7C1049CV33-12VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049CV33-12ZXI	Z44	44-pin TSOP II (Pb-Free)	
15	CY7C1049CV33-15VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049CV33-15ZXC	Z44	44-pin TSOP II (Pb-Free)	
	CY7C1049CV33-15VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049CV33-15ZXI	Z44	44-pin TSOP II (Pb-Free)	
	CY7C1049CV33-15VXE	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Automotive
	CY7C1049CV33-15ZSXE	Z44	44-pin TSOP II	Automotive
20	CY7C1049CV33-20VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049CV33-20VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial

Shaded areas contain advance information. Please contact your local Cypress Sales representative for availability of these parts.

Package Diagrams

36-Lead (400-Mil) Molded SOJ V36
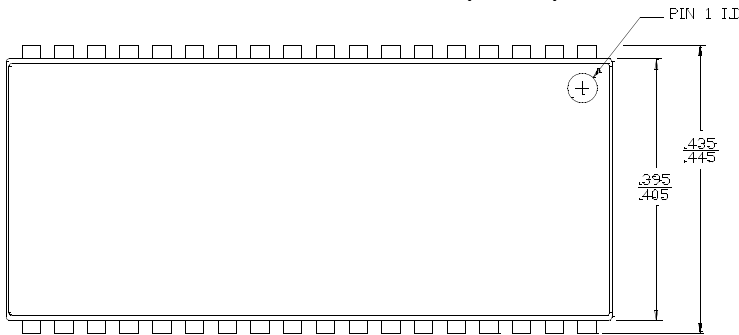
DIMENSIONS IN INCHES MIN.
                    MAX.

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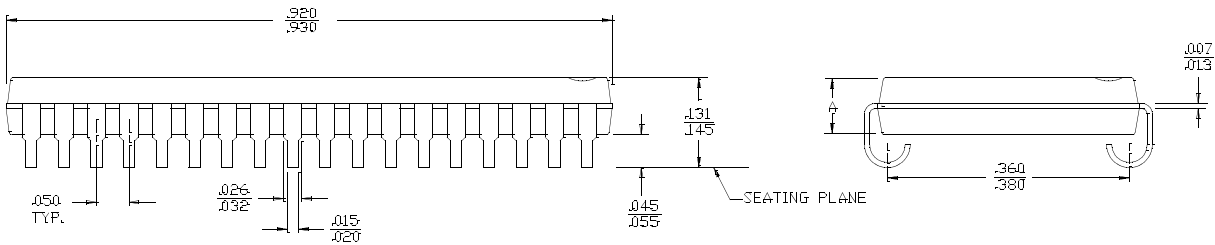
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44-pin TSOP II Z44
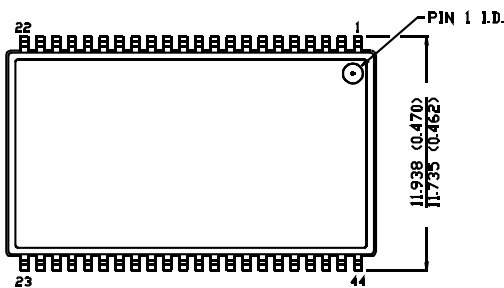
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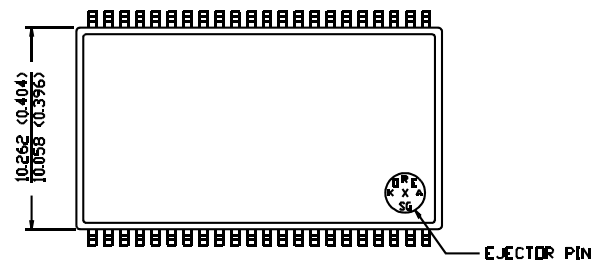
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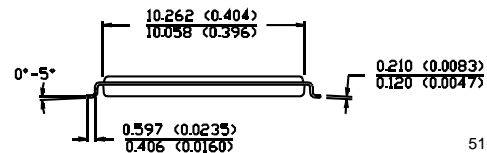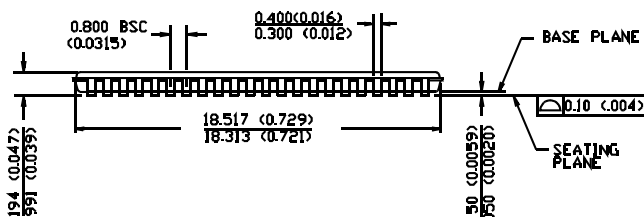
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[+] Feedback

Document History Page

Document Title: CY7C1049CV33 4-Mbit (512K x 8) Static RAM Document Number: 38-05006				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112569	03/06/02	HGK	New data sheet
*A	114091	04/25/02	DFP	Changed Tpower unit from ns to μs
*B	116479	09/16/02	CEA	Add applications foot note to data sheet, page 1.
*C	262949	See ECN	RKF	Added Automotive Specs Added Θ_{JA} and Θ_{JC} values on Page #3.
*D	300091	See ECN	RKF	Added -20-ns Speed bin
*E	344595	See ECN	SYT	Added Pb-Free package on page #8 Removed shading for CY7C1049CV33-15ZSXE in the ordering Information on page 9