TOSHIBA Bi-CMOS Integrated Circuit   Silicon Monolithic

TB62779FNG

9-Channel Constant-Current LED Driver of the 3.3-V and 5-V Power Supply Voltage Operation

The TB62779FNG is a constant-current driver designed for LED and LED display lighting.

The TB62779FNG incorporates nine channels of seven-bit PWM dimming controllers and constant-current drivers. Nine constant-current drivers are divided into three blocks, each consisting of three drivers, and the output current of each can be independently adjusted by the relevant external resistor.

The TB62779FNG is controlled using the DATA and CLK input signals. Up to 64 slave IDs (slave addresses) can be independently assigned to the TB62779FNG.

Fabricated using the Bi-CMOS process, the TB62779FNG is capable of high-speed data transfers.

The TB62779FNG operates with a supply voltage of 3.3 V or 5 V.

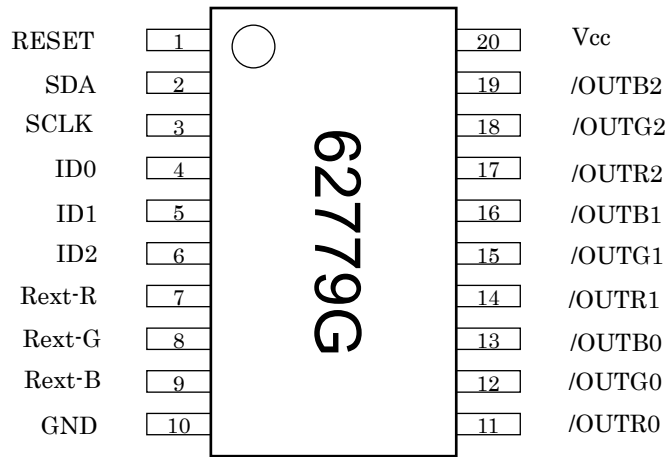The TB62779FNG is RoHS (2002/95/EL) compliant.
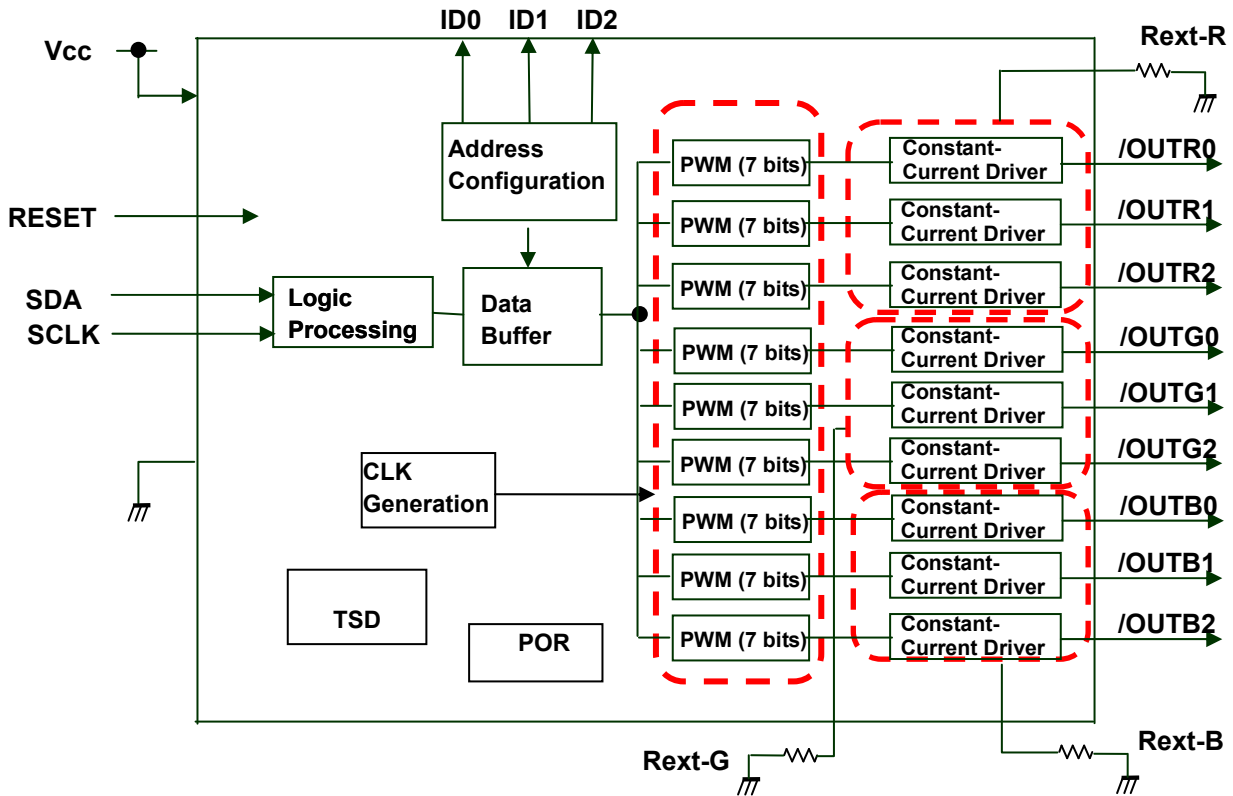

SSOP20-P-225-0.65A
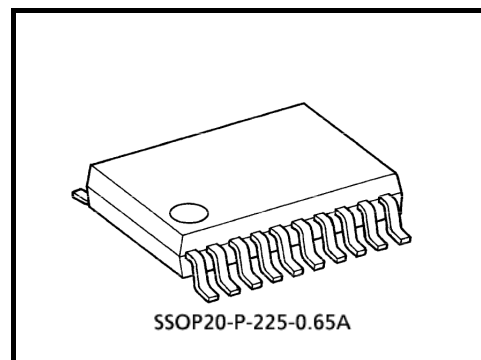
Weight: 0.10 g (typ.)

1. Features

- Power supply voltages: V_{CC} = 3.3 V/5 V
- Output drive capability and output count: 80 mA (max)× 9 channels
- Constant-current output range: 5 to 40 mA
- Voltage applied to constant-current output terminals: 0.4 V(min) (I_{OUT} = 5 to 40 mA)
- Designed for common-anode LEDs
- The input interface is controlled by the DATA and CLK signal lines.
- Thermal shutdown (TSD) (min: 150°C)
- Logical Input signal voltage level: 3.3-V and 5-V CMOS interfaces (Schmitt trigger input)
- Maximum output voltage: 28 V
- Incorporates PWM control circuitry: Provides seven-bit PWM control.
- Driver identification: Up to 64 drivers can be controlled individually.
- Operating temperature range: T_{opr} = −40 to 85°C
- Package: SSOP20-P-225-0.65A

- Constant-current accuracy

Output Voltage	Current accuracy Between Channels	Current Accuracy Between ICs	Output Current
0.4 V to 4 V	±3%	±6%	15 mA

2. Pin Assignment (top view)

RESET	1		62779G	20	Vcc
SDA	2			19	/OUTB2
SCLK	3			18	/OUTG2
ID0	4			17	/OUTR2
ID1	5			16	/OUTB1
ID2	6			15	/OUTG1
Rext-R	7			14	/OUTR1
Rext-G	8			13	/OUTB0
Rext-B	9			12	/OUTG0
GND	10			11	/OUTR0

3. Block Diagram

Note: The values of external resistors that are used for adjusting the output current (Rext-R, Rext-G and Rext-B) should be independently specified.
Three resistors must not be collectively connected to a single pin.

4. Terminal Description

| Pin No,	Symbol	Function
1	RESET	Reset signal input. (Setting this pin High resets internal data.) (Note 1)
2	SDA	Serial data input terminal
3	SCLK	Serial clock input terminal
4	ID0	ID configuration pin (Note 1)
5	ID1	ID configuration pin (Note 1)
6	ID2	ID configuration pin (Note 1)
7	Rext-R	External resistor pin for output current configuration (/OUTR0, /OUTR1, /OUTR2)
8	Rext-G	External resistor pin for output current configuration (/OUTG0, /OUTG1, /OUTG2)
9	Rext-B	External resistor pin for output current configuration (/OUTB0, /OUTB1, /OUTB2)
10	GND	Ground pin
11	/OUTR0	Constant-current output terminal (Open-collector type)
12	/OUTG0	Constant-current output terminal (Open-collector type)
13	/OUTB0	Constant-current output terminal (Open-collector type)
14	/OUTR1	Constant-current output terminal (Open-collector type)
15	/OUTG1	Constant-current output terminal (Open-collector type)
16	/OUTB1	Constant-current output terminal (Open-collector type)
17	/OUTR2	Constant-current output terminal (Open-collector type).
18	/OUTG2	Constant-current output terminal (Open-collector type)
19	/OUTB2	Constant-current output terminal (Open-collector type)
20	Vcc	Power supply terminal

Note 1: After the reset is released, it should be ensured that IDs (slave addresses) are properly configured.

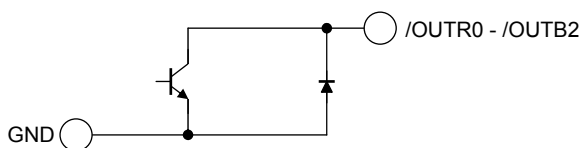## 5. Equivalent Circuits for Inputs and Outputs
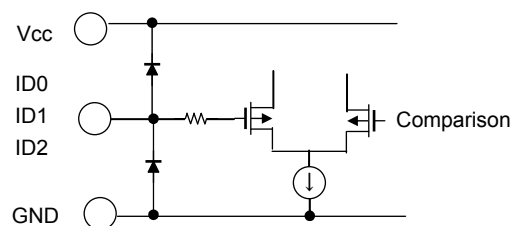
SDA, SCLK Terminals
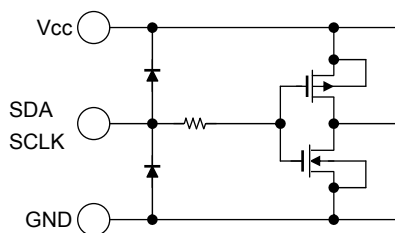
RESET Terminals
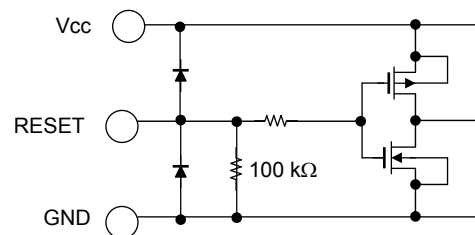
/OUTR0 to /OUTB2 Constant-Current Output Terminals

ID0, ID1, ID2 Terminals

6. Programming the TB62779FNG

The TB62779FNG can be programmed by the DATA signal on the SDA pin (pin 2) and CLK signal on the SCK pin (pin 3). Though the specification of these signal lines is similar to that of the I2C bus, these lines are only used to program data to the TB62779FNG and bi-directional data transfers are not performed. The TB62779FNG should basically be programmed using one of the following formats: (1) Serial Packet Format in Normal Programming Mode or (2) Serial Packet Format in Special Mode 1.
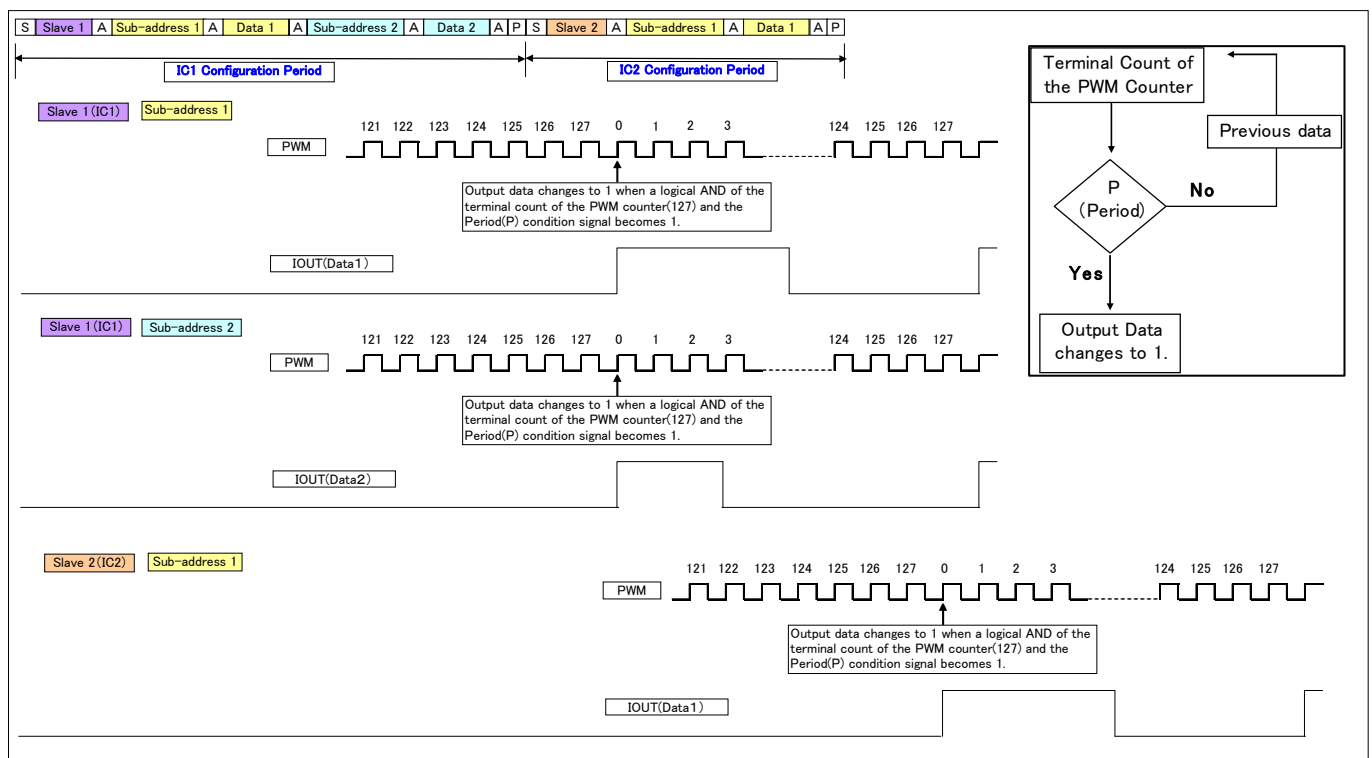
1) Serial Packet Format in Normal Programming Mode
【Typical】

S	Slave address 8 bits	A	Sub-address (Channel select) 8 bits	A	Data byte (PWM configuration) 8 bits	A	P

S: Start command; A: Acknowledge command; P: Period command

a) Data Programming Timing 1

Note: As shown in the above timing diagram, output data changes to 1 when the PWM counter reaches its terminal count after the Period condition is shifted in. Therefore, even after the P condition, the next packet should not be shifted in before the PWM counter reaches its terminal count. Otherwise, the data programmed before the P condition is overwritten with the next data. After the P condition, an interval of about 3.0 ms (128 PWM cycles) is required before shifting in the next packet.

2) Serial Packet Format in Special Mode 1

When the sub-address is specified to 1000XXXX, all the channels are selected in order. Make sure that data for all nine channels are provided.
(If data for more than nine channels are provided, the 10th and subsequent data are treated as invalid. If data for less than nine channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.)
To put the TB62779FNG back into Normal mode, a Start condition should be transmitted first.
In Special Mode 1, the sub address is set with a value of 8 x slave instruction/IC.

S	Slave Address	A	Sub-Address(channel select) 8bits (1000XXXX)	A	Data /OUTR0	A	Data /OUTG0	A	Data /OUTB0	A	Data /OUTR1	A	Data /OUTG1	A	Data /OUTB1	A	Data /OUTR2	A	Data /OUTG2	A	Data /OUTB2	A	P

3) Data Write Start Condition (S) and Period Condition (P)
    Start condition: A High to Low transition on the SDA line while SCLK is High.
   Period condition: A Low to High transition on the SDA line while SCLK is High.

SDA

SCLK   S   P

Start condition   Period condition
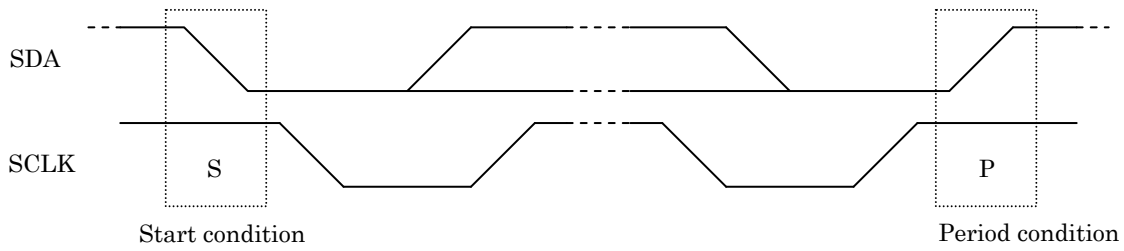
4) Setup and Hold Conditions
    The SDA signal must be changed when SCLK is Low.

SDA

SCLK

DATA must not be changed.

DATA can be changed.
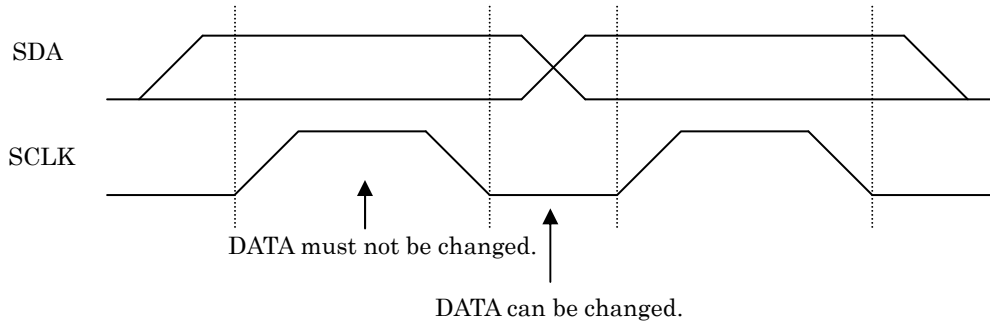
5) Acknowledge
    CLK signals for acknowledgement must be generated after every byte received.
    (Though the TB62779FNG is not designed to perform bi-directional data transfers, it must generate this acknowledgement clock signal.)

SDA

Invalid

SCL   S   1   8   9

Clock pulse for acknowledgement
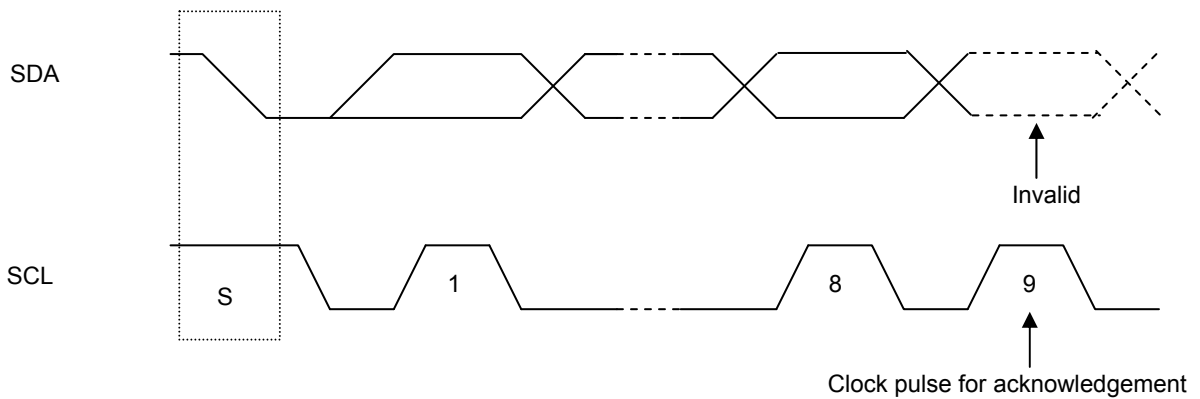
6) Data Settings

a) Slave Addresses

Input voltages and logic states of the ID0, ID1 and ID2 pins are determined as follows (where the LSB = 0):

Vcc = "11", 2/3Vcc = "10", 1/3Vcc = "01", GND = "00"

Select Address	ID2	ID1	ID0
00000000	GND	GND	GND
00000010	GND	GND	1/3Vcc
00000100	GND	GND	2/3Vcc
…	…	…	…
01111100	Vcc	Vcc	2/3Vcc
01111110	Vcc	Vcc	Vcc
1XXXXX0	All Select		

b) Sub-Addresses

Output channel select / All channel select / Special mode select

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	channel select
0	0	0	0	0	0	0	1	/OUTR0
0	0	0	0	0	0	1	0	/OUTG0
0	0	0	0	0	0	1	1	/OUTB0
0	0	0	0	0	1	0	0	/OUTR1
0	0	0	0	0	1	0	1	/OUTG1
0	0	0	0	0	1	1	0	/OUTB1
0	0	0	0	0	1	1	1	/OUTR2
0	0	0	0	1	0	0	0	/OUTG2
0	0	0	0	1	0	0	1	/OUTB2
1	1	1	1	×	×	×	×	All channel select
1	0	0	0	×	×	×	×	Special mode1

×: Don't care

c) Data Bytes (PWM configuration)

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	PWM Dimming (for reference only)
0	0	0	0	0	0	0	0	0/127(Default)
0	0	0	0	0	0	0	1	1/127
0	0	0	0	0	0	1	0	2/127
								to
0	1	1	1	1	1	1	0	126/127
0	1	1	1	1	1	1	1	127/127

Note: Any data other than those specified above must not be programmed.

7. Power-ON Reset (POR)

The POR circuitry resets all the internal data to the default values upon powering up the TB62779FNG in order to ensure proper device operation.
The POR circuitry is only activated when Vcc rises from 0 V. To reactivate POR, Vcc must be powered down to 0 V. The internal data hold voltage is guaranteed after Vcc has once reached or exceeded 3.0 V.

Initial Clear
Vcc Waveform

2.0 V — — — — — Reset Completion Voltage

1.8 V — — — — — Minimum Data Hold Voltage

POR Completed

0 V

POR Active | POR Not Active | POR Active
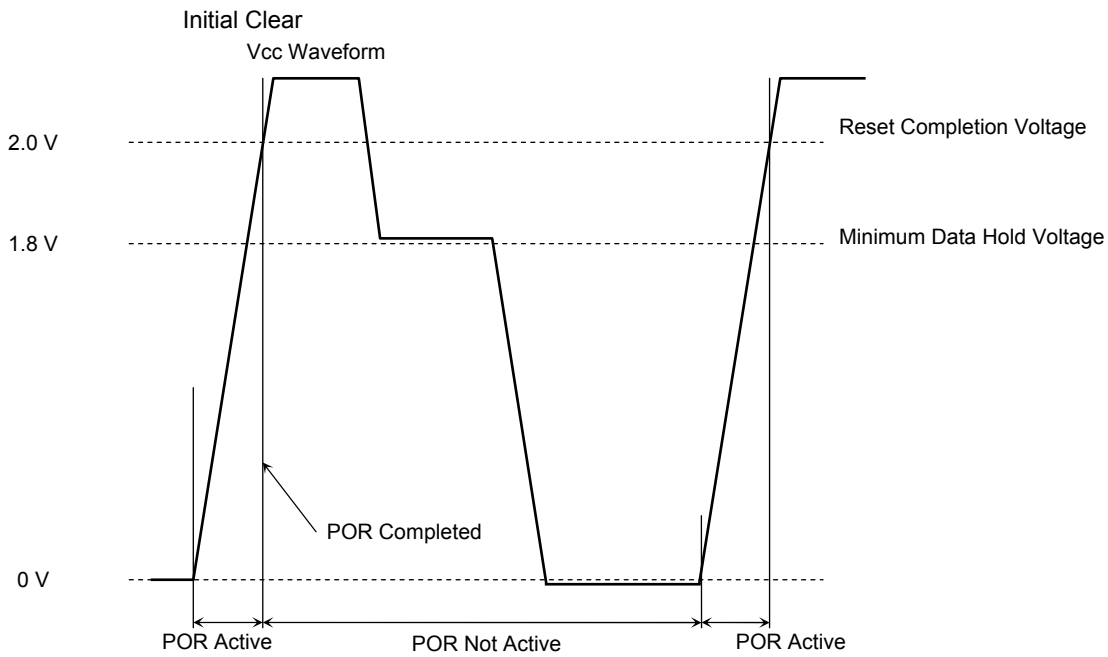
8. Thermal Shutdown (TSD)

When the die temperature reaches 150°C, the thermal shutdown circuit is tripped, switching the constant-current outputs to off.
The constant-current outputs are automatically turned on when the temperature cools past the shutdown threshold.

TSD trip temperature: 150°C to 170°C
TSD recovery temperature: 30°C below the TSD trip temperature

9. Points to Note when Setting Up the TB62779FNG

1. External resistors for specifying the LED driving current (Rext-R, Rext-G, Rext-B)
   External resistors should be separately connected to the Rext-R, Rext-G and Rext-B pins. Three resistors must not be collectively connected to a single pin.

2. External resistors for ID configuration
   The total resistance value of three external resistors used for specifying a device ID (which are connected between Vcc and GND) should be about 30 kΩ or lower.
   (A recommended value will be clearly defined after the TB62779FNG is completed.)

3. ID configuration sequence
   ID configuration can be performed after POR is released upon powering on. However, to avoid false operation of the ID configuration, transient input signals of less than two clock cycles of the reference clock for the internal oscillator are not accepted.
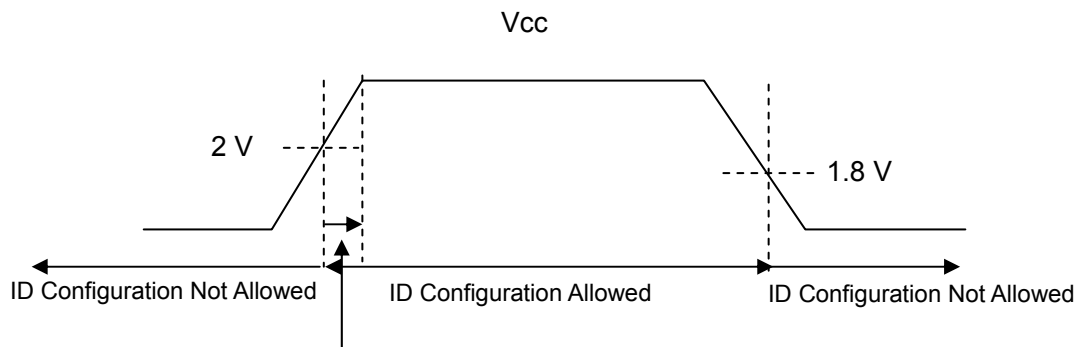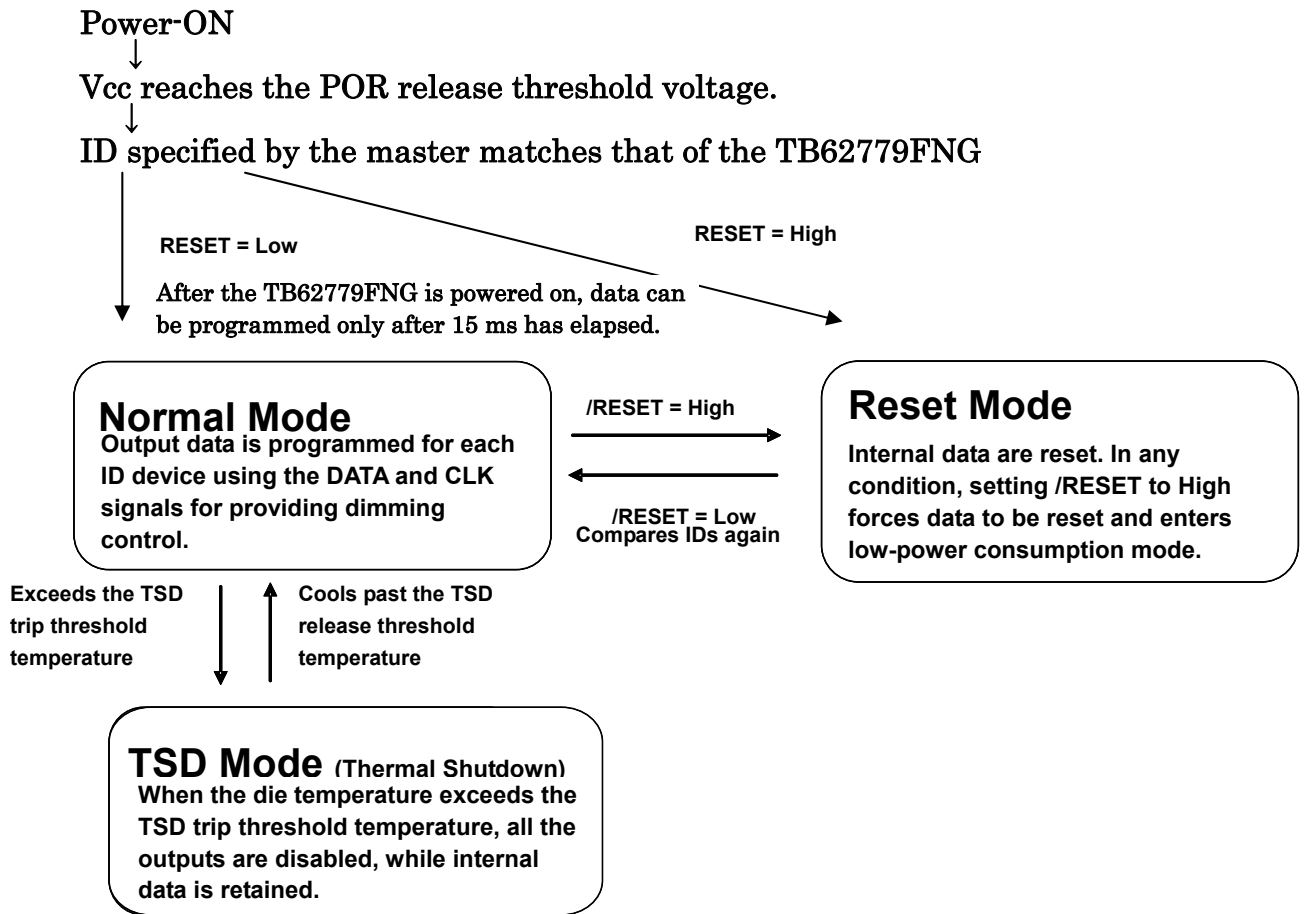

Care should be taken during the period between the POR released timing and the timing when power supply has reached the rated Vcc voltage.

4. ID configuration
   Make sure to set IDs after releasing reset condition.

10. State Transition Diagram

Power-ON
↓
Vcc reaches the POR release threshold voltage.
↓
ID specified by the master matches that of the TB62779FNG

RESET = Low

RESET = High

After the TB62779FNG is powered on, data can
be programmed only after 15 ms has elapsed.

Normal Mode
Output data is programmed for each
ID device using the DATA and CLK
signals for providing dimming
control.

/RESET = High

/RESET = Low
Compares IDs again

Reset Mode

Internal data are reset. In any
condition, setting /RESET to High
forces data to be reset and enters
low-power consumption mode.

Exceeds the TSD
trip threshold
temperature

Cools past the TSD
release threshold
temperature

TSD Mode (Thermal Shutdown)
When the die temperature exceeds the
TSD trip threshold temperature, all the
outputs are disabled, while internal
data is retained.

11. Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	6.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3 (Note 1)	V
Output current	I_{OUT}	85	mA/ch
Output voltage	V_{OUT}	−0.3 to 29	V
Power dissipation	P_d	1.02 (Notes 2 and 3)	W
Thermal resistance	$R_{th (j-a)}$	122 (Note 2)	°C/W
Operating temperature range	T_{opr}	−40 to 85	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Maximum junction temperature	T_j	150	°C

Note 1:   However, do not exceed 6.0 V.

Note 2:   When mounted on a PCB (76.2 × 114.3 × 1.6 mm; Cu = 30%; 35-μm-thick; SEMI-compliant)

Note 3:   Power dissipation is reduced by $1/R_{th (j-a)}$ for each °C above 25°C ambient.

12. Operating Ranges (Ta = −40°C to 85°C, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	—	3	—	5.5	V
Output voltage	$V_{OUT (ON)}$	All Output	0.4	—	4	V
Output current	I_{OUT}	All Output	5	—	40	mA/ch

13. Electrical Characteristics (Ta = 25°C, VCC = 4.5 to 5.5 V, unless otherwise specified)

| Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	I_{OUT1}	4	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ Vcc = 5 V	12.69	13.5	14.31	mA
Output current error between channels	ΔI_{OUT2}	4	V_{OUT} = 0.4 V, R-EXT =1.2 kΩ All ch ON Vcc = 5 V	—	—	±3.0	%
Output leakage current	I_{OZ}	4	V_{OUT} = 28 V	—	—	1	μA
Input voltage	V_{IH}	—	SDA, SCLK, RESET	0.7 × Vcc	—	Vcc	V
	V_{IL}	—		GND	—	0.3 × Vcc	
	V_{ID0}	—	ID0, ID1, ID2	0	—	0.3	
	V_{ID1}	—		-0.3	1/3 Vcc	+0.3	
	V_{ID2}	—		-0.3	2/3 Vcc	+0.3	
	V_{ID3}	—		Vcc - 0.3	—	Vcc	
Input current	I_{IH}	1	SDA, SCLK、	—	—	1	μA
			RESET(Vcc = 5 V)	25	50	75	
	I_{IL}	2	SDA, SCLK, RESET	—	—	-1	
	I_{ID}	1,2	ID0, ID1, ID2	—	—	±0.1	
Changes in constant output current dependent on V_{CC}	%/Vcc	4	Vcc = 4.5 V to 5.5 V	—	1	2	%
Supply current	$I_{CC\,1}$	3	R-EXT = 1.2 kΩ, V_{OUT} = 0.4 V, RESET = L	—	8	12	mA
Current consumption in Reset mode	$I_{CC\,(RS)}$	3	R-EXT = 1.2 kΩ, V_{OUT} = 0.4 V, RESET = H (The input current of the RESET pin is excluded.)	—	—	1	μA
Time required for a mode transition from Reset mode to Normal mode	tON2	—	Time between a High to Low transition on RESET and the timing when an output current is generated after input data is applied.	—	—	3	ms
Output rise time	Tor	5	10% to 90% points of /OUTR0 to /OUTB2 voltage waveforms	—	20	150	ns
Output fall time	Tof	5	90% to 10% points of /OUTR0 to /OUTB2 voltage waveforms	—	125	300	ns

14. Input Signal Characteristics (T$_a$ = 25°C, Vcc = 4.5 to 5.5 V, unless otherwise specified)

Characteristics	Symbol	Test Circuit	Min	Max	Unit
SCLK frequency	fCLK	5	-	1.7	MHz
(Repeated) Start condition setup time	tSU;STA	5	320	-	ns
(Repeated) Start condition hold time	tHD;STA	5	320	-	ns
Period condition setup time	tSU;STO	5	320	-	ns
Data setup time	tSU;DAT	5	10	-	ns
Data hold time	tHD;DAT	5	0	-	ns
SCLK pulse width Low	tLOW	5	90	-	ns
SCLK pulse width High	tHIGH	5	45	-	ns
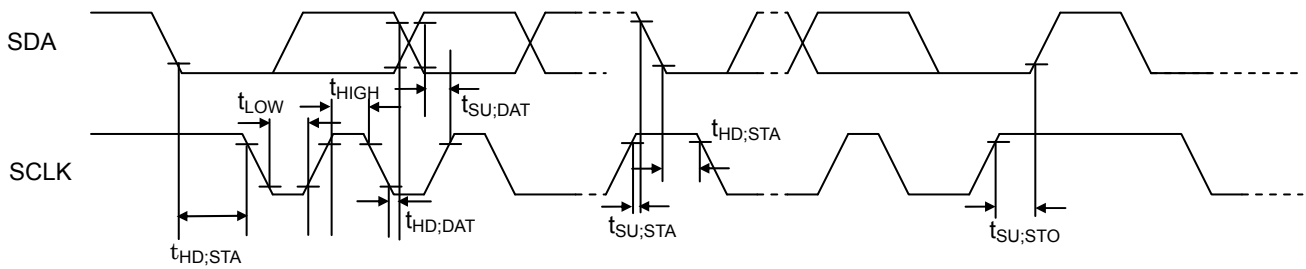
15. Test Circuits

Test Circuit 1: High-Level Input Current (I_{IH})
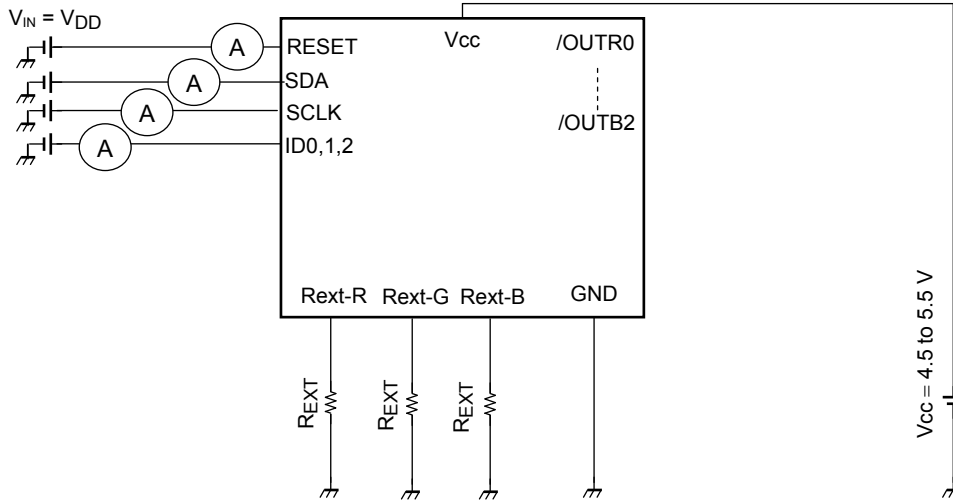
Test Circuit 2: Low-Level Input Current (I_{IL})
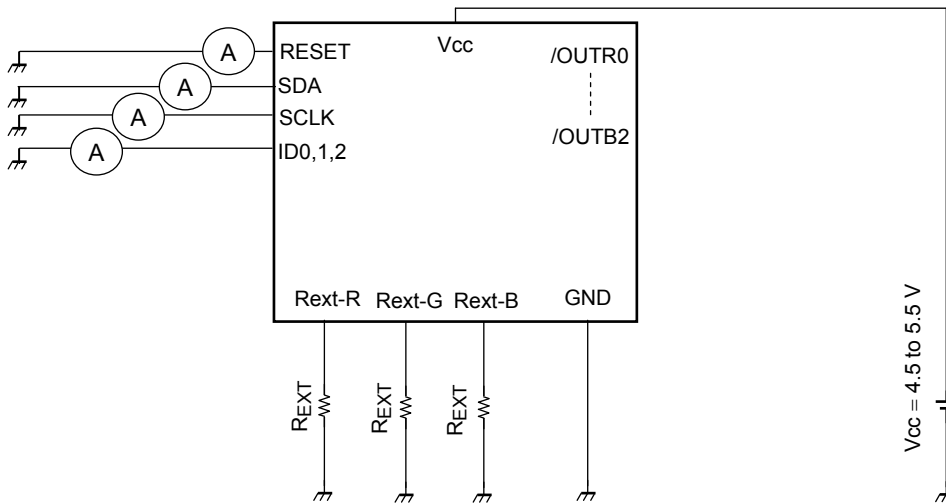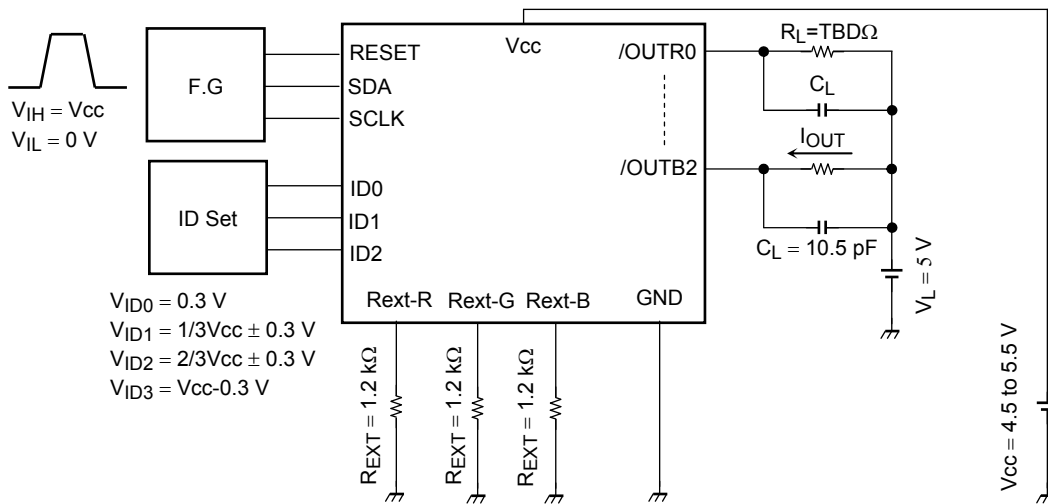

Test Circuit 3: Supply Current

$V_{ID0} = 0.3\ V$
$V_{ID1} = 1/3Vcc \pm 0.3\ V$
$V_{ID2} = 2/3Vcc \pm 0.3\ V$
$V_{ID3} = Vcc\text{-}0.3\ V$
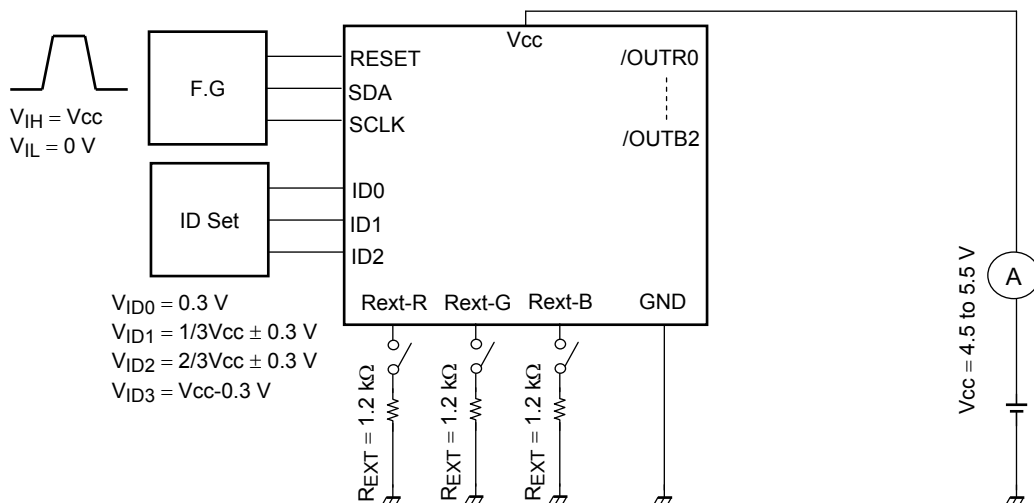
Test Circuit 4: Output Current (I$_{OUT1}$), Output Leakage Current (I$_{OZ}$) Output Current Variations (ΔI$_{OUT1}$/ΔI$_{OUT2}$), Current Variation with V$_{CC}$
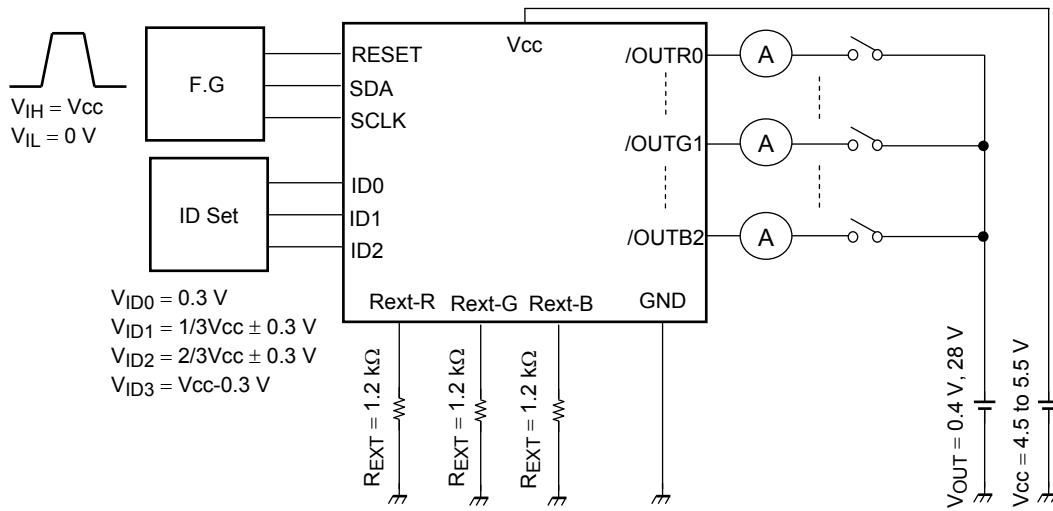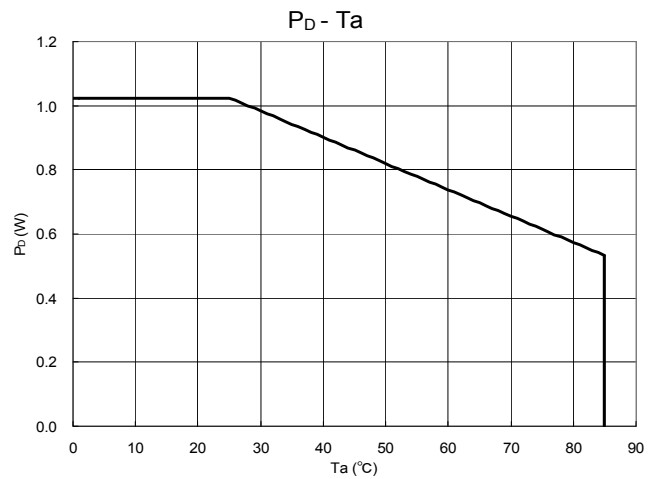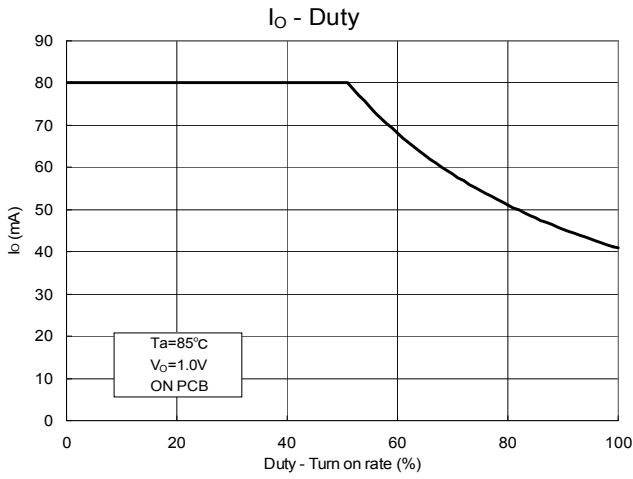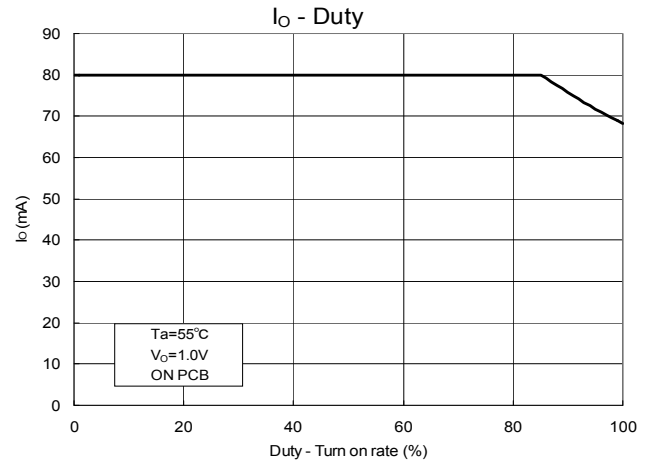

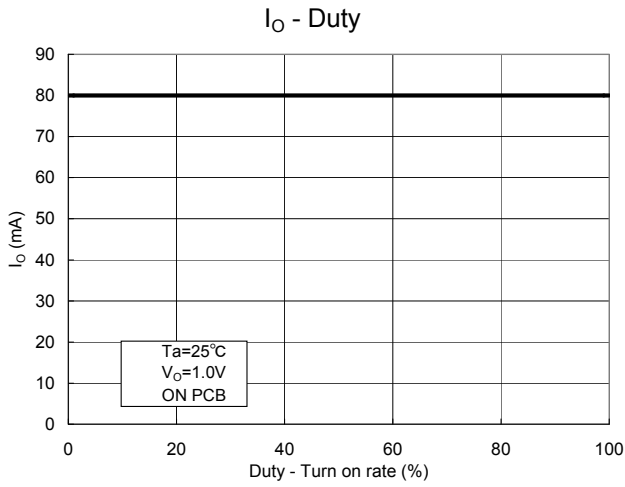Theoretical output current = 1.12 V / R$_{EXT}$ × 14.5
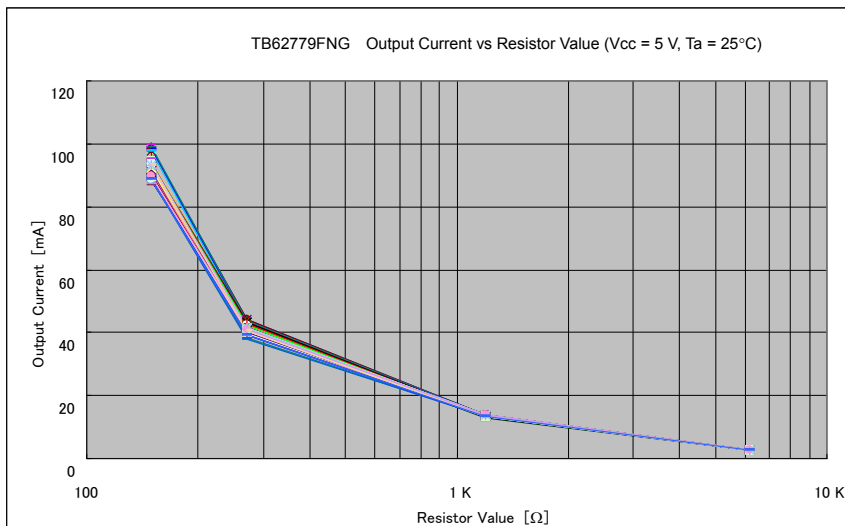
Test Circuit 5: Switching Characteristics

16. Output Current vs. Derating (lighting rate) Graph

PCB Conditions: 76.2 × 114.3 × 1.6 mm, Cu = 30%, 35-μm Thick, SEMI-Compliant
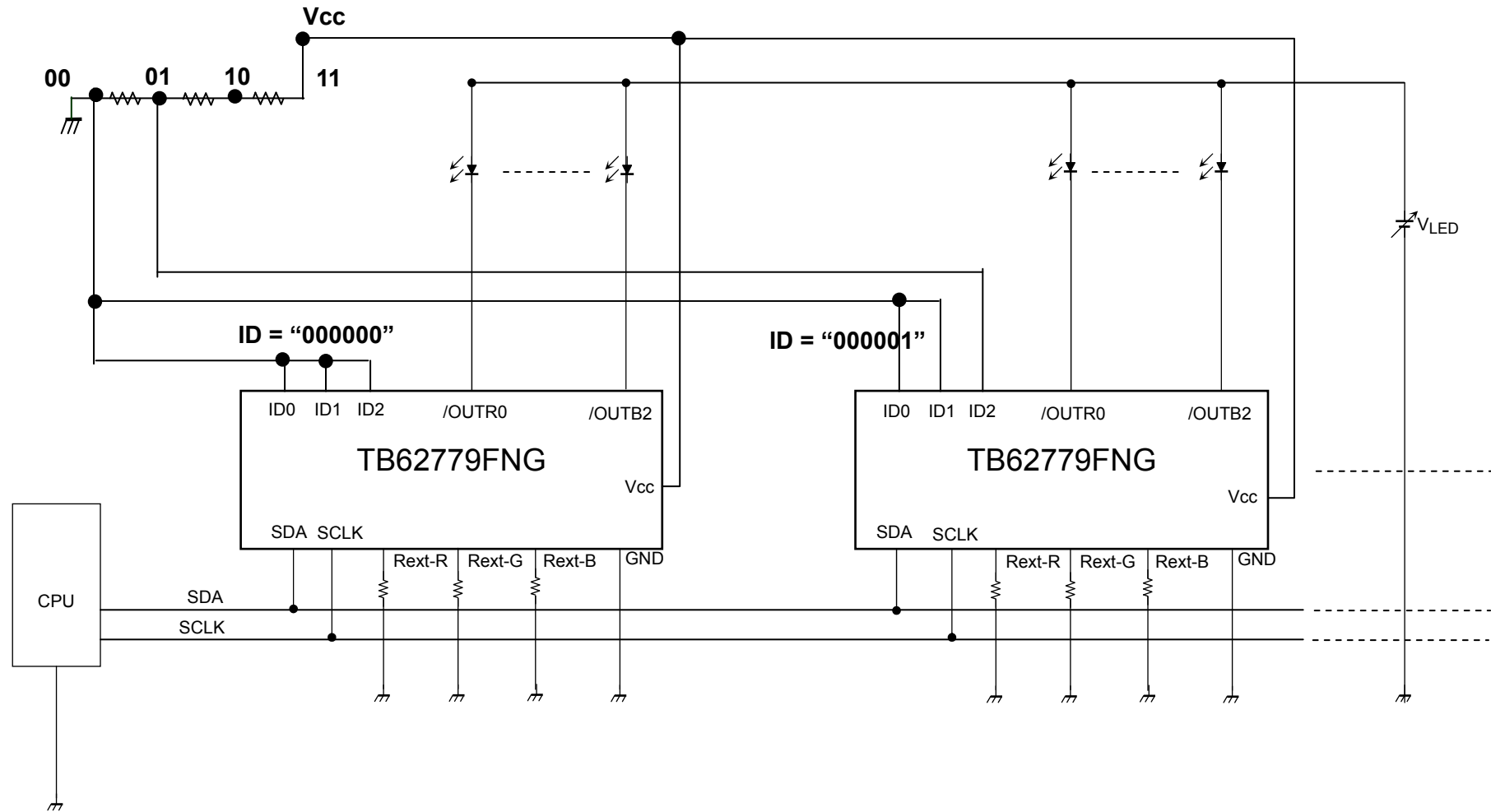A pulse width of 25 ms or more is considered to be a DC current.

I_O - Duty

Ta=25℃
V_O=1.0V
ON PCB

I_O - Duty

Ta=55℃
V_O=1.0V
ON PCB

I_O - Duty

Ta=85℃
V_O=1.0V
ON PCB

P_D - Ta

Output Current vs. External Resistor Value

TB62779FNG   Output Current vs Resistor Value (Vcc = 5 V, Ta = 25°C)
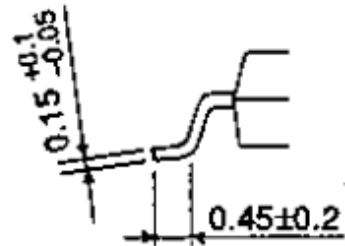
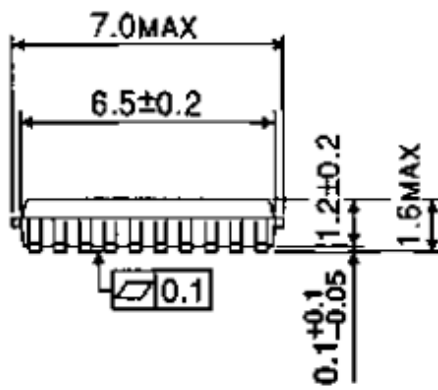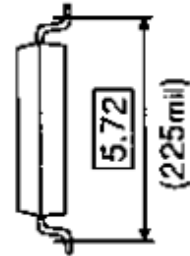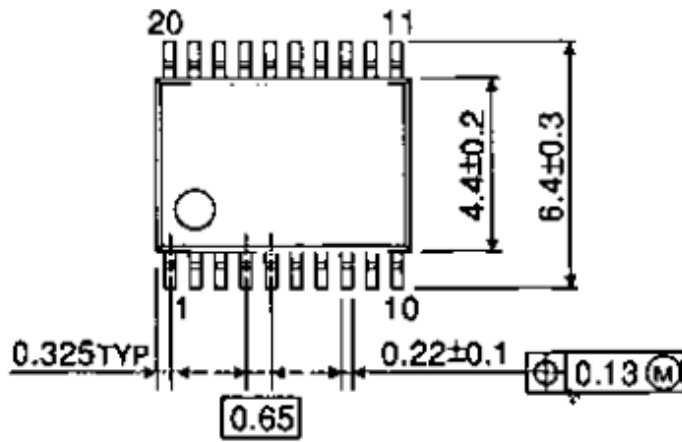Output current: 1.12 (V)/REXT(Ω)*14.5

17. Application Circuit Example 1

Package Dimensions

Unit : mm

Weight: 0.10 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Examples

The application examples provided in this data sheet are provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.
In providing these application examples, Toshiba does not grant the use of any industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause breakdown, damage or deterioration of the device, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the event of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly, or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow. Such a breakdown can lead to smoke or ignition. To minimize effects of a large current flow in the event of breakdown, fuse capacity, fusing time, insertion circuit location, and other such suitable settings are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current caused by inrush current at power ON or the negative current caused by the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
For ICs with built-in protection functions, use a stable power supply. An unstable power supply may cause the protection function to not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices incorrectly or in the wrong orientation.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause breakdown, damage or deterioration of the device, which may result in injury by explosion or combustion.
In addition, do not use any device that has had current applied to it while inserted incorrectly or in the wrong orientation even once.

(5) Carefully select power amp, regulator, or other external components (such as inputs and negative feedback capacitors) and load components (such as speakers),.
If there is a large amount of leakage current such as input or negative feedback capacitors, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Dissipation Design
In using an IC with large current flow such as a power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat dissipation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat dissipation on peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops, or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in your system design.

About solderability, following conditions were confirmed:

(1) Use of Sn-37Pb solder Bath
Solder bath temperature = 230°C
Dipping time = 5 seconds
The number of times = once
Use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
Solder bath temperature = 245°C
Dipping time = 5 seconds
The number of times = once
Use of R-type flux

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