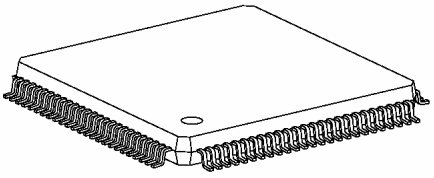
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90101FG

Y/C separation & Video Decoder

TC90101FG is a 1chip LSI of multi 3line comb and multi color decoder.
TC90101FG has 10bit ADC and 2channels 8bit ADC for analog Video signal interface and also include Y/C separation, color decode, and signal processing circuit.
The output interface of TC90101FG is a selectable for ITUR-601 & **656.**



LQFP100-P-1414-0.5C

Weight：0.65g(Typ)

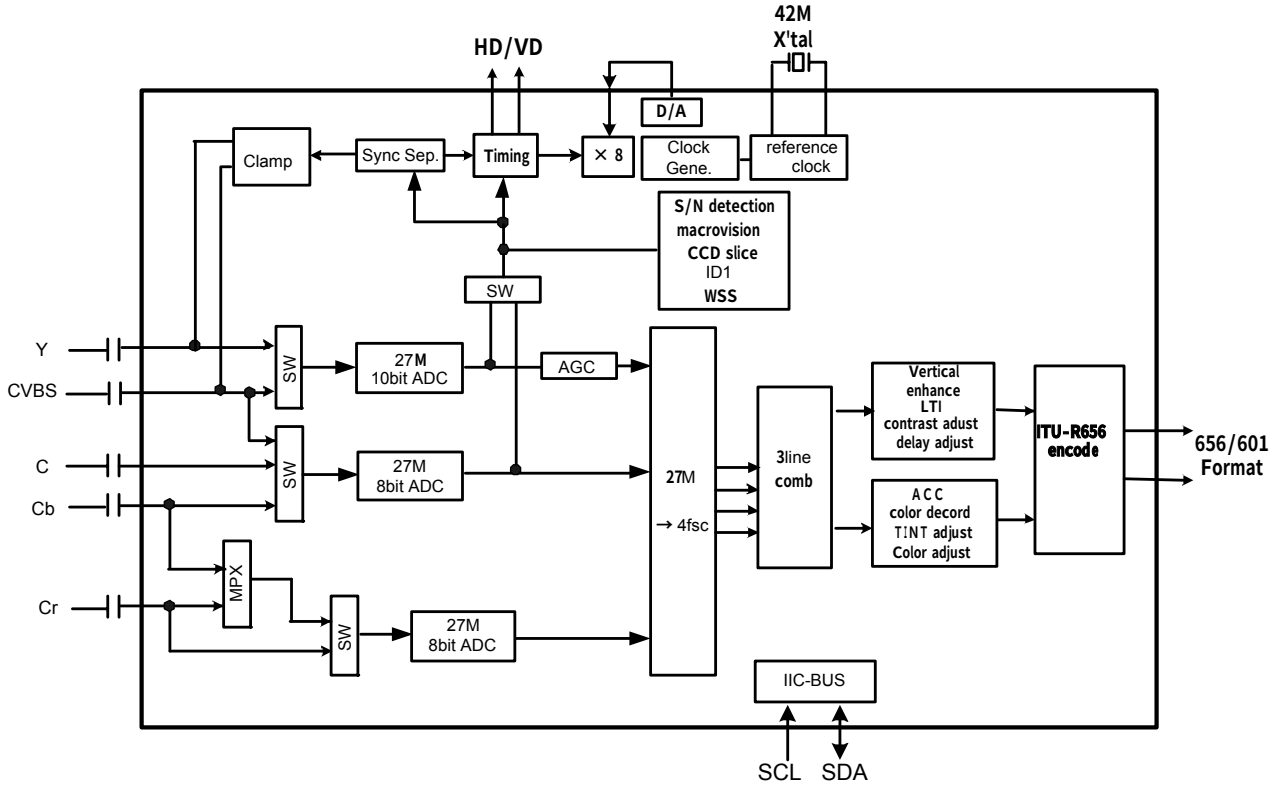
Featurs

- Multi color system
- Input I/F： CVBS, Y/C, YcbCr(1H & 525p/625p)
- Multi 3 line comb (SECAM: BPF)
- Component signal frequency detection (525i/525p/625i/625p)
- AGC circuit
- Output format : 656/601
- Picture improvement
  Y： Vertical enhance/LTI/Contrast/Setup adjust
  C： TOF/ACC/Color decode/color gain/CTI/offset adjust
- Noise level detection/ID1(525I & 525p) data slice/
  CCD data slice/WSS data slice/ Macrovision detection
- I^2C bus control
- Read data superposition on ITUR-656 output
- Package： LQFP 100 (0.5mm pitch)
- Power supply： 3.3 V， 2.5V，1.5V

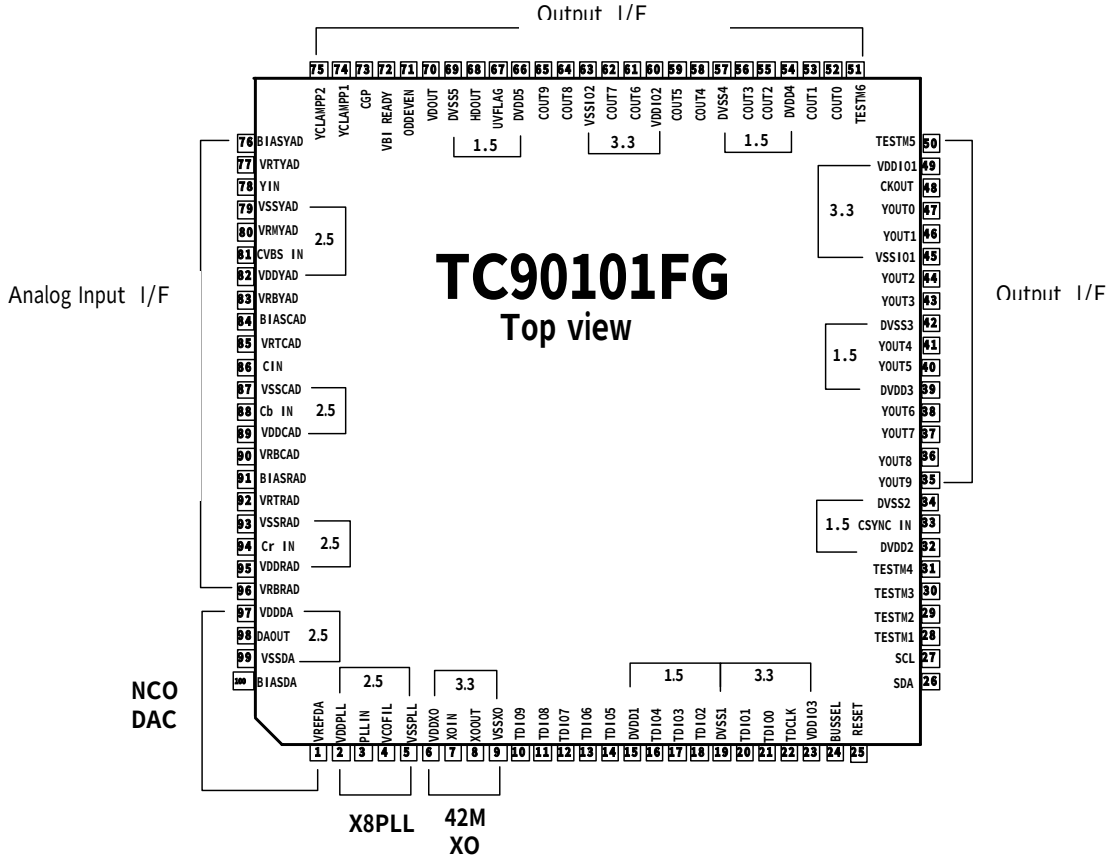
Version 4.2

(note1)These devices are easy to be damaged by high voltage or electric fields.
In regards to this, please handle with care.

1. Block Diagram



2. Pin Layout



3. Terminals discription

Pin No	Pin Name	Function ( ) : Condition at normal operation	Durable voltage (V)	I/O	Circuit (Analog or Digital)	DC at normal Oparation (V)	Analog signal Amplitude (Vp-p)
1	VREFDA	The reference voltage terminal of DAC	2.5	Bypass	Analog	1.5	-
2	VDDPLL	Power supply for X8 PLL circuit	2.5	VDD		2.5	-
3	PLLIN	Input terminal of X8 PLL circuit	2.5	IN		1.25	0.5～ VDDPLL*0.8
4	VCOFIL	Filter terminal for X8 PLL circuit	2.5	Bypass		1.2	-
5	VSSPLL	GND for X8 PLL circuit	0	GND		0	-
6	VDDXO	Power supply for X' tal OSC circuit	3.3	VDD	Digital	3.3	-
7	XOIN	X' tal OSC circuit input terminal	3.3	IN		-	-
8	XOOUT	X' tal OSC circuit output terminal	3.3	OUT		-	-
9	VSSXO	GND for X' tal OSC circuit	0	GND		0	-
10	TDIO9	Terminal for Test mode (Normaly Open)	3.3	I/O		-	-
11	TDIO8		3.3	I/O		-	-
12	TDIO7		3.3	I/O		-	-
13	TDIO6		3.3	I/O		-	-
14	TDIO5		3.3	I/O		-	-
15	DVDD1	Power supply for Logic circuit	1.5	VDD		1.5	-
16	TDIO4	Terminal for Test mode (Normaly Open)	3.3	I/O		-	-
17	TDIO3		3.3	I/O		-	-
18	TDIO2		3.3	I/O		-	-
19	DVSS1	GND for Logic circuit	0	GND		0	-
20	TDIO1	Terminal for Test mode (Normaly Open)	3.3	I/O		-	-
21	TDIO0		3.3	I/O		-	-
22	TDCLK		3.3	IN		-	-
23	VDDIO3	Power supply for I/O	3.3	VDD		3.3	-
24	BUSSEL	IICBUS slave address selection(L:B0、Hi:B2)	3.3	IN		-	-
25	RESET	Reset terminal (Low :Reset Hi :normal)	3.3	IN		3.3	-
26	SDA	IIC SDA terminal (5V input possible)	5	I/O		-	-
27	SCL	IIC SCL terminal (5V input possible)	5	IN		-	-
28	TESTM1	Terminal for Test mode (Normaly connect to GND)	3.3	IN		0	-
29	TESTM2		3.3	IN		0	-
30	TESTM3		3.3	IN		0	-
31	TESTM4		3.3	IN		0	-
32	DVDD2	Power supply for Logic circuit	1.5	VDD		1.5	-
33	CSYNCIN	External composite Sync signal input (In case not use external CSYNC, conect to GND)	5	IN		0	-
34	DVSS2	GND for Logic circuit	0	GND		0	-
35	YOUT9	Digital video port output 9 (MSB) (656/ 601 mode:YCbCr, 601:Y)	3.3	OUT		-	-
36	YOUT8	Digital video port output 8	3.3	OUT		-	-
37	YOUT7	Digital video port output 7	3.3	OUT		-	-
38	YOUT6	Digital video port output 6	3.3	OUT		-	-
39	DVDD3	Power supply for Logic circuit	1.5	VDD		1.5	-
40	YOUT5	Digital video port output 5	3.3	OUT		-	-
41	YOUT4	Digital video port output 4	3.3	OUT		-	-
42	DVSS3	GND for Logic circuit	0	GND		0	-
43	YOUT3	Digital video port output 3	3.3	OUT		-	-
44	YOUT2	Digital video port output 2	3.3	OUT		-	-
45	VSSIO1	GND for I/O	0	GND		0	-
46	YOUT1	Digital video port output 1 (In case 8bit output mode : fixed to Low)	3.3	OUT		-	-
47	YOUT0	Digital video port output 0 (In case 8bit output mode : fixed to Low)	3.3	OUT		-	-
48	CKOUT	System Clock output terminal for digital video signal output. 656 : 27MHz 601 : 13.5MHz	3.3	OUT		-	-
49	VDDIO1	Power supply for I/O	3.3	VDD		3.3	-
50	TESTM5	Terminal for Test mode (Normaly connect to GND)	3.3	IN		0	-

Pin No	Pin Name	Function ( ) : Condition at normal operation	Durable voltage (V)	I/O	Circuit (Analog or Digital)	DC at normal Oparation (V)	Analog signal Amplitude (Vp-p)
51	TESTM6	Terminal for Test mode (Normaly connect to GND)	3.3	IN	Digital	0	-
52	COUT0	CbCr digital video signal output (LSB) (656:COUT0-9 are fixed Low 601:CbCr) (In case 16bit mode: This terminal is fixed Low)	3.3	OUT		-	-
53	COUT1	CbCr digital video signal output (2'nd LSB) (In case 16bit mode: This terminal is fixed Low)	3.3	OUT		-	-
54	DVDD4	Power supply for Logic circuit	1.5	VDD		1.5	-
55	COUT2	CbCr digital video signal output 2	3.3	OUT		-	-
56	COUT3	CbCr digital video signal output 3	3.3	OUT		-	-
57	DVSS4	GND for Logic circuit	0	GND		0	-
58	COUT4	CbCr digital video signal output 4	3.3	OUT		-	-
59	COUT5	CbCr digital video signal output 5	3.3	OUT		-	-
60	VDDIO2	Power supply for I/O	3.3	VDD		3.3	-
61	COUT6	CbCr digital video signal output 6	3.3	OUT		-	-
62	COUT7	CbCr digital video signal output 7	3.3	OUT		-	-
63	VSSIO2	GND for I/O	0	GND		0	-
64	COUT8	CbCr digital video signal output 8	3.3	OUT		-	-
65	COUT9	CbCr digital video signal output 9 (MSB)	3.3	OUT		-	-
66	DVDD5	Power supply for Logic circuit	1.5	VDD		1.5	-
67	UVFLAG	Reference timing pulse for multiplexed Cb/Cr signal	3.3	OUT		-	-
68	HDOUT	Horizontal reference timing pulse	3.3	OUT		-	-
69	DVSS5	GND for Logic circuit	0	GND		0	-
70	VDOUT	Vertical reference timing pulse	3.3	OUT		-	-
71	ODD/EVEN	Field index output	3.3	OUT		-	-
72	VBIREADY	Reference timing pulse of IIC read for VBI data slice Function (Hi level at 23 line and 286 line)	3.3	OUT		-	-
73	CGP	Clamp gate timing pulse	3.3	OUT		-	-
74	YCLAMPP1	Clamp signal output for CVBSIN	3.3	OUT		-	-
75	YCLAMPP2	Clamp signal output for YIN	3.3	OUT		-	-
76	BIASYAD	Bias terminal for internal 10bit ADC	2.5	Bypass	Analog	0.8	-
77	VRTYAD	Reference top voltage terminal for internal 10bit ADC	2.5	Bypass		1.75	-
78	YIN	Analog Y signal input terminal (10bit ADC)	2.5	IN		-	VDDYADx0.4
79	VSSYAD	GND for internal 10bit ADC	0	GND		0	-
80	VRMYAD	The reference middle voltage terminal for Internal 10bit ADC	2.5	Bypass		1.25	-
81	CVBSIN	Analog CVBS signal input terminal (10bit ADC)	2.5	IN		-	VDDYADx0.4
82	VDDYAD	Power supply for internal 10bit ADC	2.5	VDD		2.5	-
83	VRBYAD	Reference bottom voltage terminal for internal 10bit ADC	2.5	Bypass		0.75	-
84	BIASCAD	Bias terminal for internal 8bit C/Cb-ADC	2.5	Bypass		0.8	-
85	VRTCAD	Reference top voltage terminal for internal 8bit C/Cb-ADC	2.5	Bypass		1.75	
86	CIN	Analog C signal input terminal (8bit ADC)	2.5	IN		1.25	VDDCADx0.4
87	VSSCAD	GND for internal 8bit C/Cb-ADC	0	GND		0	-
88	CbIN	Analog Cb signal input terminal (8bit ADC)	2.5	IN		-	VDDCADx0.4
89	VDDCAD	Power supply for internal 8bit C/Cb-ADC	2.5	VDD		2.5	-
90	VRBCAD	Reference bottom voltage terminal for 8bit C/Cb-ADC	2.5	Bypass		0.75	
91	BIASRAD	Bias terminal for internal 8bit Cr-ADC	2.5	Bypass		0.8	-
92	VRTRAD	Reference top voltage terminal for 8bit Cr-ADC	2.5	Bypass		1.75	-
93	VSSRAD	GND for internal 8bit Cr-ADC	0	GND		0	-
94	CrIN	Analog Cb signal input terminal (8bit ADC)	2.5	IN		-	VDDRADx0.4
95	VDDRAD	Power supply for internal 8bit Cr-ADC	2.5	VDD		2.5	-
96	VRBRAD	Reference bottom voltage terminal 8bit Cr-ADC	2.5	Bypass		0.75	-
97	VDDDA	Power supply for internal DAC of NCO	2.5	VDD		2.5	-
98	DAOUT	Output terminal of DAC of NCO	2.5	OUT		2	VDDDA-VDDDA*0.6
99	VSSDA	GND for internal DAC of NCO	0	GND		0	-
100	BIASDA	Bias terminal for internal DAC	2.5	Bypass		0.9	-

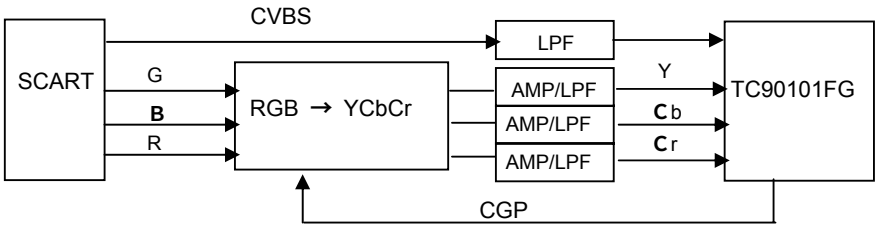
(Note) Please place the capacitor at near the terminal.
Please take care Surge for the IIC I/F terminals.

4. Functional Description

4.1 General Description

TC90101FG is a Video decoder device for multi color system (525i. 625i).
TC90101FG also has a through mode and sync processing for 525p & 625p component signal.

1.TC90101FG has input interface for CVBS, S-Video, YCbCr. For RGB signal it needs some external circuit as below.



2. Automatic clamp control circuit.
3. Multi 3line comb filter.
4. Multi color decoder and sync processing.
5. Color system detection circuit. (Selectable auto detection and manual setting.)
   Result of color system dtection can be read via IIC.
6. Frequncy detection circuit for 525i/525p/625i/625p for component signal.
7. AGC circuit circuit at after stage of ADC.
8. Picture processing circuit for CVBS, S-Video, 525i/625I component signal.
9. Selectable ITUR-601, ITUR-656 output interface.
10. VBI data slice function (525i ID-1/525p ID-1/ CCD/ WSS). It can be read via IIC.
11. Macrovision detection circuit.
12. Noise level detection circuit.
13. Superposition function for IIC read data on ITUR-656 ouitput.

4.2 Fanctional Discription

1. Clock System
   TC90101FG has a digital VCO circuit which uses 42MHz free run X'tal OSC.
   Digital VCO circuit generates 27MHz fH clock for input stage, 4fsc clock for internal comb block And 13.5MHz for output stage.

2.0 Input interface

Input signal	Pin name	Terminal
CVBS	CVBS IN	81
Y(S-Video & Component)	YIN	78
C(S-Video & Component)	CIN	86
Cb	Cb IN	88
Cr	Cr IN	94

2.1 Selection input signal
Input signal can be set via INSEL at sub address 00hex.
INSEL : 00 : CVBS 01: S-Video 10: YCbCr 11: SCART(**)
(*) : it's not available to input RGB signal dilectlly.
It's needs RGB to YCbCr conversion circuit at the before stage of TC90101FG.
In this mode CVBS must be inputted to CVBIN for sync processing, noise dtection and VBI data slice.

2.2 Input signal amplitude

TC90101FG has a 10bit ADC for CVBS & Y signal and 2ch 8bit ADC for C & Cb/Cr.
The Dynamic range of ADC is desgned as AVDD *0.4 (Normally 1Vpp at AVDD = 2.5V).
The recomemdation amplitude of the input signal : 0.7Vpp at 140IRE (CVBS/Y) . refer to fig-1.
* in case of AGC ON, recommendation input signal amplitude is 0.6Vpp (140IRE).
(AGC control range is from - 6dB to +3dB.)

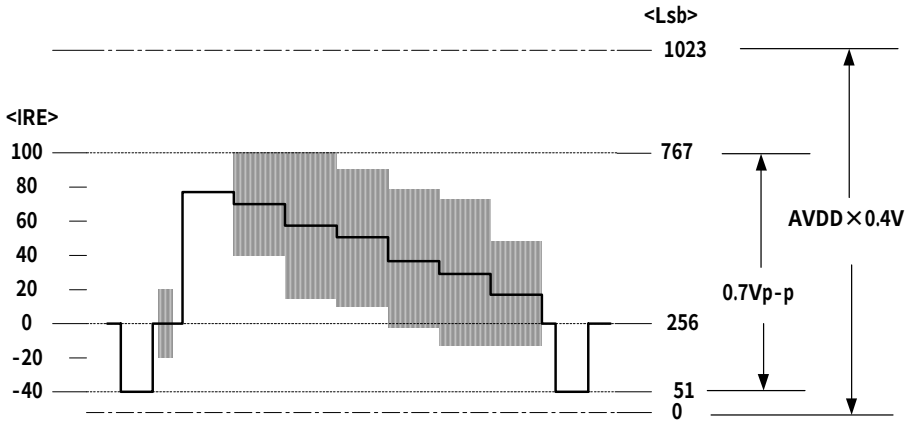


Fig-1. Amlitude of CVBS input

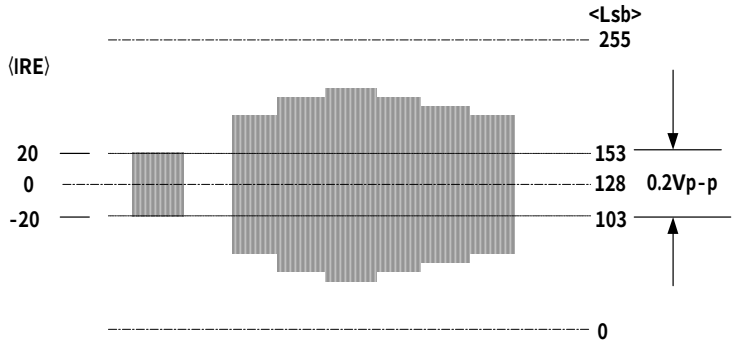


Fig-2. Amlitude of C input

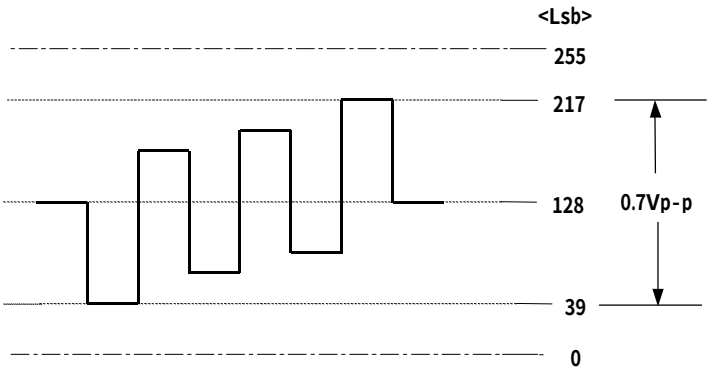


Fig-3. Amlitude of base band C signal input

The amplitude of input signal for 10bit ADC is 0.7Vp-p as 140IRE. in case of C signal for S-video.
The amplitude of input signal for C ADC is 0.2Vp-p as 40IRE. (Refer to Fig-2.)
The amplitude of input signal for Cb/Cr is 0.7Vp-p as 100% level. (Refer to Fig-3.) (VDD = 2.5V)
Input signal vs output signal level

Input signal	Input signal amplitude: Vp-p (※)	Ouput signal level (LSB)
CVBS	0.7Vp-p (500mVp-p)	16-235(pedestal to white 100%) (8bit mode)
Y	0.7Vp-p (500mVp-p)	16-235(pedestal to white 100%) (8bit mode)
C	0.2Vp-p (Burst)	16-240 (8bit mode)
Cb	0.7Vp-p (100% color)	16-240 (8bit mode)
Cr	0.7Vp-p (100% color)	16-240 (8bit mode)

※ Input signal amplitude: For CVBS and Y, it means 100% level (140IRE).
(500mVp-p: pedestal to white 100%.)
Cb/Cr, it means 100% color bar Signal.
Notice: These amplitude of output signal have done by initial value of IIC registers related with gain.

3. Clamping
The clam control circuit controls the corect clamping for input signals.
TC90101FG has a feed back clamp for H-Sync portion of CVBS/Y input signal to clamp 256LSB(10bit unit).
It is selectable to use the 2 types of the feed back clamp (internal circuit or external circuit) via IIC bus. (FBCLMPEX at sub address 03 hex.)
In case use external, the clamp signal from YCLAMP1,YCLAMP2(pin 74,75) to be connected with input Terminals. (refer to application circuit.)
For C signal, it is biased to 128 LSB. For Cb and Cr signal, it is used keed clamping control to 128 LSB.

Input mode	Input signal	Pin number	ADC	Clamping function	Comment
CVBS	CVBS	81	10bit	Feed back clamp	Time constant is selectable for internalClamping mode via BUS FBCLMOD atSub address 32hex.
S- Video/ YCbCr	Y	78	10bit		
	C	86	8bit	–	Biased to 128LSB
	Cb/Cr	88/94	8bit	Keed clamp	
CVBS+ YCbCr (1H)	CVBS	81	8bit	Sync chip clamp	
	Y	78	10bit	Feed back clamp	
	Cb/Cr	88/94	8bit(MPX)	Keed clamp	

4. TV system detection for CVBS and S- Video input
TC90101FG has 4 types of detection mode and it is selectable via AUTDET at sub address 00hex.

AUTODET	Mode	Fsc detection	Commemt
00	Manual setting	-	TV system is set via TV0 – TV3 at sub address 00hex.
01	EU	4.4336MHz 3.57954MHz	Priority : 4.43MHz PAL→ NTSC→ SECAM (it's not available to detect 3.58MHz PAL signal.)
10	South America	3.57954MHz 3.5756MHz 3.5820MHz	Priority : 3.58MHz PAL→ 3.58MHz NTSC (it's not available to detect 4.43MHz fsc signal.)
11	Full multi	4.4336MHz 3.57954MHz 3.5756MHz 3.5820MHz	Priority : PAL→ NTSC→ SECAM

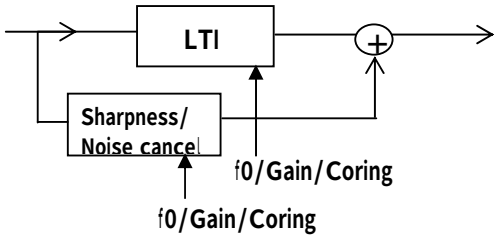
There is not priority for 50Hz/60Hz(Vertical frequency) detection.
VD output (pin 70) is controled via VD.DET at sub address 23hex.
[00] : free run.
[01] : fixed mode when it detects no signal (The frequency of VDOUT is depends on TVM2.)
[10]: Fixed Frequency at Manual setting mode.
[11]: VDOUT is depends on TVM2 at all of TV system detection mode.

5. H/V Sync processing
TC90101FG has H/V sync separation circuit and regenrates HD/VD pulse.
The phase and width of HD/VD pulse are controled via THRHV at sub address 22hex.
[0] : 656 format.
[1] : Syncronized with input signal.

6. D2 signal (525p/525p component) processing
TC90101FG has D1 and D2 detection circuit and Sync processing for D2 signal.
D2 signal is converted as 4:2:2 digital signal by internal ADC. (Sampling rate of Y ADC is 27MHz.)
ID-1 data slice for 525p is available but It's not available to use picture implrovement function and Noise level detection, (The sliced data of ID-1 can be read via IIC.)

7. T.O.F (Take Off filter)
TC90101FG has Take Off filiter which is in front of color decoder.
Characteristic of T.O.F is set via TOF at sub address 0C hex.
[000] : Off [001] : type 1- [111] : type 7
(Type 1 : BPF.)

8. Y process
a) Vertical enhancement : adjustable coring, gain, and non-linear performance
b) LTI function
The performance of this function is controlled via Iregisters at 04 and 05 hex.
f0 : 3.3MHz / 2.2MHz
Coring : 0.8IRE/1.6IRE/3.2IRE/6.4IRE
Gain : Off / 1/8 / 1/4 / 1/2
c) Sharpness
The performance of this function is controlled via Iregisters at 02 and 03 hex.
f0 : 4.2MHz / 3.3MHz
Coring : 0.8IRE/1.6IRE/3.2IRE/6.4IRE
Gain : -1/4 - Off - 1/2



d) Noise canceller
The performance of this function is controlled via Iregisters at 04 hex.
f0 : 4.2MHz / 3.3MHz (It uses same register with f0 of sharpness control.)
Coring : 0.8IRE/1.6IRE/3.2IRE/6.4IRE
Gain : -1/4 - Off - 1/2
e) Contrast
Control range : ×(1/2) - ×2.4
f) Brightness
it's effective at the periode of picture signal portion.
Control range : -128LSB - 128LSB (10bit unit)

9. C process

a) ACC control : A reference level is set up by register ACC LEVEL.
b) Killer control : sensitivity of killer is set via [BUS KILLV] at sub address 37 hex.
In case Killer detection, comb filter for Y becomes off.
c) HUE control : Hue control is available for CVBS and C signal of NTSC system.
Hue bias : 0 --- +45degree
Hue range : -45 degree --- +43.6degree
d) Sub color gain control
Amplitude of Cb and Cr signals are controlled via IIC.
Control range is –6dB --- +2.8dB

e) CTI function
f0 is selectable (1.7MHz/ 3.3MHz).
Coring level is selectable (0.4IRE/ 0.8IRE/ 1.6IRE/ 3.2IRE).
Gain is selectable (OFF/ x1/8 / x1/4 / x1/2).

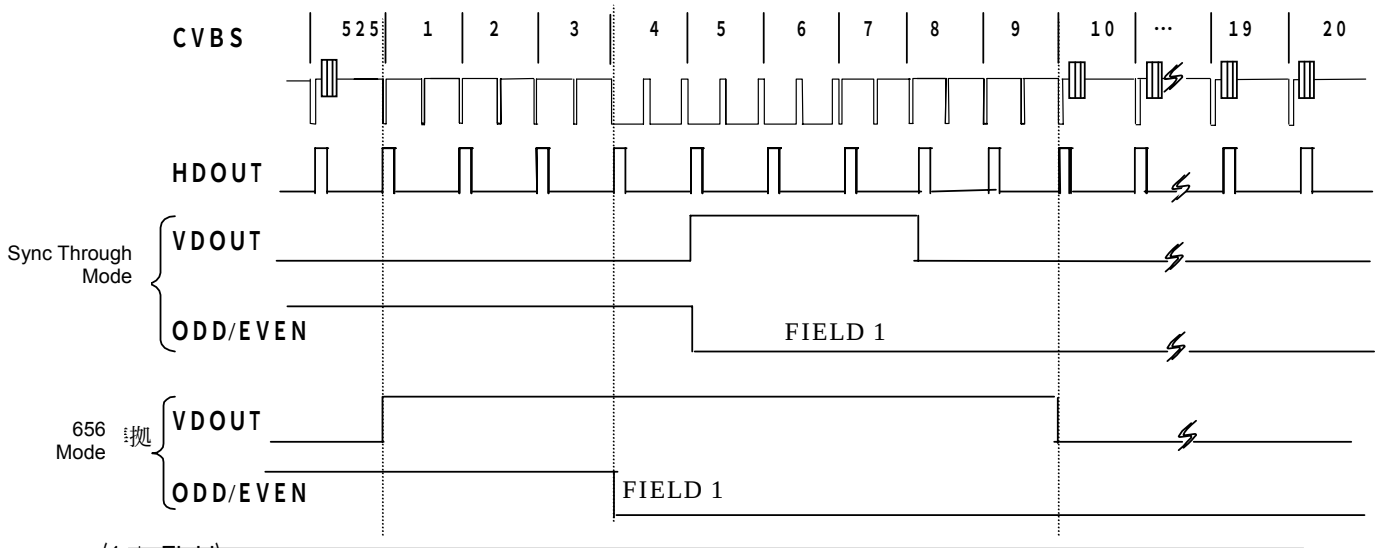
f) Offset control of the period of picture area
The DC level of the Cb and Cr signals are controlled via IIC independently.
Control range : -8LSB ---- +7LSB (10bit unit)

10. Output format
Output format (data format/clock/phase) is controlled via IIC Bus.
Y：The Pedestal level is 16LSB at 8bit output format and 64LSB at 10bit output format.
C：The signal level is 128LSB except for picture periode at 8bit output mode. (10bit mode: 512LSB)
The output format (656/601) is set via FORMATO (01h,D3) and the Dynamic range is set via OUTBITS(01h、D2)
Picture periode of Y output can be controlled by CLP (20h,D0).
CLP = [1] : the signal of under 16LSB (8bit mode) is sliced at 16LSB. (standard mode.)
CLP = [0] : It's available to output the signal of under 16LSB.
Normaly it must be set [1].

Output Terminals	Bit	Data rate	Comment
YOUT [0-9] (note)	10	13.5MHz/27MHz (601/656)	Y/YCbCr (601/656)
COUT [0-9] (note)	10	6.75MHz	Cb/Cr (CLK：13.5MHz)
UVFLAG	1	(13.5/2)MHz	Reference timing pulse for Cb/Cr Polarity : Cr = High(Initial value)
CKOUT (note)	1	13.5MHz/27MHz(/54MHz)	864fH/1728fH：625line source 858fH/1716fH：525line source Polarity : Reversal(Initial value)
HDOUT	1	fH	Re-generated HD
VDOUT	1	fV	Re- generated VD
ODDEVEN	1	fV	Field indication
VBIREADY	1	fV	Flag after VBI data slicing

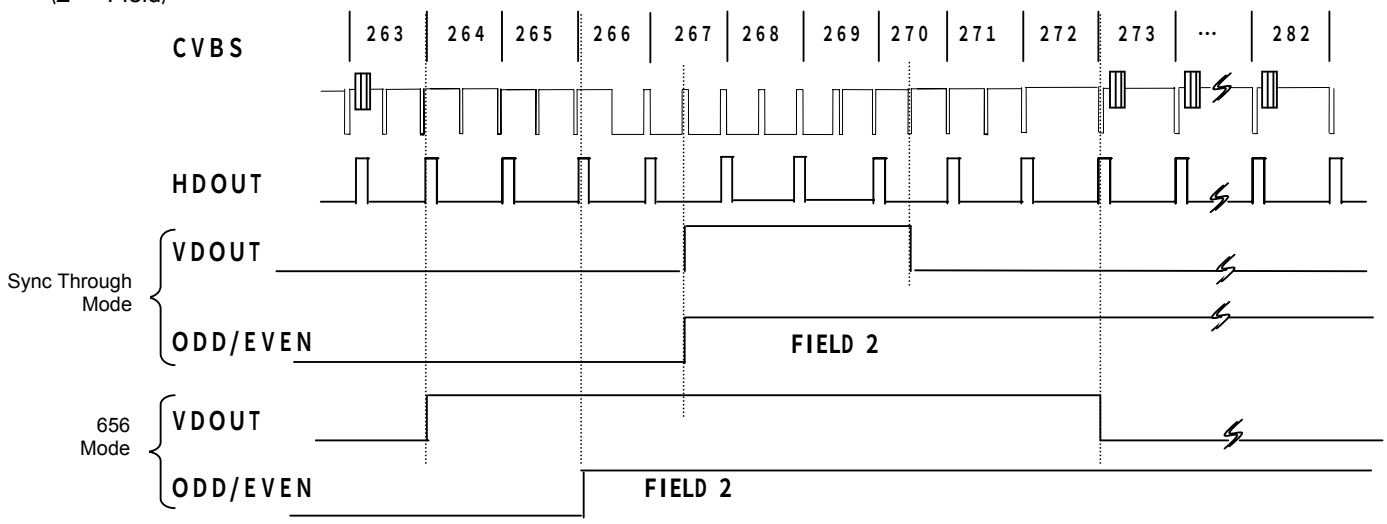
Note : YOUT, COUT, CKOUT has Hi impeadance mode. (01h,D1)

a) 525i/60Hz CVBS input mode



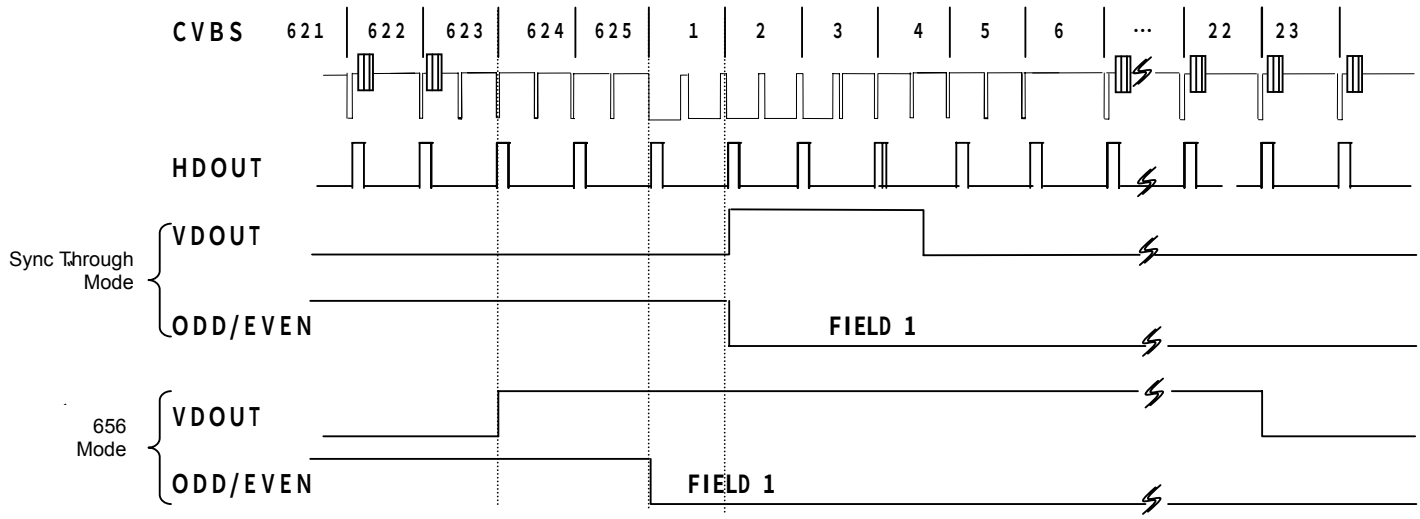
Selectable Sync through mode and 656 mode via THRHV at sub address 22hex.
656：Field1：Line 4 EAV
Field Blanking ; Start→ Line 1 EAV、 Finish→ Line 10 EAV
VBI READY：High level output → from Line 23 SAV to Line 24 EAV

(2nd Field)



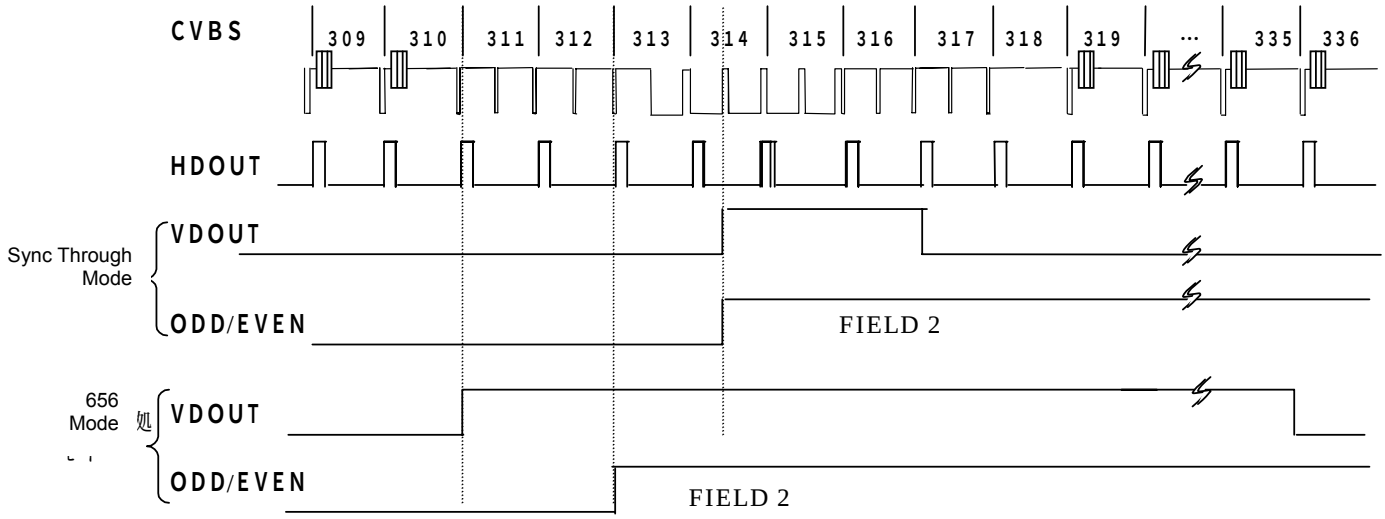
Selectable Sync through mode and 656 mode via THRHV at sub address 22hex.
656: Field 2: Line 266 EAV
Field Blanking ; Start→ Line 264 EAV, Finish→ Line 273 EAV
VBI READY: High level output → from Line 286 SAV to Line 287 EAV

b) 625/50Hz CVBS input mode
(1st, 3rd Field)



Selectable Sync through mode and 656 mode via THRHV at sub address 22hex.
656: Field1: Line 1 EAV
Field Blanking ; Start→ Line 624 EAV, Finish→ Line 23 EAV
VBI READY: High level output → from Line 64 SAV to Line 65 EAV

(2nd ,4th Field)



Selectable Sync through mode and 656 mode via THRHV at sub address 22hex.
656: Field 2: Line 313 EAV
Field Blanking ; Start→ Line 311 EAV、 Finish→ Line 336 EAV
VBI READY: High level output → from Line 377 SAV to Line 378 EAV

The pulse width of HD/VD output at Sync through mode

	525i	625i
HD pulse width	4.74 μs (128 cycle (unit: 27MHz clock)	
VD pulse width	3 H	2.5H

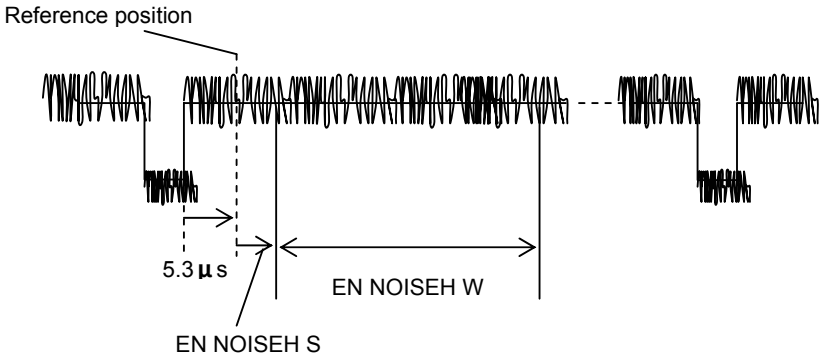
Notice: 656 output mode

The width of HD pulse is same as the period of between EAV and SAV.
In case of input non standard signal, it may not be above value.

11. Feature function

a) S/N detection (noise level detection)

Noise level detection is performed in the vertical blanking period. The result of noise level detection is stored to IIC read register and it is performed at every field.
The related write registers are as follows.
EN NOISEV S (sub address 1B hex) : Setup of start line for noise detection.
EN NOISEV W (sub address 1A hex) : Setup of the numbers of lines for noise detection .
EN NOISEH S (sub address 1A hex) : Setup of start position for noise detection at selected line.
EN NOISEH W(sub address 1A hex) : Setup of the period for noise detection at selected line.



b-1) Video ID (ID-1) data slice function for NTSC 525i signal (CVBS/S-video/Component)

ID-1 data slicing is performed at line 20 and 283 in the vertical blanking period.
The sliced data is stored to IIC read register and it is performed at every field.

b-2) Video ID (ID-1) data slice function for NTSC 525p signal (Component)

ID-1 data slicing is performed at line 41 in the vertical blanking period for NTSC 525p signal.
The sliced data is stored to IIC read register and it is performed at every vertical blanking periode.

c) CCD data slice function for US area(NTSC 525i signal (CVBS))

CCD data slicing is performed at line 21 and 284 in the vertical blanking period.
The sliced data is stored to IIC read register and it is performed at every field.
CRI detection, start bit detection and sliced data can be read via IIC bus.

d) WSS data slice function for EU area (PAL 625i signal (CVBS))

WSS data slicing is performed at line 23 and 336 in the vertical blanking period.
The sliced data is stored to IIC read register and it is performed at every field.
RUN-IN detection, start code detection and sliced data can be read via IIC bus.

e) Macrovision detection

TC90101FG can detect a pseudo sync, AGC pulse and color stripe.
The result of Macrovision detection can be read via IIC bus.

f) AGC function

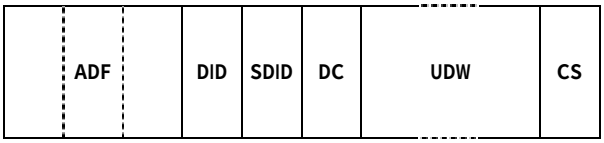
TC90101FG has an AGC function for CVBS and Y signal (S-video).
The related write registers are as follows.
PAGCON (sub address 2B hex) : Setup for PEAK AGC function.
PKLIM (sub address 2B hex) : Setup for limit level for PEAK AGC function.
SAGCON (sub address 2B hex) : Setup for SYNC AGC function.
(Through mode : Both registers (PAGCON & SAGCON) must be set [0].)

12. Insertion of IIC read data for output

TC90101FG has IIC read data insert mode for ITU-656 out put format.
It's also available for ITU-601 mode. These functions are based on ARIB STD-B6.

Selection of the line for IIC read data insertion is set via register at sub address 25hex and 26hex .

①25H D7：Insertion ON / OFF control for Horisontal blanking periode.
②25H D6：Insertion ON / OFF control for Vertical blanking periode.
③25H D5：Selection of insertion for ITU-601 mode
④25H D4-D0：Line selection of insertion for Horizontal blanking periode.
⑤26H D7-D4：Line selection of insertion for Vertical blanking periode.
TC90101FG uses "the 2nd form of ARIB "



ADF ：Auxiliary signal flag word (Fixation) 3 word
DID ：For discernment (set by register)
SDID ：For discernment 2nd data (set by register)
DC ：Data count code (the numbers of UDW word)
UDW ：User data word (main data)
CS ：Check sum (DID～UDW)

●ADF

ADF uses fixed value.

1) at the 10bit mode

000h	3FFh	3FFh

2) at the 8 bit mode

00h	FFh	FFh

●DID

DID has 4bit control registers (26H：D3-D0) .

1) For 10bit mode.

D9(MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0(LSB)
$\overline{D8}$	D[7:0]の偶数パリティビット	0	1	0	0	DID3	DID2	DID1	DID0

2) For 8bit mode.

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
0	0	0	0	DID3	DID2	0	0 固定

(Notice) DID[3:2]＝00 is not available when use 8bit mode.

●SDID

SDID has 4bit control registers (27H) .

1) For 10bit mode.

D9(MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0(LSB)
$\overline{D8}$	D[7:0]の偶数パリティビット	SDID7	SDID6	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0

2) For 8bit mode.

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
SDID7	SDID6	SDID5	SDID4	SDID3	SDID2	0	0

(Notice) DID[7:2]＝0000 00 is not available when use 8bit mode.

●DC

DC uses Fixed value.

1) For 10bit mode.

D9(MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0(LSB)
0	1	0	0	1	0	0	0	0	0

2) For 8bit mode.

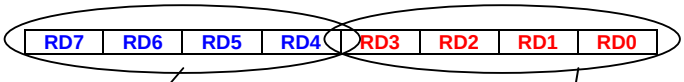
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
0	1	0	0	1	0	0	0

●UWD

<I2C Read Bus → 656 insertion specification.>

In case of 1byte Read register (RD[7:0]), it is superposed as below

・Read register 1 byte.



・656 insertion: 1st word.

D7	D6	D5	D4	D3	D2	D1	D0	D(-1)	D(-2)
0	1	RD7	RD6	RD5	RD4	0	0	0,0 (10bit mode)	

・656 insertion: 2nd word

D7	D6	D5	D4	D3	D2	D1	D0	D(-1)	D(-2)
0	0	RD3	RD2	RD1	RD0	1	0	0,0 (10bit mode)	

●CS

Check sum means total value of DID to UWD as below.

1) 10bit mode

It calculates total value of the 9bits low ranks of DID, SDID, DC and all of UDW.
MSB(D9) means $\overline{D8}$ of calculated valu. (it ignores the over flow.)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{D8}$	Total value of the 9bits low ranks of DID, SDID, DC and all of UDW. (it ignores the over flow.)								

2) 8bit mode

It calculates total value of the 7bits low ranks of DID, SDID, DC and all of UDW.
MSB(D7) means $\overline{D6}$ of calculated valu. (it ignores the over flow.)

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{D6}$	Total value of the 9bits low ranks of DID, SDID, DC and all of UDW.(it ignores the over flow.)						

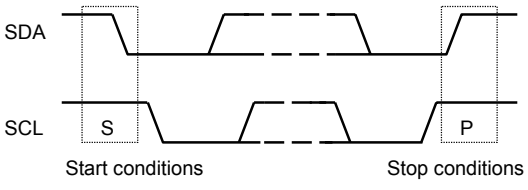
4. IIC BUS

TC90101FG has two slave address (B2 hexand B0hex). A slave address is chosen by BUSSEL Terminal which is pin 24. (BUSSEL=L：B0hex , BUSSEL=H：B2hex）。

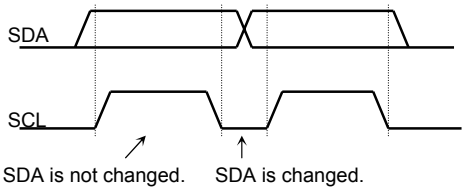
A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	1	0	0	X	X

• Data transmission format

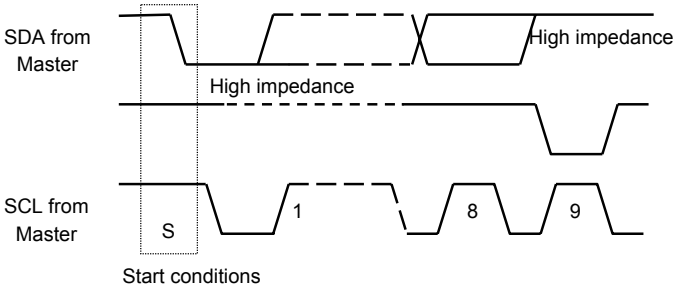
(1) Start condition, Stop condition



(2) Bit transmission



(3) Acknowledgement



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IIC BUS MAP

Sub	D7	D6	D5	D4	D3	D2	D1	D0
00H	INSEL		TVM3	TVM2	TVM1	TVM0	AUTODET	
	Input signal selection 00:CVBS 01:Y/C (S-Video) 10:YCbCr (D1or D2 Component) 11:CVBS+YCbCr(for SCART)		FSC selection 0:3.58MHz 1:4.43MHz 0000:NT358 0001:don't use 0010:PAL-M 0011:don't use	FV selection 0:60Hz 1:50Hz 0100:NT50 0101:don't use 0110:PAL-N 0111:don't use	PAL selection 0:Not PAL 1:PAL 1000:NT443 1001:SEC60 1010:PAL60 1011:don't use	SECAM selection 0:Not SECAM 1:SECAM 1100:don't use 1101:SECAM 1110:PAL 1111:don't use	Color system detection mode 00:Manual (00h-D5··D2 : Active) 01:EU mode 10:South America 11:Full detection mode	
INIT:03H								
01H	YCS Mode		SELCK		FORMATO	OUTBITS	HIZMODE	ADPWD
	3LYCS selection 0:3line 1:BPF	Fixed to [0]	Frequency of CKOUT(pin48) selection 10:54MHz 11:13.5MHz	00:13.5MHz 01:27MHz	0:Rec601 1:Rec656	0:8bit 1:10bit	setting of output 0:Normal 1:Open	Stand by mode 0:ADC-OFF 1:Normal
INIT:33H								
02H	V ENH GAIN		V ENH MAX POINT		V ENH SLICE LEVEL		FENH	PRENH
	V Enhance Gain 00:OFF 01:×1/8	10:×1/4 11:×1/2	V Enhance Non-linear 00: 6IRE 01: 9IRE	10:13IRE 11:16IRE	V Enhance Coring 00:OFF 01:0.8IRE	10:1.6IRE 11:2.3IRE	Sharpness fo 0:4.2MHz 1:3.3MHz	Pre Enhance 0:OFF 1:ON
INIT:34H								
03H	SHARPNESS GAIN				SHARPNESS SLICE LEVEL		FBCLAMP	FBCLMPEX
	Sharpness Gain Adjustment 1000:(don't use) 1001:(don't use) 1010:(don't use)	1100:-3/16 1101:-2/16 1110:-1/16	0000:1/16 0001:2/16 0010:3/16	0100:5/16 0101:6/16 0110:7/16	Shrpness coring 00:0.8IRE 01:1.6IRE	10:3.2IRE 11:6.4IRE	F/B CLAMP 0:Auto mode 1:Always ON	FB CLAMP mode 0: External 1: Internal
INIT:F0H	1011:-4/16	1111:OFF	0011:4/16	0111:8/16				
04H	NOISE CANCEL GAIN		FLTI	FCTI	SET DELAY			
	Gain Adjustment 00:OFF 01:×1/4	10:×1/2 11:×1	LTI fo 0:3.3MHz 1:2.2MHz	CTI fo 0:1.7MHz 1:3.4MHz	Cb and Cr Delay Adjustment 0000:-296ns ～ 1000:Center ～ 1111:259ns (37ns unit)			
INIT:08H								
05H	LTI GAIN		LTI SLICE LEVEL		CTI GAIN		CTI SLICE LEVEL	
	LTI Gain Adjustment 00:OFF 01:×1/8	10:×1/4 11:×1/2	LTI Coring 00:0.8IRE 01:1.6IRE	10:3.2IRE 11:6.4IRE	CTI Gain 00:OFF 01:×1/4	10:×1/2 11:×3/4	CTI Coring 00:0.4IRE 01:0.8IRE	10:1.6IRE 11:3.2IRE
INIT:00H								
06H	CONTRAST							
	Contrast Adjustment 00h:x1/2 ～ 40h:x1 ～ FFh:x2.4							
INIT:40H								
07H	BRIGHTNESS							
	Brightness Control 10000000:-128LSB ～ 00000000:0LSB ～ 01111111:+128LSB (10bit)							
INIT:00H								
08H	CR OUTPUT GAIN				CB OUTPUT GAIN			
	Cr Gain Adjustment 1000:×1/2 ～ 0000:×1 ～ 0111:×1.4				Cb Gain Adjustment 1000:×1/2 ～ 0000:×1 ～ 0111:×1.4			
INIT:00H								
09H	CR OUTPUT OFFSET				CB OUTPUT OFFSET			
	Cr Output Offset Adjustment 1000:-8LSB ～ 0000:0 ～ 0111:+7LSB (10bit)				Cb Output Offset Adjustment 1000:-8LSB ～ 0000:0 ～ 0111:+7LSB (10bit)			
INIT:00H								
0AH	HUE							FP_FIL
	HUE adjustment (for NTSC signal) 1000000:－45° ～ 0000000:0° ～ 0111111:＋43.6°							filter for Feed back 0:OFF 1:ON
INIT:01H								
0BH	HUE BIAS						CLPFOF	DCLAMP_VMASK
	HUE bias adjustment (Adjustment for the demodulation phase of R-Y (NTSC only) 000000:0° ～ 111111:＋45°						C Trap (burst) (for degital clamp) 0:OFF 1:ON	V mask of digital clamp 0:OFF 1:ON
INIT:03H								
0CH	Y INPUT OFFSET				BUS_DCOMTRP2	TOF		
	Offset adjustment for clamp Y input 1000:-31mV ～ 0000:0mV ～ 0111:+27mV				DCOMB out C Trap 0:OFF 1:ON	Take off filter selection 000:OFF , 001:BPF, 010:MIN ～ 111:MAX		
INIT:00H								
0DH								
INIT:00H								
0EH	Y ClampPulse_F			Y ClampPulse_W			DIGITAL Y CLAMP	
	Phase adjustment of digital clamp for Y 000:1.19μs ～ 111:3.26μs			Adjustment of Clamp widthfor Y digital clamp 000:0.9μs ～ 111:2.96μs			Time constant of Y digital clamp 00:OFF 10:mediam 01:small 11:large	
INIT:00H								
0FH	CR INPUT OFFSET				CB INPUT OFFSET			
	Offset adjustment for Cr input 1000:-31mV ～ 0000:0mV ～ 0111:+27mV				Offset adjustment for Cb input 1000:-31mV ～ 0000:0mV ～ 0111:+27mV			
INIT:00H								

* : Every blank register must be set “0”.

Sub	D7	D6	D5	D4	D3	D2	D1	D0
10H	CICLMPP_S				CICLMPP_W			
	Adjustment of input clamp phase for analog Cb/Cr				Adjustment of input clamp width for analog Cb/Cr			
INIT:00H	1000:-1.185μs ～ 0000:±0 ～ 0111:+1.04μs				1000:-1.185μs ～ 0000:±0 ～ 0111:+1.04μs			
11H	C ClampPulse_F			C ClampPulse_W			DIGITAL C CLAMP	
	Adjustment of digital clamp phase for Cb/Cr			Adjustment of digital clamp width for Cb/Cr			Time constant of Cb/Cr digital clamp	
	000:1.19μs ～ 111:3.26μs			000:0.9μs ～ 111:2.96μs			00:OFF	10:mediam
INIT:00H							01:small	11:large
12H	CONFIX	COLOR KILLER LEVEL			ACC LEVEL			
	Killer function	Adjustment the sensitivity of the killer detection			Adjustment ACC reference level			
	0:normal	000:Max ～ 111:Min			0000:Min ～ 1111:Max (Initial:1000)			
INIT:08H	1:killer off							
13H	DOT DIST		COMB+	1LINE DOT	COM443N	CGAIN		
	Reduse dot (Horizontal)				Comb selection	SECAM用 Y trap performance		
	00:OFF	10:x0.17	0:OFF	0:OFF	for 443NTSC	000:OFF ～ 111:×0.875 (Intial:011)		
	01:x0.16	11:x0.18	1:ON	1:ON	0:1H Comb			
INIT:5BH					1:2H Comb			
14H	EXTERNAL SYNC		SEPA LVL	SYNC TIP CLAMP1		VSEPLVL	VLMT	HHKIL
	Mode selection for external sync		Sync sepa. Level	Sync tip clamp mode for CVBS		V sepa mode	V sepa limit	AFC V mask
	00:OFF(internal)	10:CsyncL	0:30%	00:ON	10:AUTO1		0: 1/8	0:OFF
	01:CsyncH	11:VsyncH	1:40%	01:OFF	11:AUTO2	0:5/16	1: 1/16	1:ON
INIT:1CH						1:1/2		
15H	SHCTRL						MUTE	C MUTE
	Adjustment Horizontal phase reference						picture mute	Cb/Cr out mute
	100000:-4.74μs ～ 000000:±0μs ～ 011111:+4.46μs (1/6.75MHzステップ)						0:OFF	0:OFF
INIT:00H							1:ON	1:ON
16H	HDAMP1			HD GAIN1				
	Time constant 1 fpr H PLL(Phase difference: big)			Loop gain 1 for H PLL(Phase difference: big)				
INIT:4EH	000:large ～ 111:small			00000:small ～ 11111:large				
17H	HDAMP2			HDGAIN2				
	Time constant 2 fpr H PLL(Phase difference: middle)			Loop gain 1 for H PLL(Phase difference: middle)				
INIT:85H	000:large ～ 111:small			00000:small ～ 11111:large				
18H	HDAMP3			HDGAIN3				
	Time constant 3 fpr H PLL(Phase difference: small)			Loop gain 1 for H PLL(Phase difference: small)				
INIT:A6H	000:large ～ 111:small			00000:small ～ 11111:large				
19H	HGCON12				HGCON21			
	Threshold level at the phase diffrence large to middle				Threshold level at the phase diffrence middle to big			
INIT:48H	0000:OFF ～ 1111:High				0000:OFF ～ 1111:High			
1AH	EN_NOISEH_S			EN_NOISEH_W			EN_NOISEV_W	
	Adjustment start phase for noise detection			Adjustment the width for noise detection			Noise detection line numbers	
	000:32.2uS ～ 100:36.9uS ～ 111:40.5uS			000:9.4uS ～ 100:14.1uS ～ 111:17.7uS			00:1H	10:3H
INIT:90H							01:2H	11:4H
1BH	EN_NOISEV_S					FLOCK	VSRACH	
	Adjustment start line for noise detection					HPLL Gain at lock	fsc lock period	
	000:0H ～ 111:+15H					0:1/2	00:3V	01:4V
	60Hz:line 7 is as 0H					1:no change	10:5V	11:6V
INIT:00H	50Hz:line 4 is as 0H							
1CH	HDPH				VDPH			
	Adjustment horizontal phase for digital output				Adjustment Vertical phase for digital output			
INIT:00H	1000:-1.185uS ～ 0000:0uS ～ 1111:+1.04uS				0000:0H ～ 1111:+15H			
1DH	EN_PIXH_S				EN_PIXH_W			
	Adjustment start phase of horizontal signal processing				Adjustment width of horizontal signal processing			
INIT:00H	1000:-1.185μs ～ 0000:cemter ～ 0111:+1.04μs				1000:-1.185μs ～ 0000:center～ 0111:+1.04μs			
1EH	EN_PIXV_S				EN_PIXV_A	COMB KILL		
	Adjustment start phase of vertical signal processing					000:OFF	011:1～23H	110:1～26H
	0000:line 10 ～ 1111: line 25				0:Manual	001:1～21H	100:1～24H	111:Auto
INIT:07H					1:Auto	010:1～22H	101:1～25H	(60:22H,50:23H)
1FH	HBLK_S				HBLK_W			
	Adjustment start phase of horizontal BLK				Adjustment width of horizontal BLK			
INIT:00H	1000:-2.37μs ～ 0000:±0 ～ 0111:+2.27μs				1000:-2.37μs ～ 0000:±0 ～ 0111:+2.27μs			

* : Every blank register must be set “0”.

Sub	D7	D6	D5	D4	D3	D2	D1	D0
20H	BFP_S				VBIVAD[2:0]			CLP
	Adjustment start phase of burst gate 0000:center ～ 1111:+4.44μs (0.296μs step)				Adjustment the pase of VBI data slice 100:-4H～000:center ～111:3H			16LSB limit 0:OFF 1:ON
INIT:00H								
21H	VPHS			HDST			BYFOFF	BCFOFF
	Adjustment start phase of V at THRHV=1 110:384W 011:192W 000:0W 111:don't use 100:256W 001:64W (1W:27MHz) 101:320W 010:128W			Delay adjustment of HDOUT 10:40w 00:32w 11:44w 01:36w (1W:27MHz)			BSRY filter 0:ON 1:OFF	BSRC filter 0:ON 1:OFF
INIT:03H								
22H	PHPOLE	PVPOLE	PFPOLE	THRHV	INVCK	SEL_BLK	YOLEVEL	
	HDOUT polarity 0:active 1:negative	VDOUT polarity 0:active 1:negative	Field polarity 0:active 1:negative	H,V-OUT through 0: 656 1: through	CKOUT polarity 0:active 1:negative	V.BLK processing 0:normal 1:through	1/1.71875 Y output amplitude 0:1.71875 1:1.0	
INIT:18H								
23H		RBCHG	VD_DET		FIELD_DET	EXVDF		
		Cb/Cr phase 0:normal 1:change	Control VDOUT 00:Free run 01:Fixed mode 50/60 (on TVM2) 10:Fixed mode at MANUAL mode 11:Fixed mode for MANUAL mode & no sig at AUTO mode		Field Det. at no -sig. 0:AUTO 1:Fixed Low	Adjustment Ext VD phase 000:center 011:+5.96us 110:-3.97us 001:+1.99us 100:-7.94us 111:-1.99us 010:+3.97us 101:-5.96us		
INIT:00H								
24H	FLDTMSEL			VCTOLE	VCRESET	AFC_Cont	SEL_RDATA	
	Adjustment horizontal phase for field detection 000:-5.7μs 011:-13.2μs 110:-20.9μs 001:-8.2μs 100:-15.7μs 111:-23.2μs 010:-10.7μs 101:-18.4μs			V count 0:-H/8 ～ +H/4 1:±H/8	V count reset 0:OFF 1:ON	AFC control 0:OFF 1:ON	Start phase of IIC read registers 00:CDEC 01:CCD 10:ID1 11:WSS	
INIT:80H								
25H	AXD_HON	AXD_VON	AXD_SSEL	AXD_HSEL[4:0]				
	data insert of H 0:OFF 1:ON	data insert of V 0:OFF 1:ON	data incert for 601 format 0:incert to CbCr 1:incert to Y	Line number for incert data NTSC: 21/284 line + AXD_HSEL PAL時: 24/337 line + AXD_HSEL				
INIT:00H								
26H	AXD_VSEL[3:0]				DID[3:0]			
	Line number for incert data to field BLK NTSC: 1line+AXD_VSEL PAL: 1line+AXD_VSEL				For DID code			
INIT:00H								
27H	SDID[7:0]							
	For DID code							
INIT:00H								
28H	CSONTIM		CSOFTIM		strp_idg_wd[1]	strp_idg_wd[0]	strp_idg_lv[1]	strp_idg_lv[0]
	Adjustment histerisis for Color stripe detect ON 00:OFF 10:2.0s 01:1.0s 11:3.0s		Adjustment histerisis for Color stripe detect ON 00:OFF 10:1.0s 01:0.5s 11:1.4s		Adjustment mask periode for color stripe detection 00:10clk 10:20clk 01:15clk 11:30clk		Sensitivity of color stripe detection 00: Low ～ 11: High	
INIT:00H								
29H	CPSON		AGCWID	PSEWID		PSEMOD	PSLICEL	
	Color syripe detection 0:OFF 1:ON		Adjustment AGC detection periode 0:2.3～3.2μS(D1) 1: 2.0～3.5μS(D1) 0:1.1～1.7μS(D2) 1: 1.0～1.8μS(D2)	Adjustment Pseudo periodeof H detect 0:1.3～2.7μS(D1) 1: 1.0～3.0μS(D1) 0:0.9～1.3μS(D2) 1: 0.8～1.4μS(D2)		Pseudo H sync detection 0:OFF 1:ON	Slice level for pseudo H sync 00:20% 01:25% 10:40% 11:60%	
INIT:3AH								
2AH	PALPFON	PASEL		AGCMOD	ASLICEL		AGCHYS	
	LPF for AGC pulse & pseudo H sync detection 0:OFF 1:ON	AGC Hsync detection 0: after AGC 1:befor AGC		AGC pulse detection 0:OFF 1:ON	Adjustment of slice level for AGC pulse 00:60% 01:70% 10:80% 11:90%		Adjustment of histerisis time for AGC pulse detection 00:OFF 01:0.4s 10:0.7s 11:1.0s	
INIT:DAH								
2BH	PAGCON	PKLIM		AGCLPFON	PATTK		PSLP	
	Peak AGC 0:OFF 1:ON	Peak AGC limit level 00:105% 10:115% 01:110% 11:120%		fsc Trap Filter 0:OFF 1:ON	Adjustment Peak AGC Atack time 00: fast～11:slow		Sesitivity for Peak detection 00:big～11: small 01:1/4 11:1/8	
INIT:1AH								
2CH	SAGCON				SATTK		SSLP	
	Sync AGC 0:OFF 1:ON				Adjustment Sync AGC Atack time 00: fast～11:slow		Adjustment Sync AGC recovery time 00: fast～11:slow	
INIT:0FH								
2DH	CLPFON	CSLICES	CSLICEL		IRTIMS	CSTMOD	CCDMOD	
	LPF for CCD 0:OFF 1:ON	CCD slice function mode 0:Auto slice 1:fixed slice level	Adjustment fixed slice level 00:416LSB 01:496LSB 10:296LSB 11:336LSB		Phase for ID1 detection 0:±0.6μs 1:±1.2μs	sensitivity of CCD start bit 0:big 1:small	Field selection for CCD data slice 00:ODD 01:EVEN 10:Both Field 11:Both Field	
INIT:80H								
2EH	ILPFON	ISLICES	ISLICEL		IRWIDON	IEDGES	IPHASES	
	LPF for ID1 data slice 0:OFF 1:ON	ID1data slice function mode 0:Auto slice 1:fixed slice level	Adjustment fixed slice level for ID1 00:480LSB 01:592LSB 10:312LSB 11:368LSB		Det. for amplitude of ID1signal 0:80LSB 1:OFF	Phase adjustment forID1det. 0:Adaptive mode 1:Fixed mode	Adjustment the sampling pase for ID1 0:0 1:-1 2:+2 3:+1	
INIT:80H								
2FH	WLPFON	WSLICES	WSLICEL			WSTMOD	WSSMOD	
	LPF for WSS1 data slice 0:OFF 1:ON	WSS data slice mode 0:Adaptive 1:Fixed mode	Adjustment of the slice level for WSSdata 00:512LSB 01:640LSB 10:320LSB 11:384LSB			WSS SC det. Mode 0:sensive 1:Slow	Field selection for WSS data slice 00:ODD 01:EVEN 10:Both Field 11:Both Field	
INIT:88H								

* : Every blank register must be set “0”.

	D7	D6	D5	D4	D3	D2	D1	D0
30H	CCDDLY				ID1DLY			
	Phase adjustment for CCD data slice 0000:min ～ 1000:center ～ 1111:max 1STEP = 128fh				Phase adjustment for ID1 data slice 0000:min ～ 1000:center ～ 1111:max 1STEP = 128fh			
INIT:88H								
31H	WSSDLY				CDECEV1[4]	YADFILON	FILON1	FILON0
	Phase adjustment for WSS data slice 0000:min ～ 1000:center ～ 1111:max 1STEP = 128fh				fsc pull in performance 0:Nornal 1:Wide	13.5M trap for ADC 0：OFF 1：ON	IIR FILTER selection 0:FIL1 1:FIL2	IIR FILTER ON/OFF 0:OFF 1:ON
INIT:84H								
32H	PROG		BUS_FBCLMOD					
	D1/D2 detection 0：Manual 1：Auto det.	Manual set 0：D1 1：D2	Time constant of theInternal feed back clamping 00：Reference 01：Large 10：Small 11：Mid					
INIT:80H								
33H	MGAINSL	MGAIN						
	Manual Gain set for GCA 0：OFF 1：ON	Adjustment for GCA Gain						
INIT:00H								
34H	CGP_S				CGP_W			
	Adjustment start phase of output pulse of CGP 1000：-1.185μs ～ 0000：±0 ～ 0111：+1.04μs 0000：Sync center + 3.7μs				Adjustment pulse width of CGP 1000：-1.185μs ～ 0000：±0 ～ 0111：+1.04μs 0000：center (2μs)			
INIT:00H								
35H	DET4VAL						SYNC TIP CLAMP2	
	Threshold level for DET. 443 [1000:MIN 0000:CEN 0111:MAX]				0	1	Clamp control 00：ON 01：OFF	10：AUTO1 11：AUTO2
INIT:07H								
36H	CGPOUTM	BUS_DCOMTRP1						BUS_ENPIXOFF
	CGP OUT control 0:auto 1:forced ON	DCOMB OUT C Trap 0：OFF 1：ON						Mute 0：ON 1：OFF
INIT:00H								
37H	BUS_YNCCK	BUS_YNCLV	BUS_YNCGA	BUS_YNCON	BUS_CKILLLV	BUS_CNCLV	BUS_CNCGA	BUS_CNCON
	Y NOISE	Y NOISE LIM 0:4LSB 1:8LSB	Y NOISE GAIN 0:×1/2 1:×1	Y NOISE 0:OFF 1:ON	CKILL Gain 0:Center 1:+3dB	C NOISE LIM 0:4LSB 1:8LSB	C NOISE GAIN 0:×1/2 1:×1	C NOISE 0:OFF 1:ON
INIT:00H								

* : Every blank register must be set “0”.

IIC BUS Read Data

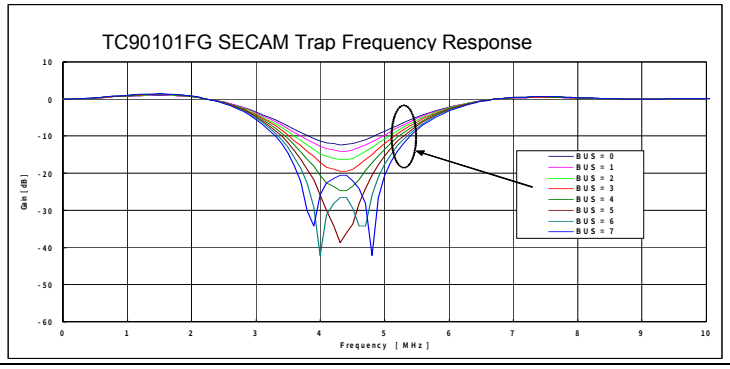
Sub	D7	D6	D5	D4	D3	D2	D1	D0
A-1	DET50 Field Frequency 0:60Hz 1:50Hz	NOSIG Signal det. 0:Signal det. 1:no signal	NOVP V-Sync Sep 0:V sig det 1:no V sig	FIELD Field indication 0:ODD 1:EVEN	UNLOCK HPLL for inpit sig 0:LOCK 1:UNLOCK	H/VSTD H-V std. det. 0:std. 1:non-std.	0	progressive D1/D2 det. 0:D1 1:D2
A-2	DET443 4.43MHz det. 0:non 1:Det.	PALDET PAL det. 0:non 1:Det.	SECAMDET SECAM det. 0:non 1:Det.	FSC_SEL fsc detection 00:3.579545MHz 01:3.575611MHz 10:3.582056MHz 11:4.433MHz		CKILL Killer det. 0:Color 1:White&black	0	FSCLOCK fsc lock det. 0:unlock 1:lock
A-3	NOISE_OUT7 (MSB)	NOISE_OUT6	NOISE_OUT5	NOISE_OUT4 S/N detection 0000_0000:Strong signal → 1111_1111:Weak signal	NOISE_OUT3	NOISE_OUT2	NOISE_OUT1	NOISE_OUT0 (LSB)
A-4	H_Cont [7] 10000000 : Min	H_Cont [6]	H_Cont [5]	H_Cont [4] information of H counter numbers for 1V periode 00000000 : Typ	H_Cont [3]	H_Cont [2] 01111111 : Max	H_Cont [1]	H_Cont [0]
A-5	0固定	COLSTYPE Color stripe 0 : TYPE2 1:TYPE3	COLSDET Color stripe det. 0:non 1:det.	Color_S_DET Psuedo Sync det. 0:non 1:det.	AGC DET AGC Pulse det. 0:non 1:det.	0	0	0
B-1	IIR CCD[7] CCD CRI det. 0 : under 3ck 1 : upper then 3ck	IIR CCD[6] Start bit det. 0 : NG 1 : OK	IIR CCD[5] CCD sliced data (LSB)	IIR CCD[4]	IIR CCD[3]	IIR CCD[2]	IIR CCD[1]	IIR CCD[0]
B-2	IIR CCD[15]	IIR CCD[14]	IIR CCD[13]	IIR CCD[12] CCD sliced data	IIR CCD[11]	IIR CCD[10]	IIR CCD[9]	IIR CCD[8]
B-3	IIR CCD[23] CCD sliced data (MSB)	IIR CCD[22]	IIR CCD[21] Field information 0 : ODD 1 : EVEN	IIR CCD[20] Numbers of CRI (MSB)	IIR CCD[19]	IIR CCD[18]	IIR CCD[17] (LSB)	IIR CCD[16] 0
B-4	IIR CCD[31] (MSB)	IIR CCD[30]	IIR CCD[29]	IIR CCD[28] information of CCD slice level	IIR CCD[27]	IIR CCD[26]	IIR CCD[25]	IIR CCD[24] (LSB)
C-1	IIR ID1[7] Reference sig. det. 0:NG 1:OK	IIR ID1[6] CRC code det. 0:NG 1:OK	IIR ID1[5] WORD0(sliced data) (LSB)	IIR ID1[4]	IIR ID1[3] WORD1(sliced data)	IIR ID1[2]	IIR ID1[1]	IIR ID1[0]
C-2	IIR ID1[15]	IIR ID1[14]	IIR ID1[13]	IIR ID1[12] WORD2(sliced data)	IIR ID1[11]	IIR ID1[10]	IIR ID1[9]	IIR ID1[8]
C-3	IIR ID1[23]	IIR ID1[22]	IIR ID1[21]	IIR ID1[20] CRCC(sliced data)	IIR ID1[19]	IIR ID1[18]	IIR ID1[17] 0	IIR ID1[16] Field information 0:ODD 1:EVEN
C-4	IIR ID1[31] (MSB)	IIR ID1[30]	IIR ID1[29]	IIR ID1[28] information of ID1 slice level	IIR ID1[27]	IIR ID1[26]	IIR ID1[25]	IIR ID1[24] (LSB)
D-1	IIR_WSS[7] RUN-IN det. 0:NG 1:OK	IIR_WSS[6] START CODE det. 0:NG 1:OK	IIR_WSS[5] WSS(sliced data) (LSB)	IIR_WSS[4]	IIR_WSS[3]	IIR_WSS[2]	IIR_WSS[1]	IIR WSS[0]
D-2	IIR WSS[15]	IIR_WSS[14]	IIR_WSS[13]	IIR_WSS[12] WSS(sliced data)	IIR_WSS[11]	IIR_WSS[10]	IIR_WSS[9]	IIR_WSS[8] (MSB)
D-3	IIR_WSS[23] Bi phase det. 0:NG 1:OK	IIR_WSS[22] Field information 0:ODD 1:EVEN	IIR_WSS[21] (MSB)	IIR_WSS[20]	IIR_WSS[19] information of WSS slice level	IIR_WSS[18]	IIR_WSS[17]	IIR WSS[16] (LSB)

SEL_RDATA	IIC read data sequence
00h	A B C D
01h	B C A D
10h	C A B D
11h	D A B C

●Additional information about IIC registers.

BUS address	Function	Contents
00H : D7-D6	Input signal selection.	An input signal is chosen.
00H : D5-D2	Select TVM.	The TV-system is fixed forcibly. It uses when it is worked in the manual.
00H : D1-D0	Color system detection mode.	Setup Color system detection mode. Manual / Europeian / South American / Full auto detection.
01H : D7	Setup for YCS.	3-lineComb or BPF is chosen. 0: 3-line-Comb 1: B.P.F
01H : D5-D4	Select clock	Setup for an output clock frequency. Select "601 : 13.5MHz" or "656 : 27MHz".
01H : D3	Select OUTPUT FORMAT	Setup for an output format (601or656).
01H : D2	Select OUTBITS	Setup for an output bits range (8bit or 10bit).
01H : D1	Digital-Output Control	Each digital output terminals are controlled. 0 : Active 1 : OPEN (Because it becomes Hi Impedance, coexistence with other IC's is possible.)
01H : D0	ADC-Power Control	The control of the power supply for ADC. 0 : The power supply of ADC is turned off. 1 : Normal (It usually uses by this setup.)
02H : D7-D6	Set V Enhance Gain	Gain (off, 1/8, 1/4 and 1/2) is set up.
02H : D5-D4	Set V Enhance non-liner point.	Setup the characteristic of V-enhance gain for non- correlation Component. Choose it from 4 point
02H : D3-D2	Set V Enhance coring	Choose Coring(No response level).
02H : D1	Set "f0" of sharpness	Set f0 of Sharpness. It works with f0 of Noise-canceler as well together.
02H : D0	Select Pre-Enhance	Pre-Enhance makes it control the part Edgy of Sharpness.
03H : D7-D4	Adjustment Sharpness Gain.	Control the Gain of Sharpness. 1011 : -1/4 ～ 1111 : OFF ～ 0111 : 8/16 1000, 1001 and 1010 can't be used.
03H : D3-D2	Set Sharpness-coring -Level.	Choose Coring(No response level).
03H : D1	Set the Feed-Back CLAMP	Set the Feed-Back CLAMP. 0: Auto. It becomes a diode clamp when TC90101FG detects a non-signal. 1 : Feed-Back Clamp is active.
03H : D0	Change the Feed-Back CLAMP	Select Internal-Feed-Back or External-Feed-Back. 0: External mode (Pin74, 75 outputs clamp signal). 1: Internal mode (Pin74, 75 : Open). The time-constant for internal feedback clamp is set via BUS_FBCLMOD at sub address 32 hex.
04H : D7-D6	Set Noise canceler Gain	Set the Gain of NOISE-CANCEL.
04H : D5	Set LTI f0	Set the f0 of LTI.
04H : D4	Set CTI f0	Set the f0 of CTI.
04H : D3-D0	Cb & Cr delay adjust.	Fine tune for delay of Cb & Cr. Step is 37[ns] between -296ns～259ns. But step is 74[ns] at YCbCr input mode.
05H : D7-D6	LTI Gain adjustment	It set the Gain of LTI.
05H : D5-D4	LTI coring Level	It set the Coring(No response level) of LTI. Use after you confirm a picture.
05H : D3-D2	CTI Gain adjustment	It set the Gain of CTI.
05H : D1-D0	CTI coring Level	It set the Coring(No response level) of CTI.

BUS address	Function	Contents
06H：D7-D0	Contrast Adjustment	It set the Contrast. (Reference value: [01000000]) Variability is ×0.5～×2.4. (When use big value and inputs big amplitude signal, It takes place over range of internal circuit.)
07H：D7-D0	Brightness Adjustment	It set the Brightness. Variability is -128LSB ～ +128LSB.
08H：D7-D4	Cr Gain Adjustment	It set Gain of Cr. (Refrence value:[0000]) Variability is ×0.5～×1.4. (When use big value and inputs big amplitude signal, It takes place over range of internal circuit.)
08H：D3-D0	Cb Gain Adjustment	It set Gain of Cb. (Refrence value:[0000]) Variability is ×0.5～×1.4. (When use big value and inputs big amplitude signal, It takes place over range of internal circuit.)
09H：D7-D4	Cr Output OFFSET adjust.	Fine tune for offset of the Cr at output stage.
09H：D3-D0	Cb Output OFFSET adjust.	Fine tune for offset of the Cr at output stage.
0AH：D7-D1	HUE adjustment	HUE adjustment at the NTSC input mode. Variable is -45°-+43.6 °.
0AH：D0	Filter for feed-back	Setup BPF for feed-back-clamp. [1]:ON [0]:OFF Normaly It must be set [1].
0BH：D7-D2	HUE Bias adjustment	Fine tune HUE-Bias at the NTSC input mode. Variable is 0°～+45 ° .
0BH：D1	C Trap for dirital clamp.	It is C-Trap for Digital-clamp of Y. [1]:ON [0]:OFF Use [1] at the digital-clamp-mode.
0BH：D0	V-mask of digital clamp	Setup of the digital clamping at V-Blk period. [1]: Clamp OFF [0]: Clamp ON. It usually uses on [1].
0CH：D7-D4	Offset adjustment for clamp Y-input	Offset adjustment for Y signal at Analog-input. Use with 0[mV] when you use with digita-clamp.
0CH：D3	C-trap of D-COMB	Setup C-trap for Y at Digital-COMB-block. [1]: ON [0]: OFF. This setup can reduce Cross-color and beat.
0CH：D2-D0	Take off Filter select	Setup Take-off-Filter. Take-off-Filter is put in front of Decoder. 000：OFF、001：BPF、010～111：TOF (TOF1～TOF6) When BPF is set up, it can't get the effect of TOF.
0EH：D7-D5	Phase adjustment of Digital-clamp for Y.	Digital-clamp is put by input-Y-signal Adjustment of the phase of Digital-clamp-pulse for Y. Reference value:[011].The variable is about 0.3[μs] step.
0EH：D4-D2	Adjustment of clamp-width for Y-digital -clamp	Adjustment of the width of Digital-clamp-pulse for Y. Reference value: [011].Variable is about 0.3[μs] step.
0EH：D1-D0	Time constant of Y-Digital-clamp	It can select ON/OFF of Digital-clamp-Y. And adjustment of time constant of Digital-clamp-Y.
0FH：D7-D4	Offset adjustment for Cr-Input	Adjust the offset of the Cr at input by YCbCr signal. Use with 0[mv] at the time of Digital-clamp. Variable is -31[mV] ～ +27[mV].
0FH：D3-D0	Offset adjustment for Cb-Input	Adjust the offset of the Cb at input by YCbCr signal. Use [0000] at the Digital-clamp mode. Variable is -31[mV] ～ +27[mV].
10H：D7-D4	Adjustment of input clamp phase for Cb/Cr	Adjust the clamp-phase of Cb/Cr at YCbCr signals. It usually uses on BUS:[0000].

BUS address	Function	Contents
10H : D3-D0	Adjustment of input clamp width for Cb/Cr	Adjust the clamp pulse width of Cb/Cr at YCbCr signals. It usually uses on BUS:[0000].
11H : D7-D5	Adjustment of digital -clamp-Pulse-phase for C/Cb/Cr	Adjust the digital-clamp-phase for C/Cb/Cr. (S-Video/YCbCr inputs.) It usually uses on BUS:[011].
11H : D4-D2	Adjustment of digital Clamp-pulse-width for C/Cb/Cr	Fine tune the digital-clamp-pulse-width for C/Cb/Cr. (S-Video/YCbCr inputs.) It usually uses on BUS:[011].
11H : D1-D0	Time constant of C-Digital-clamp	This is adjustment of time constant of Digital-clamp-C. It can set ON/OFF and three-kinds.
12H : D7	Setup killer function	Setup color killer function. [0]: Active (normal) [1]: Killer become OFF always.
12H : D6-D4	Level of color-killer	Level of color-killer-ON is set up. [000]:killer sensitivity is max.[111]: killer sensitivity is minimum.
12H : D3-D0	ACC reference Level	Reference-level of ACC(auto color control) is set up. Level by ACC becomes smallest when it is set up in 000.
13H : D7-D6	Reduce H-dot	Setup of dot-reducer at the horizontal edge. When it is turned on, dot of the part of H is reduced.
13H : D5	Setup Comb+	It has an effect as below for PAL system. When the horizontal lines of the front and the rear have color and edge element,and the horizontal line of center has no color, it drops Y signal level for calculated result. Therefore it occurs dots of black in spite of white and gray picture.When COMB+ is on, it can decrease this noise. It usually uses ON, when PAL signal.
13H : D4	1 LINE DOT	Setup of 1LINE-DOT-improver in the YCS block. [1]:ON [0]:OFF It can reduce the dot,when only 1-line has a color signal.
13H : D3	443NTSC Comb control	Comb control in 443NTSC is changed. [1]:2H comb [0]:1H comb Cross-color will reduce when 2H-Comb is selected.
13H : D2-D0	SECAM Y trap setup	Setup Y-trap performance for SECAM. 

BUS address	Function	Contents
14H : D7-D6	Selection for external-sync	It select the input signal of Composite-SYNC-in of Pin-33. [00]: OFF(Internal) Pin33 must be connect to GND. [01]: External composite Sync mode (polarity: High) [10]: External composite Sync mode (polarity: Low) [11]: External V-Sync mode (polarity: High)
14H : D5	Sync Separation level	Level of Sync-sepa is set up. Initial value is [0]:30%.
14H : D4-D3	Sync-tip-clamp-mode for CVBS	It set the control of clamp. [00]: Sync tip clamp ON [01]: Sync tip clamp OFF [10]: AUTO1(Sync-tip-clamping becomes activity, When it detect non-signal or pedestal has a big difference. [11]: AUTO2 (Sync-tip-clamping becomes activity, When it detect non-signal.
14H : D2	Setup for V-sepa	Setup for V-sepa 0: Type 1 1: Type 2 (Type 2 is more effective than Type1.)
14H : D1	V-sepa limit	Limit of V-sepa is set up. V-sepa becomes easy, when it is set up in 1/16. But,Usually use with 0(1/8) .
14H : D0	Setup of Half-H-killer	It count Half-H at the V period. [0]: OFF (Initial value) [1]: ON (It is effective for top-curl problem of non-standard signal.(VCR trick mode etc‥)
15H : D7-D2	Horizontal phase reference	Reference-Horizontal-counter of internal is set up. This register is reference timing for all of internal function. Usually, it uses with 0[μs].
15H : D1	Picture MUTE	[0]: Normal [1]: Picture Mute ON
15H : D0	Cb and Cr MUTE	[0]: Normal [1]: Color signal Mute ON
16H : D7-D5	Time constant 1 for HPLL (Phase difference:big)	It is time-constant of PLL. It becomes active when the phase difference has big value. Reference value: [010]
16H : D4-D0	Loop Gain 1 for HPLL (Phase difference:big)	It is Loop-Gain of PLL. It becomes active when the phase difference has big value. Reference value: [01110]
17H : D7-D5	Time constant 2 for HPLL (Phase difference:middle)	It is time-constant of PLL. It becomes active when the phase difference has middle value. Reference value: [100]
17H : D4-D0	Loop Gain 2 for HPLL (Phase difference:middle)	It is Loop-Gain of PLL. It becomes active when the phase difference has middle value. Reference value: [01101]
18H : D7-D5	Time constant 3 for HPLL (Phase difference:small)	It is time-constant of PLL. It becomes active when the phase difference has small value. (it means under stable.) Reference value: [101]
18H : D4-D0	Loop Gain 3 for HPLL (Phase difference:small)	It is Loop-Gain of PLL. It becomes active when the phase difference has small value. Reference value: [00110]

BUS address	Function	Contents
19H : D7-D4	Threshold level at the phase difference big to middle	Threshold level that Phase-diffrent changes from Big to middle is set up. Recommendation value: [0100]
19H : D3-D0	Threshold level at the phase difference middle to big	Threshold level that Phase-diffrent changes from middle to Big is set up. Recommendation value: [01000]
1AH : D7-D5	Start phase for noise detection	The horizontal-start-phase of the detection of Noise is set up. "Point of 5.3μs from sync" is center.
1AH : D4-D2	Width for noise detection	The horizontal-width of the detection of Noise is set up. The amount of noise-detection changes by Width. When width is widened, detection sensitivity rises.
1AH : D1-D0	The number of horizontal lines which Noise is detected in	It is the numbers of lines which Noise is detected in. The number of line's can be set up from 1H to 4H.
1BH : D7-D4	Start line for Noise detection	The vertical start line of the Noise detection is set up. 60Hz : 7-lines as 0H.It is set up in 1 line unit. 50Hz : 4-lines as 0H.It is set up in 1 line unit.
1BH : D2	HPLL-Lock-Gain	The fsc Lock-Gain is set up. Usually used with 1/2.
1BH : D1-D0	fsc lock period	Lock-period of fsc is set up. Search-time becomes long, when it is set up ～6V. But, it is easy to pull in.
1CH : D7-D4	Horizontal phase for digital format	The position of EAV&SAV is set up. Usually, it uses with initial-value:0[us].
1CH : D3-D0	Vertical phase for digital format	V-phase of VD is set up when "H/V OUT through". Variability of V-phase is the 1H unit.
1DH : D7-D4	Start phase of Horizontal signal processing	The horizontal start phase of the picture-processing-period is set up. The picture-processing is set up with COMBKILL (1EH D2～D0).
1DH : D3-D0	Width of Horizontal signal processing	The horizontal width of the picture-processing-period is set up. The start reference is a horizontal start phase. Make adjustment after start-setup.
1EH : D7-D4	Start phase of vertical signal processing	The vertical start line of the picture-processing-period is set up.It becomes MUTE to the setup from the vertical start line.
1EH : D3	The setup of the vertical picture processing	AUTO or MANUAL is selected. MANUAL : It becomes the value that it is set up with 1EH(D7-D4). AUTO: 60Hz= from 10th line / 50Hz= from 23th line Picture-processing is started from each line.
1EH : D2-D0	Setup of COMBKILL period	The period of COMBKILL is set up. This period doesn't do picture processing. AUTO:60Hz=1～22H、50Hz=1～23H But, it is a mask period to 21H by the Y/C input of 60Hz and the YCbCr input of 60Hz.
1FH : D7-D4	Start phase of Horizontal BLK	The start phase of H-BLANK-PULSE is set up. Usually, it uses with initial-value:0[us].
1FH : D3-D0	Width of Horizontal BLK	The width of H-BLANK-PULSE is set up. Usually, it uses with initial-value:0[us].
20H : D7-D4	Start phase of burst gate	The start phase of BURST-GATE-PULSE is set up.

BUS address	Function	Contents
20H : D3-D1	Set line of VBI data slice	The line of VBI-data-slice is set up. Usually used with center. When it uses at the outside synchronism, it uses for the adjustment, when the phase of the outside VD-pulse and the input signal are shifted. VBI and Macrovision detection line move at the same time, too.
20H : D0	16LSB limit	It limit less than 16LSB at the Digital output. Use by ON, when you use with 601/656 output.
21H : D7-D5	Start phase of V at THR-V	The phase of VD is set up. Bus:111 can't be set up.
21H : D4-D3	Delay adjustment of HD-OUT	When Thru of V, Set the delay of HD-Pulse.The variability is 32W～44W (1W=27MHz).
21H : D1	BSRY filter	It usually uses on ON.
21H : D0	BSRC filter	It usually uses on ON.
22H : D7	HD-OUT of polarity	The polarity of the HD output is chosen.
22H : D6	VD-OUT of polarity	The polarity of the VD output is chosen.
22H : D5	Polatity of Field	The polarity of the Field output is chosen.
22H : D4	H/V-OUT through	H/V-OUT in 601 output is chosen. 656 : H/V-pulse equal to 656. Through : H/V-pulse equal to the input signal.
22H : D3	Polarity of CKOUT	The polarity of the CKOUT is chosen.
22H : D2	V.BLK processing	Processing of V-Blanking is chosen. It usually uses on 0:NORMAL. The period of blanking in NORMAL are Y=16LSB (8bit) and C=128LSB (8bit). Through is for the test.
22H : D1	Y output Amplitude	The amplitude of the Digital output is changed. It usually uses on 0:1.71875. "1" is for the test.
23H : D6	Cb/Cr phase	The output of Cb and Cr can change. 0 : Digital Format Normal 1 : change
23H : D5-D4	50/60Hz VD cotrol	VD output is controlled. (It becomes effective when it is set up in 601 output.) 00 : Free run 01 : It is fixed on 50 or 60 on non-signal. Frequency to fix depends on TVM2. 10 : When Video-system is MANUAL control, a setup is always fixed on TVM2. 11 : It is always fixed on TVM2 at MANUAL. It is fixed on TVM2 at non-signals.
23H : D3	Field Det on non-signal	The detection of Field is set up on non-signals.
23H : D2-D0	Ext VD phase	It is A phase in the external-VD-input. Variable is -7.94[μs] ～ 5.96[μs].
24H : D7-D5	Horizontal phase for field detection	It is H-phase of Field-detection. It is the phase margin. Use with Bus:100.
24H : D4	V count	It is the allowable range of V-counter. It can set margin of "V-Sep phase and H-counter". It usually uses on 0.
24H : D3	V count reset	It is the specifications of reset of V-counter. When ON, It can reduce field-miss-detection. It usually uses on ON.

BUS address	Function	Contents
24H：D2	AFC leak control	It is Leak-control in the AFC circuit. It usually uses on OFF.
24H：D1-D0	The order of read Data	It can change order that Read-data. 00: ABCD A：Detection、B：CCD、C：ID1、D：WSS BUS：01=BCAD、BUS：10=CABD、BUS：11=DABC
25H：D7	Data insert of H	It insert Read-data to the H period of the output. Data is inserted after EAV at 656. Data is inserted same place with 656 at 601.
25H：D6	Data insert of V	It insert Read-data to the V period of the output. Data is inserted after EAV at 656. Data is inserted same place with 656 at 601.
25H：D5	Data insert for 601	Data can insert on either of Y or CbCr at 601 output. Data cannot insert both line.
25H：D4-D0	Line number for insert Data.	Set line which Read-Data insert. It can set each 1-line for 1bit.
26H：D7-D4	Line number for insert Data in field blank.	Set line(in Field-Blanking) which Read-Data insert. It can set each 1-line for 1bit.
26H：D3-D0	For DID code	This setup is DID code.
27H：D7-D0	For DID code	This setup is DID code.
28H：D7-6	Histerisis for color stripe detection	It is Histerisis of the Color-stripe-detection. If takes the long time, detection-time increase. But, miss-detection decreases.
28H：D5-D4	Histerisis for color stripe detection	It is Histerisis of the Color stripe detection-OFF. If takes the long time, detection-OFF-time increase. But, miss-detection decreases.
28H：D3-D2	Mask period for color stripe detection	It is the detection period of color-stripe. It is judged in more than the setup period.
28H：D1-D0	Sensitivity for color stripe detection	It is the detection sensitivity of color-stripe. It is judged in more than the setup.
29H：D7	Color stripe detection	It set ON/OFF of color stripe detection.
29H：D5	AGC detection periode	It is the Pulse width of the AGC detection.
29H：D4	Pulse width of Pseudo sync	It is the Pulse width of the pseudo-sync pulse.
29H：D2	Pseudo H sync detection	It set ON/OFF of pseudo H sync detection.
29H：D1-D0	Slice level for pseudo H sync	It set slice level of pseudo H sync.
2AH：D7	LPF for AGC pulse & pseudo H sync detection	It set ON/OFF of LPF for AGC pulse & pseudo H sync detection
2AH：D6	Route change of AGC pulse & pseudo H sync	It is Route of “AGC pulse & pseudo H sync”. Switching of Route is before and after the AGC circuit.
2AH：D4	AGC Pulse detection	It set ON/OFF of AGC Pulse detection.
2AH：D3-D2	Slice level for AGC pulse	It set slice level of AGC pulse.
2AH：D1-D0	Histerisis time for AGC pulse detection	It set histerisis-time of AGC pulse detection.
2BH：D7	Peak AGC ON/OFF	It set ON/OFF of peak AGC.
2BH：D6-D5	Limit level of Peak AGC	It set Limit level of Peak AGC.
2BH：D4	fsc Trap Filter	It set ON/OFF of fsc Trap Filter.
2BH：D3-D2	Peak AGC attack time	It set Peak AGC attack time.

BUS address	Function	Contents
2BH : D1-D0	An integral coefficient of Peak AGC detection	It is the integral-coefficient of Peak AGC detection.
2CH : D7	Sync AGC	It set ON/OFF of Sync AGC.
2CH : D3-D2	Sync AGC attack time	It set Sync AGC attack time.
2CH : D1-D0	Peak/Sync AGC recovery time	It set recovery time of Peak AGC and Sync AGC.
2DH : D7	LPF for CCD	It set ON/OFF of LPF for CCD.
2DH : D6	CCD slice function mode	It set mode of CCD slice function. Level changes by the input amplitude,when Auto mode.
2DH : D5	CCD slice level	It set CCD slice level. It is effective when 2DH:D6 is set a fix.
2DH : D3	Phase width of ID1 detection	It set phase width of ID1 detection.
2DH : D2	CCD Start bit detection	It is the detection sensitivity of the start bit of CCD.
2DH : D1-D0	Select CCD field	It set field that detect CCD.
2EH : D7	LPF for ID1	It set ON/OFF of LPF(Input stage of ID1-detection circuit)
2EH : D6	ID1 data slice function	It set ID1 data slice function. When Auto slice,slice level changes by the input amplitude.
2EH : D5-D4	ID1 slice level	It set ID1 slice level. It is effective when 2EH:D6.
2EH : D3	Detection for amplitude of ID1 signal	It is the reference amplitude of the detection. When it is off, Amplitude detection becomes AUTO.
2EH : D2	Phase of ID1 detection	It is the reference phase of the ID1 detection. When Adaptive , it can search in the range of $\pm 1.1\mu s$ at the D1.
2EH : D1-D0	Sampling phase of ID1	It is the phase of the detection of ID1. "1" changes in 0.12μs unit at D1, 0.28μs unit at D2. It usually uses on "0".
2FH : D7	LPF for WSS1	It set ON/OFF of LPF(Input stage of WSS-detection circuit)
2FH : D6	WSS data slice function	It set WSS data slice function. When Adaptive slice,slice level changes by the input amplitude.
2FH : D5-D4	WSS slice level	It set WSS slice level. It is effective when 2FH:D6.
2FH : D2	WSS SC Det mode	It set detection sensitivity of start-code of WSS.
2FH : D1-D0	Select WSS field	It set field that detect WSS.
30H : D7-D4	Adjust line timing of CCD	It is Delay-adjust of LINE-timing for the CCD detection. It uses when detection start deviates in weak electric density
30H : D3-D0	Adjust line timing of ID1	It is Delay-adjust of LINE-timing for the ID1 detection. It uses when detection start deviates in weak electric density
31H : D7-D4	Adjust line timing of WSS	It is Delay-adjust of LINE-timing for the WSS detection. It uses when detection start deviates in weak electric density
31H : D3	fsc pull in	It set sensitivity of Pulled-in of fsc. High: Sensitivity is up.
31H : D2	13.5MHz trap	It set ON/OFF of 13.5MHz Trap at ADC. It usually uses on "ON".
31H : D1	IIR Filter selection	Characteristic selecting of C-filter of SECAM.
31H : D0	IIR Filter ON/OFF	It set ON/OFF of C-filter of SECAM. A color beat can be reduced. It usually uses on "Always ON" in SECAM.

BUS address	Function	Contents
32H : D7	D1/D2 Det	It is the distinction of D1/D2. It is effective 32H:D6 when manual set.
32H : D6	D1/D2 Manual set	Internal control is fixed with D1orD2.
32H : D5-D4	Internal feed-back-clamp	When clamp set internal, it can set time constant.
33H : D7	Manual Gain AGC	It set ON/OFF of Peak-AGC Gain. It is effective when it is ON. It gives priority to Manual when this bit is ON. Therefore, it can't get the effect of AGC.
33H : D6-D0	Manual Gain	It is effective when 33H(D7). Gain becomes a fix.
34H : D7-D4	CGP start phase	It set start phase of CGP(Output of Terminal-73).
34H : D3-D0	Width of CGP	It set width of CGP(Output of Terminal-73).
35H : D7-D4	Threshold for DET.443	It set threshold for DET.443. It is easy to distinguish when a MAX side is chosen.
35H : D1-D0	Sync-tip-clamp-mode for Y-input	It is the control of limit-clamp to add under the input signal at Y input. Four kinds of switchings are possible. ON:Always,limitter-clamp to add to Low-level of input is ON. OFF:Always,limitter-clamp to add to Low-level of input is off. AUTO1 : It is ON in the no-signal and 'When Pedestal-Level deviated greatly.' AUTO2 : It is ON on no-signal.
36H : D7	CGP OUT control	It set action of CGP. AUTO: It is output only when an input signal is set 11(D7 and D6 on 00H). Forced on: It is output to all the input.
36H : D6	C Trap of DCOMB	It is ON, when you want reduce Cross-color and beat.
36H : D0	Mute	The Blanking period becomes mute.
37H : D7	Y Noise	It set f0 of Y-Noise-Canceler. It usually uses on "0".
37H : D6	Y Noise Lim	It set Limitter of Y-Noise-Canceler.
37H : D5	Y Noise Gain	It set Gain of Y-Noise-Canceler.
37H : D4	Y Noise canceler	It set ON/OFF of Y-Noise-Canceler.
37H : D3	CKILL Gain	It set the condition of CKILL Gain. When it is set up in +6dB, Level which color disappears to grows big. It uses "0" when weak electric density.
37H : D2	C Noise lim	It set Limitter of C-Noise-Canceler.
37H : D1	C Noise Gain	It set Gain of C-Noise-Canceler.
37H : D0	C Noise canceler	It set ON/OFF of C-Noise-Canceler.

MAXIMUN RATINGS (Vss=0V, Ta=25℃)

Each item of the maximum rating shows the marginal value of this product. Since a product is sometimes damaged when rating is exceeded also one item or for a moment again, be sure to use it within rating.

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage1 (1.5V System)	VDD1	-0.3 ～ VSS+2.0	V
Power Supply Voltage2 (2.5V System)	VDD2	-0.3 ～ VSS+3.5	V
Power Supply Voltage3 (3.3V System)	VDD3	-0.3 ～ VSS+3.9	V
Input Voltage	VIN	-0.3 ～ VDDIO +0.3	V
	SDA/SCL(Note1)	-0.3 ～ VSS + 5.5	V
	A IN	-0.3 ～ VDDAD+0.3	V
Potential difference between power supply terminals (1.5V System)	VDG1 (Note2)	0.3	V
Potential difference between power supply terminals (2.5V System)	VDG2 (Note2)	0.3	V
Potential difference between power supply terminals (3.3V System)	VDG3 (Note2)	0.3	V
Potential difference between power supply terminals (1.5V System＞2.5V System)	VDG4 (Note2)	0.3	V
Potential difference between power supply terminals (2.5V System ＞3.3V System)	VDG5 (Note2)	0.3	V
Power Dissipation	PD(Note3)	1900	mW
Storage Temperature	Tstg	-40 ～ 125	℃

(Note1) SDA, SCL： 5V tolerance.

(Note2) 1.5V system power supply terminal is made into the same voltage, 2.5V system power supply terminal is made into the same voltage, and 3.3V system power supply terminal is made into the same voltage.
The maximum potential difference should not exceed rating for all power supply terminals then.

(Note3) Derated above Ta=25℃ in the proportion of 19mW/℃.

Operation conditions (Vss=0V)

Cannot guarantee operation of TC90A92F, when the recommendation power supply voltage range (1.40V-1.65V, 2.3V-2.7V, 3.0V-3.6V) is exceeded.
Once, when it returns from the over range, it differs from a front condition.

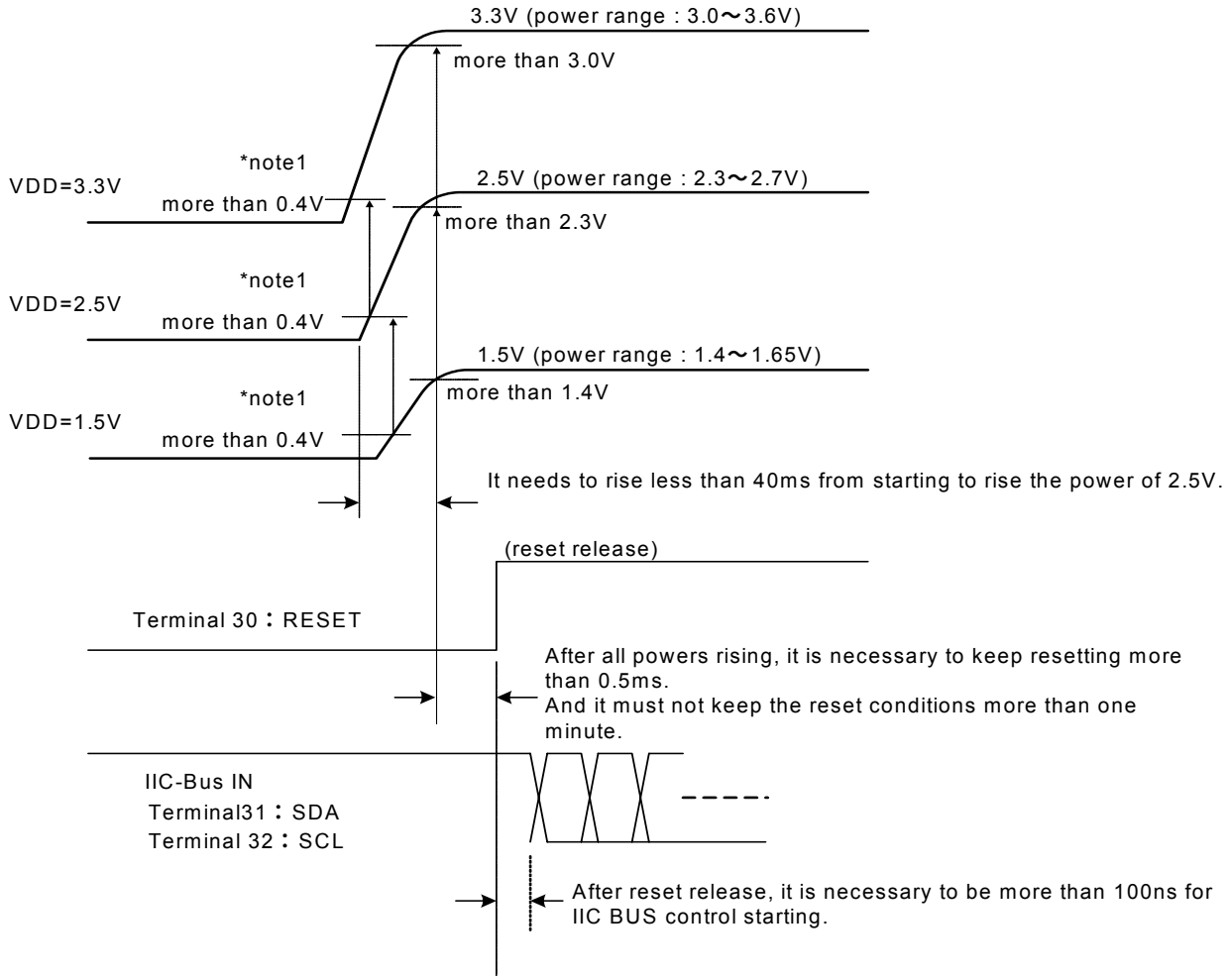
CHARACTERISTIC	Terminal No.	SYNBOL	MIN	TYP	MAX	UNIT
Supply Voltage for digital block	15,32,39,54,66	DVDD1-5	1.40	1.5	1.65	V
Supply Voltage for I/O block	23,49,60	VDDIO1-3	3.0	3.3	3.6	V
Supply Voltage for XO block	6	VDDXO	3.0	3.3	3.6	V
Supply Voltage for PLL block	2	VDDPLL	2.3	2.5	2.7	V
Supply Voltage for Analog block	82,89,95,97	VDDAD/VDDDA	2.3	2.5	2.7	V
Ambient operating temperature	-	Topr	-10	—	75	℃

The condition of power (VDD=3.3V, 2.5V, 1.5V) rising and falling

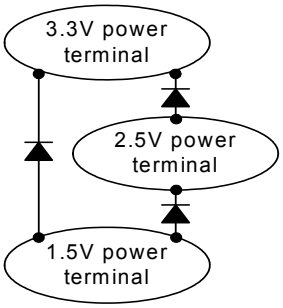
(1)Power Supply rising

These contents are the important items which influence the reliability guarantee of the IC.
It is necessary to satisfy the following condition.

(1) Power rising condition



*note1
Such the power terminal are embedded the protective diode.
It must not send a penetration electric current.
Condition:
Power level of 3.3V line ≧ Power level of 2.5V line ≧ Power level of 1.5V line
When the power level of 1.5V line is more than 0.4V, 3.3V line and 2.5V line must reach the level of power more than 0.4V.
And when the power level of 2.5V line is more than 0.4V, 3.3V line must reach the level of power more than 0.4V.



(2) Power falling condition

It is necessary to fall the power of 1.5V line before 3.3V line and 2.5V line are fallen, and to fall the power of 2.5V line before 3.3V line is fallen.
It must not send a penetration electric current too.

ELECTRICAL CHARACTERRISTICS

(1) DC CHARACTERRISTICS

(Ta=25°C,VDD1=1.50±0.1V,VDD2=2.50±0.2V,VDD3=3.30±0.3V)

ITEM	Terminal No.	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Current	15,32,39,54,66	IDD1	30	45	70	mA	Sum total current of 1.5V system power supply terminal NTSC:Y/C IN, Color Bar Signal
	2,82,89,95,97	IDD2	80	105	135	mA	Sum total current of 2.5V system power supply terminal NTSC:Y/C IN, Color Bar Signal
	6,23,49,60	IDD3	15	30	60	mA	Sum total current of 3.3V system power supply terminal Changes with the loads of I/O.
Input Voltage	10,11,12,13,14,16,17,18,20,21,22,24,25,28,29,30,31,50,51	VIH	VDD3x0.8		VDD3	V	I/O input terminal of 3.3V system
	26,27,33						I/O input terminal of 5.0V system
	10,11,12,13,14,16,17,18,20,21,22,24,25,28,29,30,31,50,51	VIL	VSS		VDD3x0.2	V	I/O input terminal of 3.3V system
	26,27,33				VDD3x0.2		I/O input terminal of 5.0V system 5.0V Pull up use
					0.3		I/O input terminal of 5.0V system 3.3V Pull up use
Input Current	10,11,12,13,14,16,17,18,20,21,22,24,25,28,29,30,31,50,51	IIH	-10		10	µA	3 I/O input terminal of 3.3V system
	26,27,33						I/O input terminal of 5.0V system
	10,11,12,13,14,16,17,18,20,21,22,24,25,28,29,30,31,50,51	IIL	-10		10	µA	I/O input terminal of 3.3V system
	26,27,33						I/O input terminal of 5.0V system
Output Voltage	35,36,37,38,40,41,43,44,46,47,48,52,53,55,56,58,59,61,62,64,65,67,68,70,71,72,73,74,75	VOH	VDD3-0.6		VDD3	V	I/O output terminal of 3.3V system Load of 4mA outflow
	35,36,37,38,40,41,43,44,46,47,48,52,53,55,56,58,59,61,62,64,65,67,68,70,71,72,73,74,75	VOL	VSS		0.4	V	I/O output terminal of 3.3V system Load of 4mA inflow
	26						I/O output terminal of 5.0V system Load of 4mA inflow

Notice : **The specifications of VIL is difference in the Pull-up voltage.**
When it specially uses for 3.3V with pull-up, do the design which is less than 0.3V securely.

(2) AC CHARACTERRISTICS

(Ta=25°C,VDD1=1.50V,VDD2=2.50V,VDD3=3.30V)

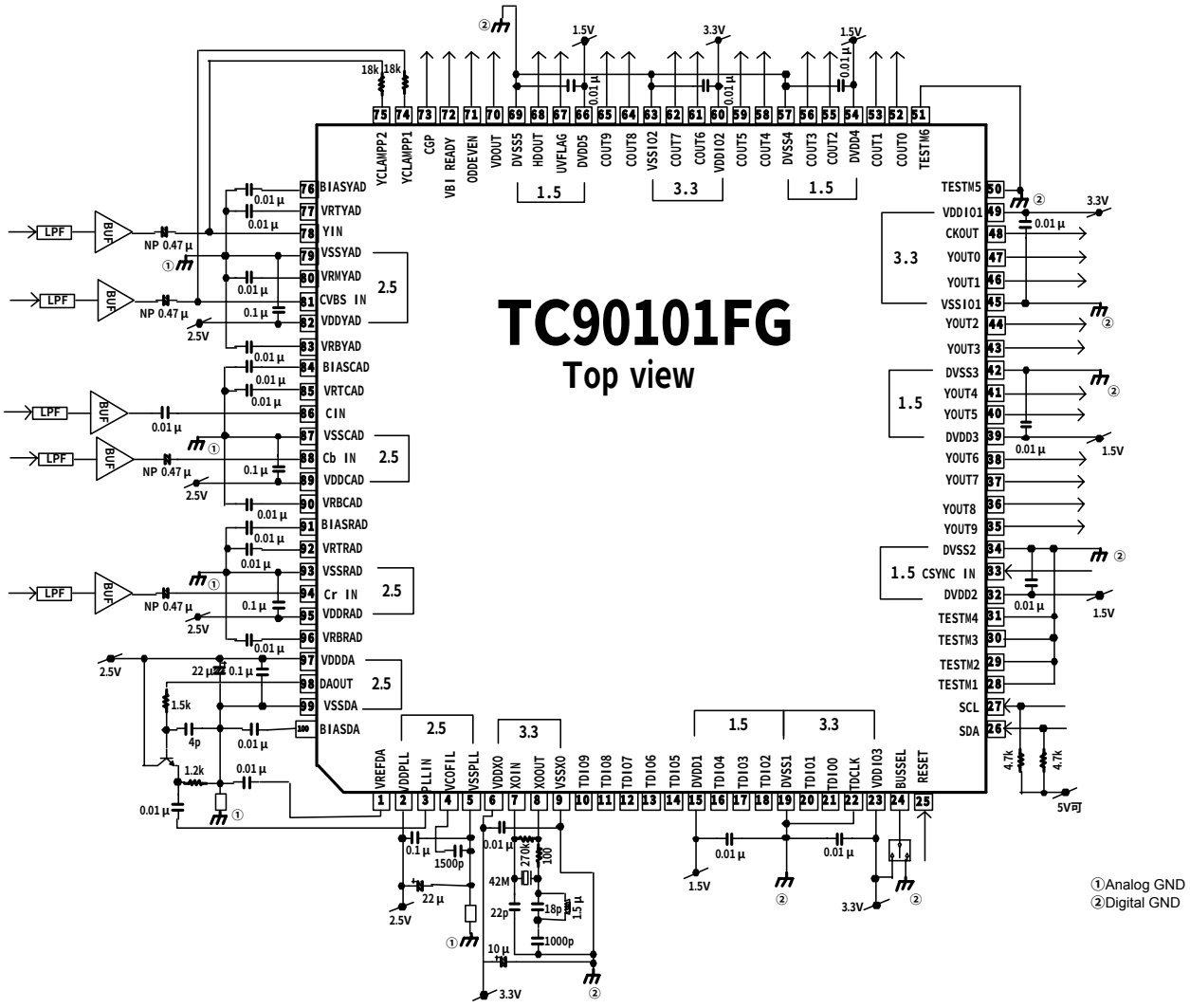
ITEM	Symbol	Min.	Typ.	Max.	Unit	Note
AD input level for Y	VYIN		0.7	0.8	Vp-p	White 100% Signal
AD input level for C	VCIN		0.5	0.8	Vp-p	Cb/Cr input
ADC differentiation error	DLEa		±4		LSB	
ADC integration error	ILEa		±4		LSB	
Output impedance	Zy	160	200	240	Ω	

(3) PLL CHARACTERRISTICS

(Ta=25°C,VDD1=1.50V,VDD2=2.50V,VDD3=3.30V)

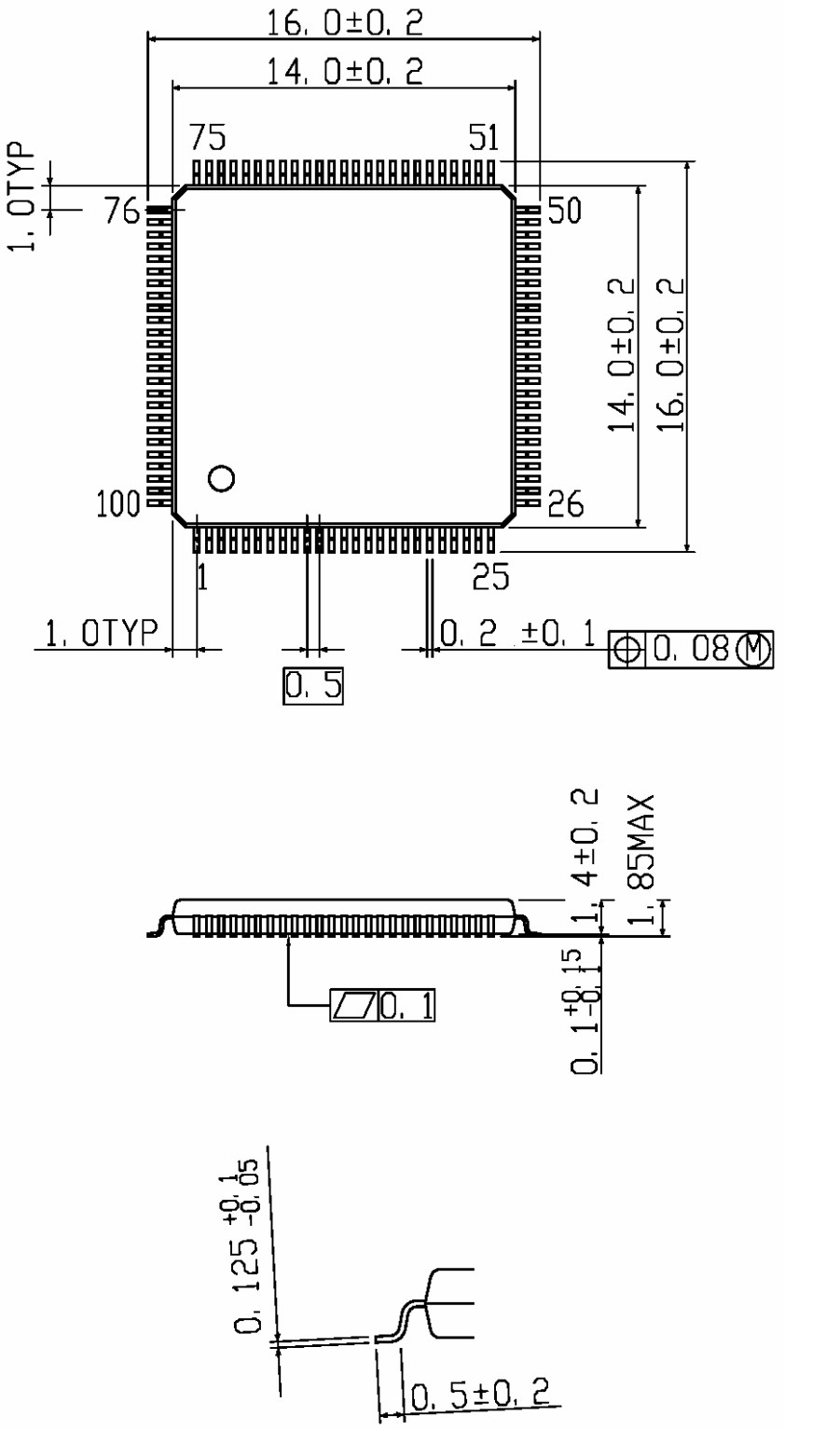
ITEM	Symbol	Min.	Typ.	Max.	Unit	Note
Drawing-in frequency range	ΔfckN	-50		50	kHz	Clock Amplitude:0.5Vp-p
Operation input amplitude	Vck	0.3	0.5	2.0	Vp-p	Standard clock frequency input

Application



● PACKAGE OUTLINE

LQFP100-P-1414-0.50C UNIT:mm



Weight：0.65g（center）

About soloderability, following conditions were confirmed.

● Solderability

(1) Use of Sn-63Pb solder Bath
- solder bath temperature=230°C
- dipping time=5seconds
- the number of times=once
- use of R-type flex

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- solder bath temperature=245°C
- dipping time=5seconds
- the number of time=once
- use of R-type flex

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030619EBA

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