

TOSHIBA Bi-CMOS Linear Integrated Circuit Silicon Monolithic

TB2932HQ (TENTATIVE)

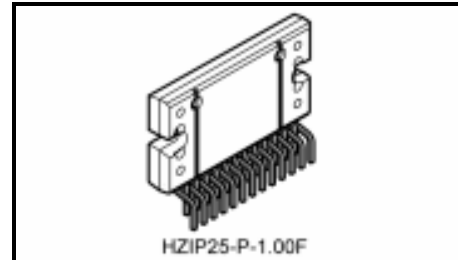
Maximum Power 43 W BTL × 4-ch Audio Power IC

The TB2932HQ is 4ch audio amplifier for car audio application.

This IC can generate high power, high quality sound output, $P_{OUT\ MAX} = 43\ W$, using a pure complementary P-ch and N-ch DMOS output stage.

The built-in self diagnosis function which is included can be controlled via I²C BUS.

In addition, stand-by and mute function, and various Protection feature are included.



Weight: 7.7 g (typ.)

Features

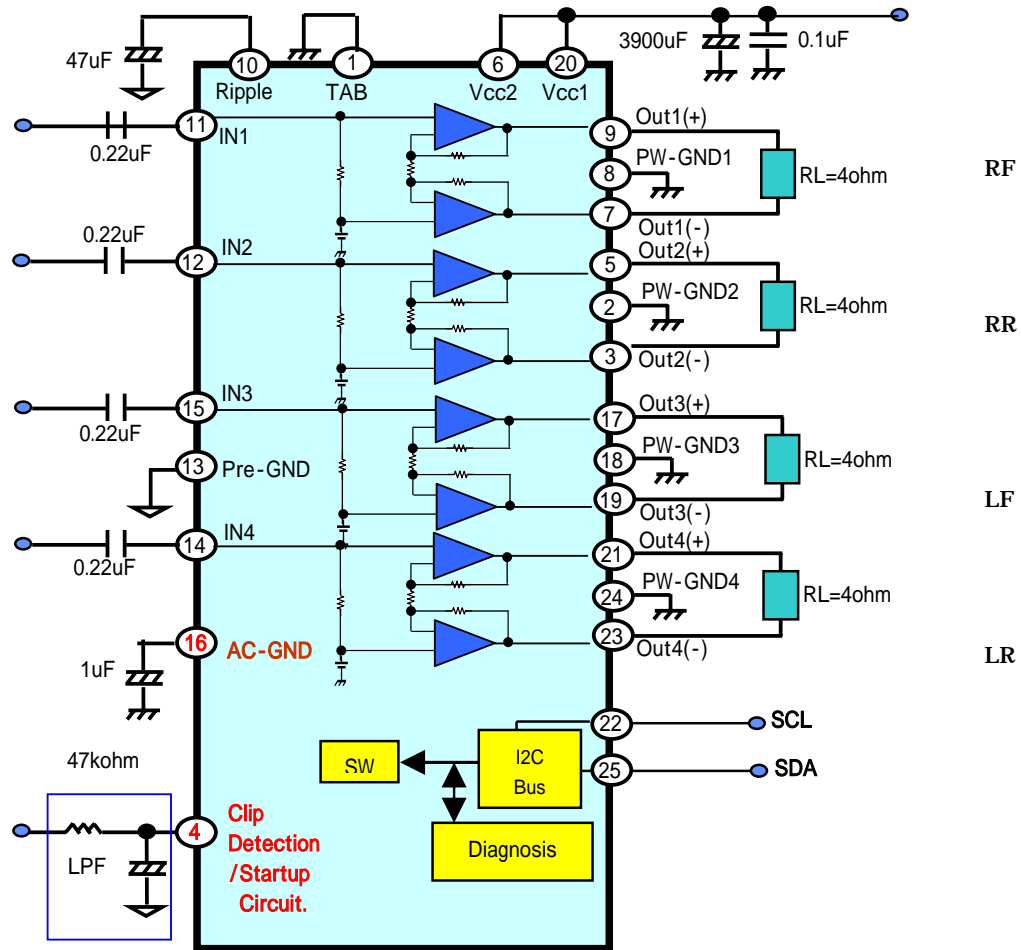
- **High power output**
 - : $P_{OUT\ MAX} (1) = 43\ W$ (typ.)
P ($V_{CC} = 15.2\ V$, $f = 1\ kHz$, JEITA max, $R_L = 4\ \Omega$)
 - : $P_{OUT\ MAX} (2) = 41\ W$ (typ.)
($V_{CC} = 14.4\ V$, $f = 1\ kHz$, JEITA max, $R_L = 4\ \Omega$)
 - : $P_{OUT\ MAX} (3) = 70\ W$ (typ.)
($V_{CC} = 14.4\ V$, $f = 1\ kHz$, JEITA max, $R_L = 2\ \Omega$)
 - : $P_{OUT} (1) = 27\ W$ (typ.)
($V_{CC} = 14.4\ V$, $f = 1\ kHz$, THD = 10%, $R_L = 4\ \Omega$)
 - : $P_{OUT} (2) = 23\ W$ (typ.)
($V_{CC} = 13.2\ V$, $f = 1\ kHz$, THD = 10%, $R_L = 4\ \Omega$)
 - : $P_{OUT} (3) = 45\ W$ (typ.)
($V_{CC} = 14.4\ V$, $f = 1\ kHz$, THD = 10%, $R_L = 2\ \Omega$)
- **Low distortion ratio:** THD = 0.007% (typ.)
($V_{CC} = 13.2\ V$, $f = 1\ kHz$, $P_{OUT} = 5\ W$, $R_L = 4\ \Omega$)
- **Low noise:** $V_{NO} = 60\ \mu V_{rms}$ (typ.)
($V_{CC} = 13.2\ V$, $R_g = 0\ \Omega$, BW = 20 Hz to 20 kHz, $R_L = 4\ \Omega$)
- **Built in stand by & muting function:** controlled via I²C Bus (26/12dB)
- **Built in clipping detection** (pin 4)
- **Built in I²C Bus for stand-by, mute, voltage gain control, self diagnosis:** Output short detection, offset detection, tweeter or speaker open detection (pin 22 and 25)
- **Built-in various protection circuits** (Note 1, Note 2)
Thermal shut down, over-voltage, out to GND, out to V_{CC} , out to out short circuit
- **Operating supply voltage:** $V_{CC} (opr) = 8\ to\ 18\ V$ ($R_L = 4\ \Omega$)
 $V_{CC} (opr) = 8\ to\ 16\ V$ ($R_L = 2\ \Omega$)

Note 1: Install the product correctly. Otherwise, it may result in break down, damage and/or degradation to the product or equipment.

Note 2: These protection functions are intended to avoid some output short circuits or other abnormal conditions temporarily. These protect functions do not warrant to prevent the IC from being damaged.

- In case of the product would be operated with exceeded guaranteed operating ranges, these protection features may not operate and some output short circuits may result in the IC being damaged.

Block Diagram



Some of the functional blocks, circuits, or constants labels in the block diagram may have been omitted or simplified for clarity.

Caution and Application Information (description is made referring only on the single channel.)

External Component Values

Component Name	Recommended Value	Purpose	Effect		Notes
			Lower than Recommended Value	Higher than Recommended Value	
C1	0.22 μ F	To eliminate DC	Cut-off frequency becomes higher	Cut-off frequency becomes lower	Pop noise is concerned with this capacitor.
C2	10 μ F	To reduce ripple To determine the time of turn on diag	Power ON/OFF time and turn ON diag cycle shorter	Power ON/OFF time and turn ON diag cycle longer	
C3	0.1 μ F	To provide sufficient oscillation margin	Reduces noise and provides sufficient oscillation margin		
C4	4.7 μ F	To reduce pop noise	Pop noise becomes larger Muting ON/OFF time is shorter	Pop noise becomes smaller Muting ON/OFF time is longer	
C5	3900 μ F	Ripple filter	Power supply ripple filtering		

Note 3: In case of the recommended value not used.

1. Fast Mute Mode

This feature will normally be used to suppress pop noise resulting from VCC transients during engine cranking condition.

The fast mute mode can be entered on receipt of a command via I²C bus.

Using the IB2 register and setting to 'one' the bit D6, it is possible to generate a fast I²C mute command.

If a fast mute command is received, this IC will operate and will discharge the built-in capacitor .

Therefore the Pop sound will be reduced compared to the condition when Fast Mute is not used in the engine cranking condition.

2. IC start up procedure

As for this product, to decrease an quiescent current with the stand-by state, the I²C BUS communication possible condition and the simple condition in case of the turning on exist.

Please confirm of the request the following contents in the limit of the set design.

1) The hardware stand-by state

It doesn't impress the external voltage (5V/3.3V) and it says the time when the Ripple voltage potential is large to the ClipDet terminal (4 pins).In case of this condition, it becomes Istby=0.

2) The software stand-by state

When impressing the external voltage (5V/3.3V) on the ClipDet terminal (4 pins), the internal reference of VDD amplifier starts-up, it becomes I²C BUS communication will possible condition.

In case of this condition, it becomes Istby=30uA.

3) The IC operation condition

In I²C BUS command (Stby L H), when sending by the Write command, the charging by the Ripple voltage (terminal) begins after the switchover to the condition of the above 2).

When the Ripple voltage(terminal) reaches the value of the wish by this, it becomes an IC operation condition. Therefore, before communicating in I²C BUS, it impresses voltage on the ClipDet terminal once and VDD must be started.

VDD stands up and after the I²C BUS communication becomes possible, because this terminal functions as the ClipDet terminal, only in IC start-up, it requests sequence setting to impress potential.

Incidentally, because it touches much more by the separate section about the conduct of the ClipDet terminal, .

3. Explanation for Self Diagnosis Via I²C

(1) Bus map

【Slave Address】

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Details	Hex
							0	Write Mode	
							1	Read Mode	
1	1	0	1	1	0	0	—		D8H

【WRITE】

• Sub address

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Details	Hex
0								Page Mode (auto increment) OFF	
1								Page Mode (auto increment) ON	
—	0	0	0	0	0	0	1	Control Byte1	01H
—	0	0	0	0	0	1	0	Control Byte2	02H

• Control byte1 (01H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
0	0	0	0	0	0	0	1	Clip Det 1% to 10% change
0	0	0	0	0	0	1	0	R-ch Muting off (play)
0	0	0	0	0	1	0	0	Fch Muting off (play)
0	0	0	0	1	0	0	0	R-ch Gain 26dB to 12dB
0	0	0	1	0	0	0	0	Fch Gain 26dB to 12dB
0	0	1	0	0	0	0	0	Offset Det Enable
0	1	0	0	0	0	0	0	Diag Cycle Enable
1	—	—	—	—	—	—	—	Turn-on Select (normal/repeatedly)

• Control byte2 (02H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
0	0	0	0	0	0	0	1	Rare short DET
0	0	0	0	0	0	1	0	Soft Mute delay time (40ms/20ms)
0	0	0	0	0	1	0	0	Current Detection Enable
0	0	0	0	1	0	0	0	Line Drive Diag
0	0	0	1	0	0	0	0	Stand By OFF (play)
0	0	1	0	0	0	0	0	Clip Det Pin change to Offset Det
—	1	—	—	—	—	—	—	Fast mute ON/OFF
1	0	0	0	0	0	0	0	Current Detection. Level change from 500 mA (max) to 300 mA (max)

Note 4: Self mute circuit is included on chip and is independent from I²C bus stage.
Self mute operating voltage is $V_{CC} = 7.8\text{ V}$

Note 5: Auto Increment is available.

If control byte 1 is chosen by sub address, it is not necessary to send byte 2 in cases when both byte 1 and 2 are to be written.

Ex) In case of sub address = byte1 chosen:

Sub address byte 1 → byte 1 writing → Sub address byte 2 → byte 2 writing: available

Sub address byte 1 → byte 1 writing ----- → byte 2 writing: available

【READ】

Byte 1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch1 Short to GND
0	0	0	0	0	0	1	0	Ch1 Short to V _{CC}
0	0	0	0	0	1	0	0	Ch1 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch1 Short load
0	0	0	1	0	0	0	0	Ch1 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch1 Current Detection (at IB2 D2 = 1 = enable only) (IB2 – D7 = 0: bit = 1: <250 mA, 0: >500 mA) (IB2 – D7 = 1: bit = 1: <100 mA, 0: >300 mA)
0	1	0	0	0	0	0	0	Bit = 1: Diag. Cycle terminated, 0: Not terminated
1	0	0	0	0	0	0	0	TSD Mute ON (thermal warning)

Byte 2

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch2 Short to GND
0	0	0	0	0	0	1	0	Ch2 Short to V _{CC}
0	0	0	0	0	1	0	0	Ch2 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch2 Short load
0	0	0	1	0	0	0	0	Ch2 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch2 Current Detection (at IB2 D2 = 1 = enable only) (IB2 – D7 = 0: bit = 1: <250 mA, 0: >500 mA) (IB2 – D7 = 1: bit = 1: <100 mA, 0: >300 mA)
0	1	0	0	0	0	0	0	Current sensor activated (D6 = 1)
1	0	0	0	0	0	0	—	Offset detection activated (D7 = 1)

Byte 3

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch3 Short to GND
0	0	0	0	0	0	1	0	Ch3 Short to V _{CC}
0	0	0	0	0	1	0	0	Ch3 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch3 Short load
0	0	0	1	0	0	0	0	Ch3 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch3 Current Detection (at IB2 D2 = 1 = enable only) (IB2 – D7 = 0: bit = 1: <250 mA, 0: >500 mA) (IB2 – D7 = 1: bit = 1: <100 mA, 0: >300 mA)
—	1	—	—	—	—	—	—	Diagnostic status (= IB1 – D6 bit = 1: diag enable)
1	—	—	—	—	—	—	—	Stand-by status (= IB2 – D4 bit = 1: play)

Byte 4

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch4 Short to GND
0	0	0	0	0	0	1	0	Ch4 2 Short to VCC
0	0	0	0	0	1	0	0	Ch4 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch4 Short load
0	0	0	1	0	0	0	0	Ch4 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch4 Current Detection (at IB2 D2 = 1 = enable only) (IB2 – D7 = 0: bit = 1: <250 mA, 0: >500 mA) (IB2 – D7 = 1: bit = 1: <100 mA, 0: >300 mA)
0	1	0	0	0	0	0	0	Rare short
1	0	0	0	0	0	0	0	LDT DET

Note 6: Short circuit protection can be operated channel by channel.

EX) If channel 1 output is shorted, channel 1 is protected but other channels are available.

Caution: sub address 0x15 (15H) is for our internal testing only. Do not apply for your using.

(2) Description for turn on diagnosis

This IC can determine whether the conditions listed below occur or not at turn ON:

- Short to GND
- Short to VCC
- Output to output short
- Speaker open

As first “switch on”, the write data is sent to “turn ON” the IC.

If the turn on diagnostic is activated at this time, the write data, with the diagnostic cycle byte: IB1 D6 set at 1, is sent at the same time

The result of self diagnosis can be obtained from the read data sent after the turn on diagnostic data permitted time, as below Figure:

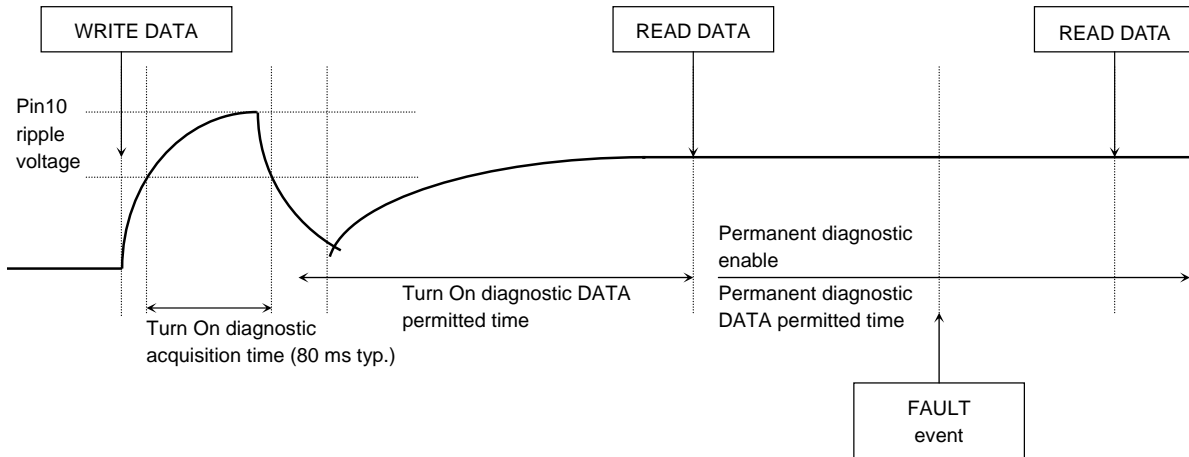


Figure 4 Diagnosis Timing Chart

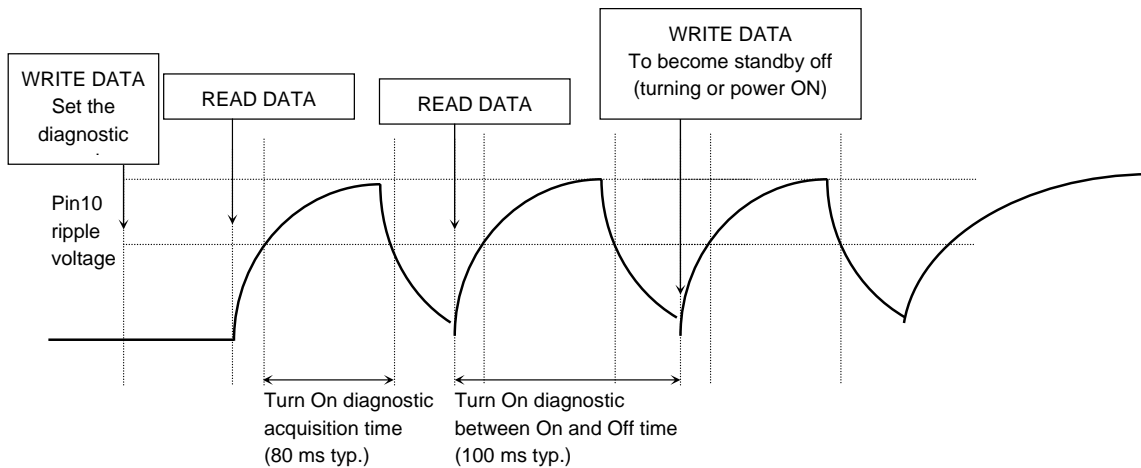


Figure 5 Number of Times Turn ON Diagnosis Timing Chart

As initially, the write data is set when the on diagnostic cycle enable (IB1 D6 = 1), the turn on diagnosis can be available for repeated use by sending the read command repeatedly after the initial set up as shown as Figure 5.

Therefore, it is useful to check number of cycles from Power ON to the output appearance.

This IC has two built-in diagnostic modes dependent on the Turn-on timing.

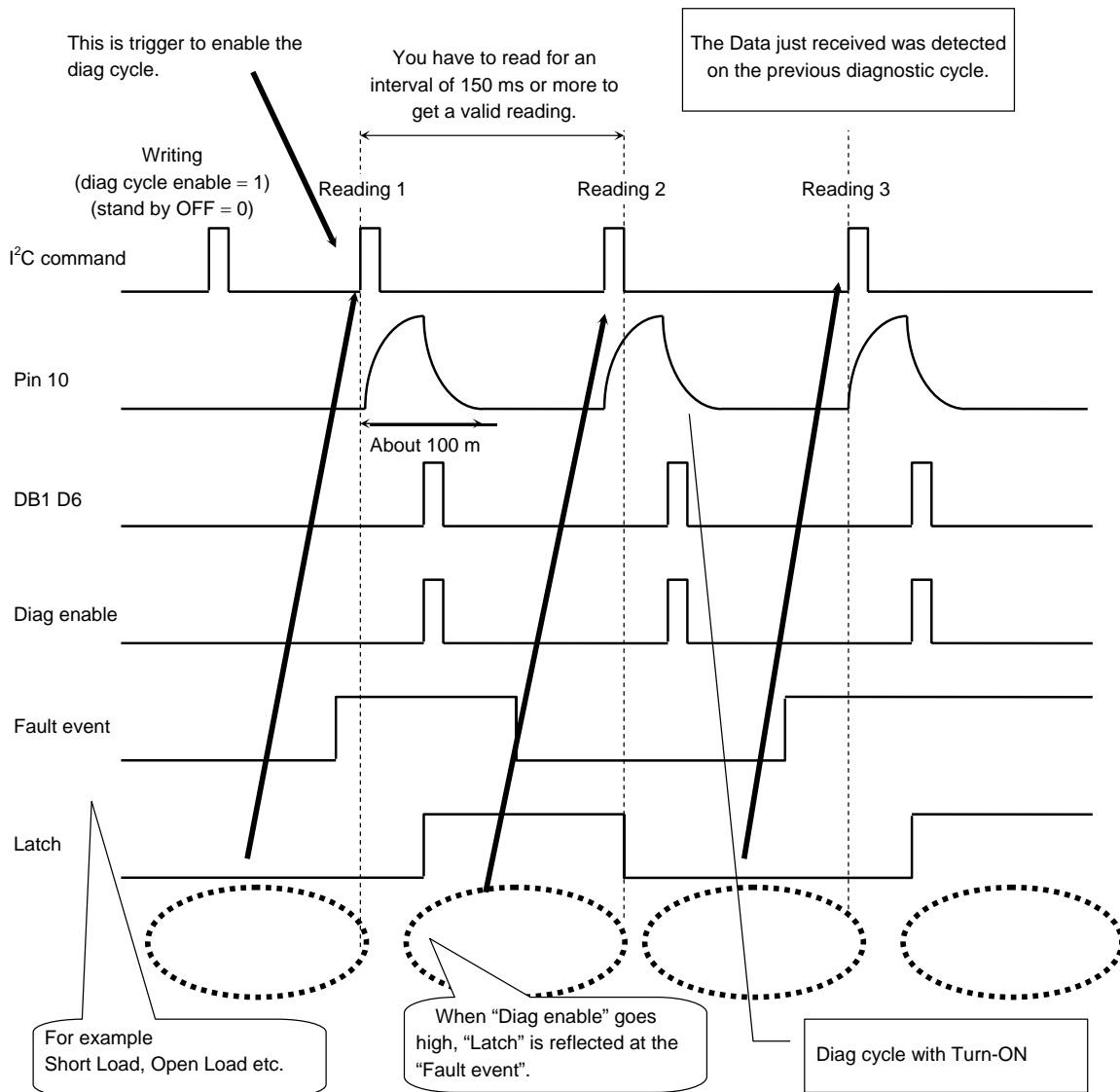
A) Normal mode (one shot) of Turn-on diagnostics (data of IB1, D7 = 0)

B) Repeatability mode of Turn-on diagnostics (data of IB1, D7 = 1)

A) Normal mode (one shot diag.)

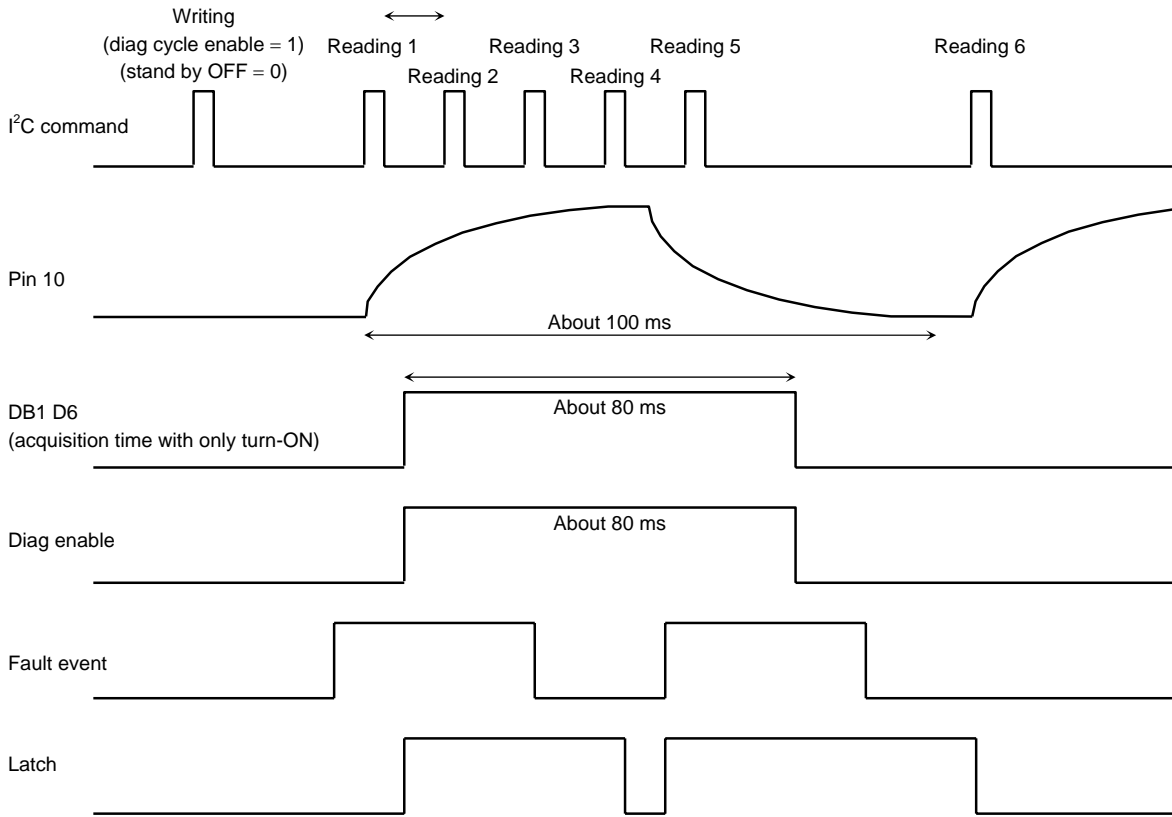
For example, if you want to get two valid readings, you have to send the command to read three times.

True data are second data and third data.



B) Repetition mode

Maximum interval:
You can select the acquisition time.
Minimum interval:
It is determined by the speed of microcomputer.



The turn ON diagnostic acquisition time is determined by the ripple filter capacitance C2 and the equivalent internal resistance Rr as below expression.

$$\text{Acquisition time} = 2 \times C2 \times Rr = 4400 \times C2 \text{ (typ.)}$$

Rr is fixed in internal circuit and it is not varied by the fluctuation of power supply VCC voltage.

C2 value determines the time from power ON (standby off) to the appearance of sound signal from output and the characteristic for ripple rejection ratio, too. So, take care with the decision on C2 value.

If the turn ON diagnosis is not used, in other words the diagnostic cycle defeat command is sent, the waveform of ripple terminal voltage will change but the time from turning on to the output signal appearance will not change as illustrated below in Figure 6.

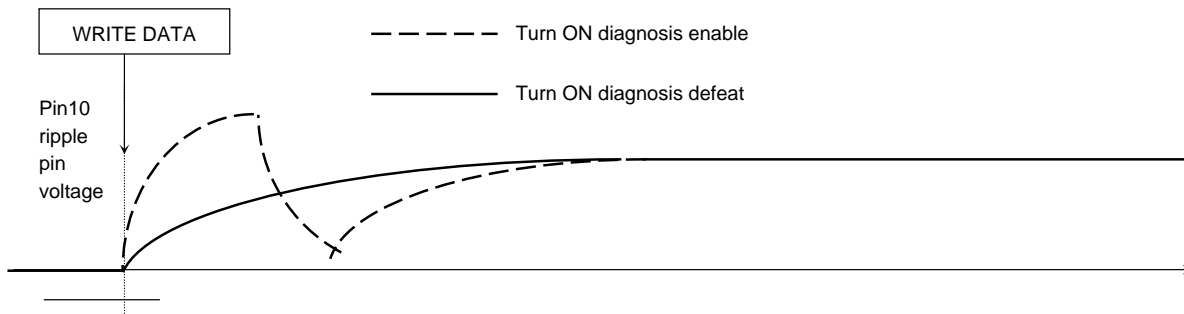


Figure 6 Turn on Diagnosis Timing Chart when Turn on diagnosis not used.

(3) Description for permanent diagnosis

This IC can provide permanent diagnosis under the following conditions, whether they occur before or after turning ON:

- Short to GND
- Short to VCC
- Output to output short circuit
- Output offset detection
- Current detection for tweeter open

This permanent diagnosis is available not only with the diagnostic cycle byte: IB1 D6 set at 1 but also when set at 0.

Additionally, the signal can be obtained by entering just a read command. It is not necessary to write the data.

With permanent diagnosis fault detection, the first read data after fault removal will still show a Fault. Therefore, it is necessary to obtain 3 or more readings in order to prevent a miss judgment. For example, the speaker sometimes makes a large counter electro motive force which this IC could recognize as a fault event.

Additionally, this permanent diagnosis is automatically on after the turning on diagnosis operation finished therefore there is no need to send the extra command.

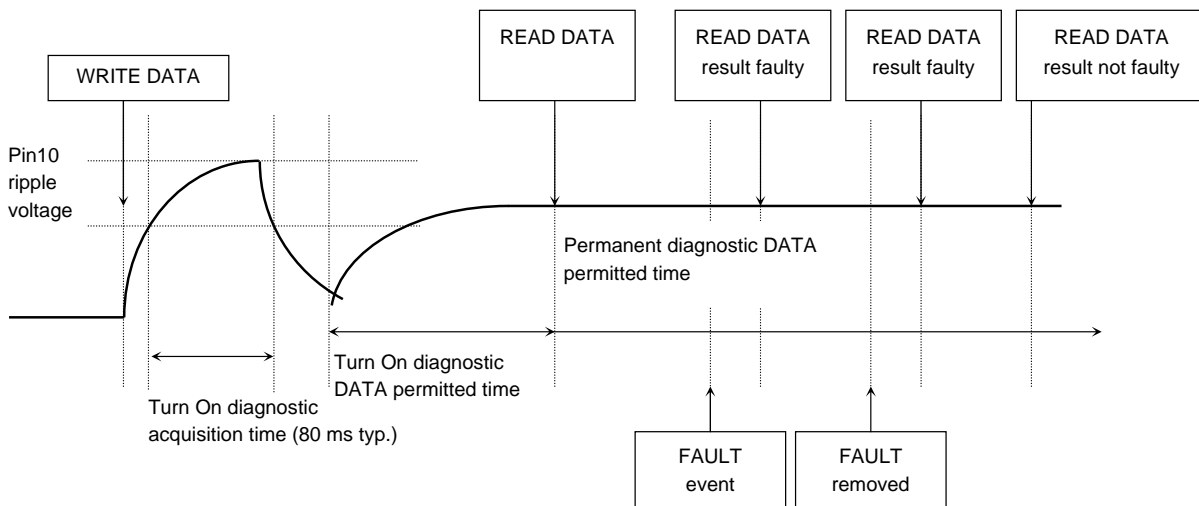


Figure 7 Permanent Diagnosis Timing Chart for Each Short Detection

Regarding operation of the output offset detection, The software always detects the output offset but the result is not latched internally as shown in the Figure below:

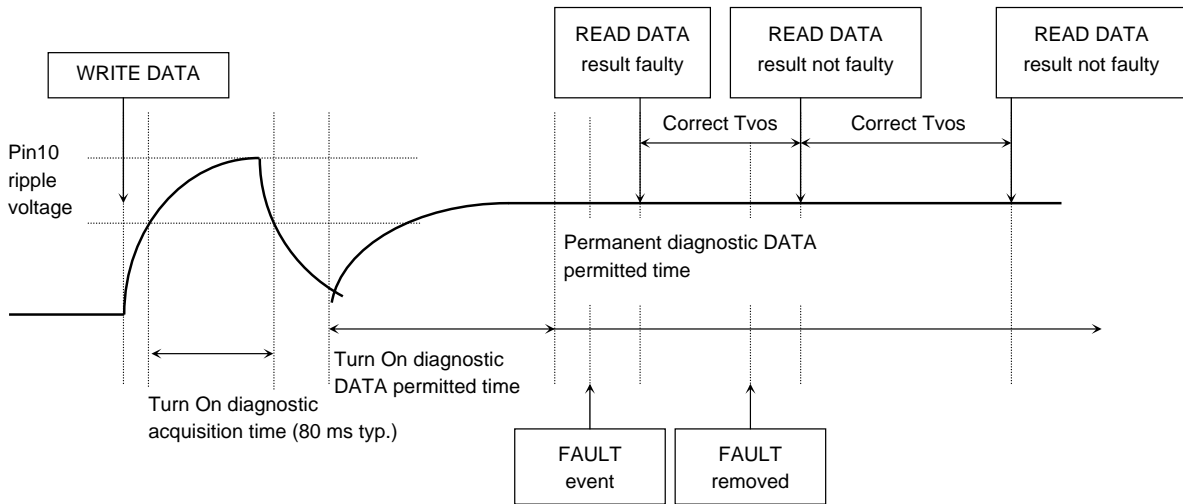


Figure 8 Software Output Offset Detection Timing Chart

However, this detection has to be performed in real time: Time voltage offset (Tvos) between read and next read is set at $Tvos = 1/\text{the lowest signal frequency}$, or more. For instance $Tvos > 50 \text{ ms}$ if the lowest output signal frequency is 20 Hz, and to obtain 2 or more readings in order not to make a misjudgment

Additionally, the threshold level is designed at $\pm 2 \text{ V}$.

The output from the terminal of pin 4 can be changed from clip detector to offset detector output by sending the write command via I²C.

If the L.P.F output voltage has become a half of pull up voltage for a while, firstly the signal output volume goes down (clipping detector function). After that, it can be judged that the abnormal output offset has occurred, if the L.P.F. output voltage does not rise above half of pull up voltage.

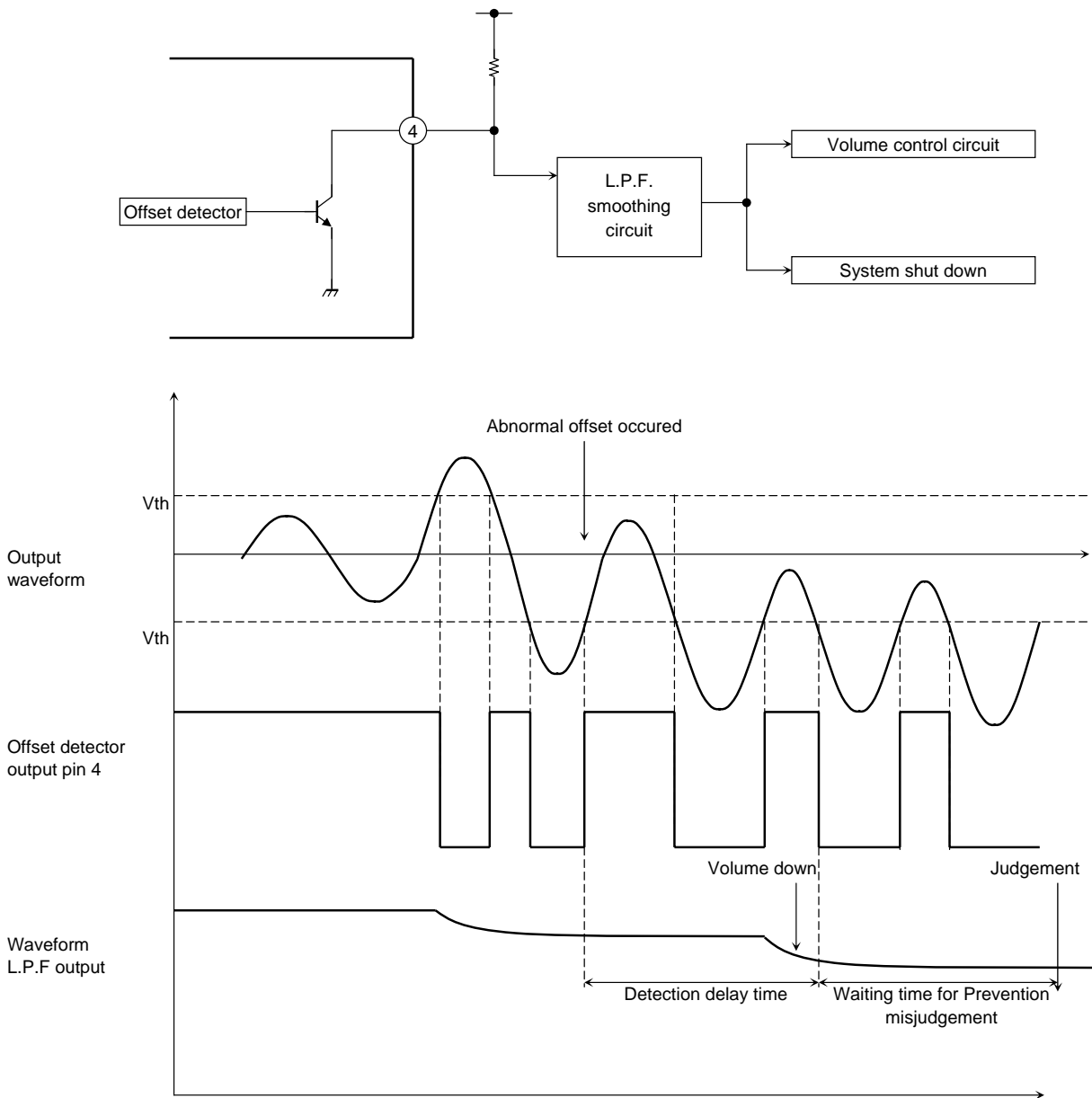


Figure 9 Hardware Output Offset Detection

- When the current detector for Tweeter open check is used, it is necessary to take care as below:
- Need to input the pulse or signal which is the higher out of audience frequency for example $f = 20 \text{ kHz}$
 - The pulse or signal input timing has to be after mute off (play mode)
 - At least, the read timing has to be after 1 cycle of input pulse or signal and more, the recommendation cycles are 3 cycle and more if can.
 - The level of input pulse or signal is more than the detection threshold level 300 mA or 500 mA.
- For instance, if the tweeter impedance is 20Ω at $f = 20 \text{ kHz}$ which is same as input signal frequency, the output minimum voltage is: $V_{out} = 500 \text{ mA} \times 20 \Omega = 10 \text{ V}$ and more.

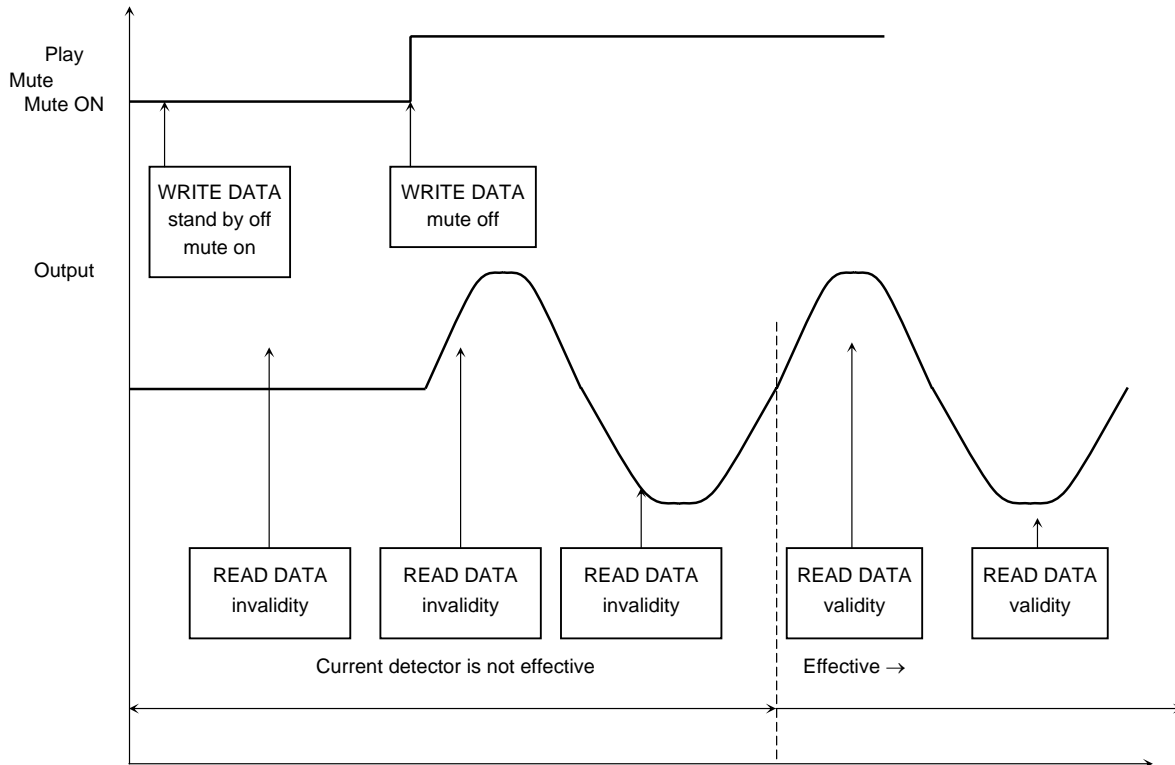


Figure 10 Tweeter Open Detection Timing Chart

Finally, if DB1 D7 = 1 then the temperature of IC chip is close to the thermal shutdown point. This warning bit becomes high, about 10 degrees below the temperature at which the overtemperature protection operates.

Note 7: Timing charts may have been simplified for ease of reading.

Note 8: Please arrange to read all self-diagnosis functions twice or more and apply judgment in order to avoid false triggering.

<Since the first diagnostic result has low confidence, please diagnose 2 times or more.>

(4) Multiple faults

The self diagnosis shows as below tables when there are multi fault connection for the audio outputs.

At Turning ON:

	S.GND (out+)	S.GND (out-)	S.VCC	Out to Out. S	Open L
S.GND (out+)	S.GND	S.GND	S.Load	S.GND	S.GND + No open
S.GND (out-)		S.GND	S.Load	S.GND	S.GND + No open
S.VCC			S.VCC + S.Load	S.VCC + S.Load	S.VCC + S.Load + open or No open
Out to Out.S				S.Load	S.Load + No open
Open L					Open

At Permanent:

	S.GND (out+)	S.GND (out-)	S.VCC	Out to Out. S	Open L
S.GND (out+)	S.GND	S.GND	S.GND or S.VCC (Note 10)	S.GND	S.GND (Note 9)
S.GND (out-)		S.GND	S.GND or S.VCC (Note 10)	S.GND	S.GND (Note 9)
S.VCC			S.VCC	S.VCC	S.VCC (Note 9)
Out to Out.S				S.Load + S.GND	N/A
Open L					Normal

Note 9: If the DC offset detection mode is ON, the information which the DC offset is appeared is added.

Note10: The chance which they can read this exact information is only one time although in case of other diagnosis, the more times sending read command, the higher the confidence of the result.

For example,

a) ch1+ is connected to GND

b) ch1- is connected to VCC

c) They can read or get the "Short to GND" information when the uP send the Read command.

d) Next, however, they can not get the "Short to GND" or "Short to VCC" information when the uP send the Read command again.

Note 11: Please arrange to read all self-diagnosis functions twice or more and apply judgment in order to avoid false triggering.

(5) Explanation of I²C bus commands

Below the "ADDRESS BYTE", presently the address byte is fixed at 216 dec = D8hex = 101100xbin.

- Address Selection is D8hexa:

A7	Address bit	1
A6	Address bit	1
A5	Address bit	0
A4	Address bit	1
A3	Address bit	1
A2	Address bit	0
A1	Address bit	0
A0 (R/W)	Read/Write bit	X

X: 0 = Write instruction to device; 1 = Read instruction to device

- If R/W = 0, the Up Sends Two Instruction Bytes, IB1 and IB2:

IB1 Instruction Byte:

Bit	
D7	Turn-on diag timing Normal (D7 = 0) Repeat (D7 =1)
D6	Diagnostic cycle enable (D6 = 1) Diagnostic cycle defeat (D6 = 0)
D5	Offset Detection enable (D5 = 1) Offset Detection defeat (D5 = 0)
D4	Front Channel Gain = 26dB (D4 = 0) Gain = 12dB (D4 = 1)
D3	Rear Channel Gain = 26dB (D3 = 0) Gain = 12dB (D3 = 1)
D2	Mute front channels (D2 = 0) Unmute front channels (D2 = 1)
D1	Mute rear channels (D1 = 0) Unmute rear channels (D1 = 1)
D0	CD 1% (D0 = 0) CD 10% (D0 = 1)

IB2 Instruction Byte:

Bit	
D7	Current Det 500 mA (max) (D7 = 0) Current Det 300 mA (max) (D7 = 1)
D6	Fast mute on (D6 = 1) off (D6 = 0)
D5	Pin4 Clip Detection (D5 = 0) Pin4 Offset Detection (D5 = 1)
D4	Std-by on-PA not working (D4 = 0) Std-by off-PA working (D4 = 1)
D3	Amplifier mode diagnostic (D3 = 0) Line driver mode diagnostic (D3 = 1)
D2	Current Det. diag enabled (D2 = 1) Current Det. diag defeat (D2 = 0)
D1	Software mute on and off delay time select Work standard 40ms delay (D1 = 0) Work standard 20ms delay (D1 = 1)
D0	Rare short detection Harf-short diag defeat (D1 = 0) Harf-short diag enable (D1 = 1)

- If R/W = 1, the Power Amplifier Sends Four Diagnostics Bytes, DB1, DB2, DB3 and DB4:

DB1 Diagnostic Byte:

Bit	
D7	Thermal warning active (D7 = 1)
D6	Diag not activated or not terminated (D6 = 0) Diag terminated (D6 = 1)
D5	Channel 1 current detection Output peak current < 250 mA (IB2 – D7 = 0) – open load (D5 = 1) Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1) Output peak current > 500 mA (IB2 – D7 = 0) – normal load (D5 = 0) Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)
D4	Channel 1 Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel 1 Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel 1 Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1) Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)
D1	Channel 1 No short to V _{CC} (D1 = 0) Short to V _{CC} (D1 = 1)
D0	Channel 1 No short to GND (D0 = 0) Short to GND (D0 = 1)

DB2 Diagnostic Byte:

Bit	
D7	Offset detection not activated (D7 = 0) Offset detection activated (D7 = 1)
D6	Current sensor not activated (D6 = 0) Current sensor activated (D6 = 1)
D5	Channel 2 current detection Output peak current < 250 mA (IB2 – D7 = 0) – open load (D5 = 1) Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1) Output peak current > 500 mA (IB2 – D7 = 0) – normal load (D5 = 0) Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)
D4	Channel 2 Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel 2 Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel 2 Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1) Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)
D1	Channel 2 No short to V _{CC} (D1 = 0) Short to V _{CC} (D1 = 1)
D0	Channel 2 No short to GND (D0 = 0) Short to GND (D0 = 1)

Note 12: DBx (D5) is effective only at the time of “Current detection enable”.

DB3 Diagnostic Byte:

Bit	
D7	Stand-by status (= IB2 – D4)
D6	Diagnostic status (= IB1 – D6)
D5	Channel 3 current detection Output peak current < 250 mA (IB2 – D7 = 0) – open load (D5 = 1) Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1) Output peak current > 500 mA (IB2 – D7 = 0) – normal load (D5 = 0) Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)
D4	Channel 3 Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel 3 Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel 3 Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1) Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)
D1	Channel 3 No short to V _{CC} (D1 = 0) Short to V _{CC} (D1 = 1)
D0	Channel 3 No short to GND (D0 = 0) Short to GND (D0 = 1)

DB4 Diagnostic Byte:

Bit	
D7	Lad dump voltage detection enable (D7=1) Disable(D6=0)
D6	Rare short detection enable (D6=1) Disable (D6=0)
D5	Channel 4 current detection Output peak current < 250 mA (IB2 – D7 = 0) – open load (D5 = 1) Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1) Output peak current > 500 mA (IB2 – D7 = 0) – normal load (D5 = 0) Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)
D4	Channel 4 Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel 4 Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel 4 Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1) Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)
D1	Channel 4 No short to V _{CC} (D1 = 0) Short to V _{CC} (D1 = 1)
D0	Channel 4 No short to GND (D0 = 0) Short to GND (D0 = 1)

Note 13: DBx (D5) is effective only at the time of "Current detection enable".

Examples of Bytes Sequence

1 - Turn-On Diagnostic - Write Operation

Start	Address byte with D0 = 0	ACK	Sub-address D0 = 1	ACK	IB with D6 = 1	ACK	IB2	ACK	STOP
-------	--------------------------	-----	--------------------	-----	----------------	-----	-----	-----	------

Note 14: Auto increment

2 - Turn-On Diagnostic - Read Operation

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP
-------	--------------------------	-----	-----	-----	-----	-----	-----	-----	-----	-----	------

3a - Turn-On of the Power Amplifier with 26dB Gain, Mute On, Diagnostic Defeat.

Start	Address byte with D0 = 0	ACK	Sub-address D0 = 1	ACK	IB 1	ACK	IB2	ACK	STOP
					X0X0000X		XXX1X0XX		

Note 15: Auto increment

3b - Turn-Off of the Power Amplifier

Start	Address byte with D0 = 0	ACK	Sub-address D0 = 1	ACK	IB 1	ACK	IB2	ACK	STOP
					X0XXXXXX		XXX0XXXX		

Note 16: Auto increment

4 - Offset Detection Procedure Enable

Start	Address byte with D0 = 0	ACK	Sub-address D0 = 1	ACK	IB 1	ACK	IB2	ACK	STOP
					XX1XX11X		XXX1X0XX		

Note 17: Auto increment

5 - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2, DB3, DB4).

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP
-------	--------------------------	-----	-----	-----	-----	-----	-----	-----	-----	-----	------

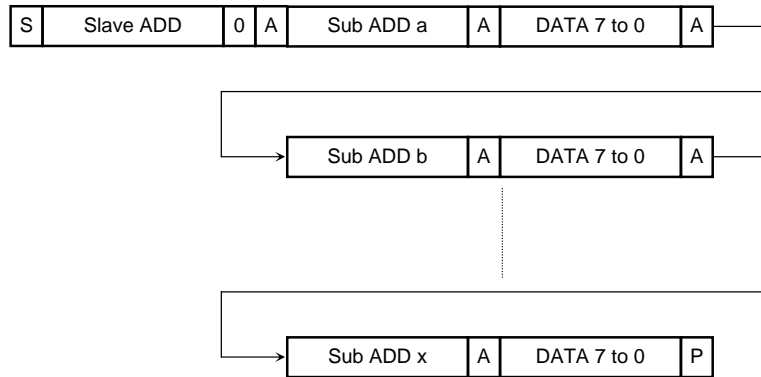
TB2932HQ I²C Bus Transmission Format

(1) Write mode

In addition to usual transmission, it corresponds to continuation transmission and the auto increment mode as a transmission format. After a transmission end, in case data transmission is newly, it is necessary to open the term beyond 1 clock.

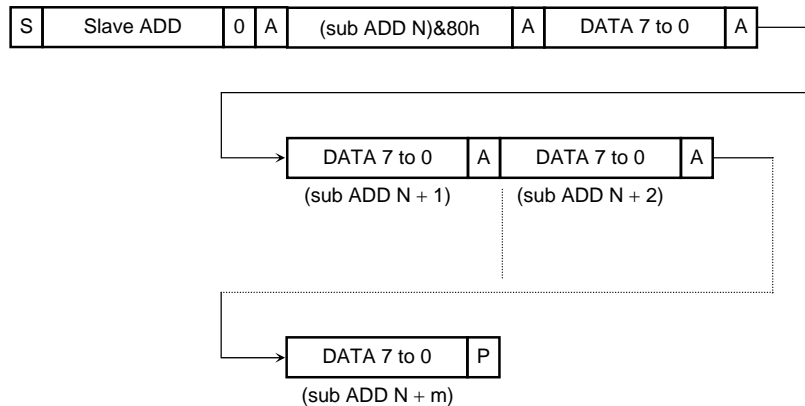
1) Continuation transmission

(An address to change is specified. At this time, MSB of a sub-address is set as 0.)



2) Auto increment

(Sub address are set to increment from N one by one. MSB of a sub-address is set as 1.)



(2) Read mode

The slave address became the read mode by changing the 8 Bit of the slave address from 0 to 1.

The data output from TB2932HQ starts after the micro controller receives the ACK 1 bit which follows a slave address.

Stop condition are shown in the under the map.

The micro controller shall send the stop condition P after it sent the reversed Acknowledge (high) in case of the read mode finished.

The data transmission became not available condition if the micro controller intended to send the stop condition P expect for this procedure because this IC occupies the data bus until the micro controller send the start conditions again.



.....send a DATA from microcontroller.

.....send a DATA from TB2932HQ.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Peak supply voltage (0.2 s)	V _{CC (surge)}	50	V
DC supply voltage	V _{CC (DC)}	28	V
Operation supply voltage	V _{CC (opr)}	18	V
Output current (peak)	I _{O (peak)}	9	A
Power dissipation	P _D (Note 19)	125	W
Operation temperature	T _{opr}	-40 to 85	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note 19: Package thermal resistance $\theta_{j-T} = 1^{\circ}\text{C}/\text{W}$ (typ.) (Ta = 25°C, with infinite heat sink)

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

Electrical Characteristics

(unless otherwise specified, $V_{CC} = 13.2\text{ V}$, $f = 1\text{ kHz}$, $R_L = 4\ \Omega$, $T_a = 25^\circ\text{C}$)

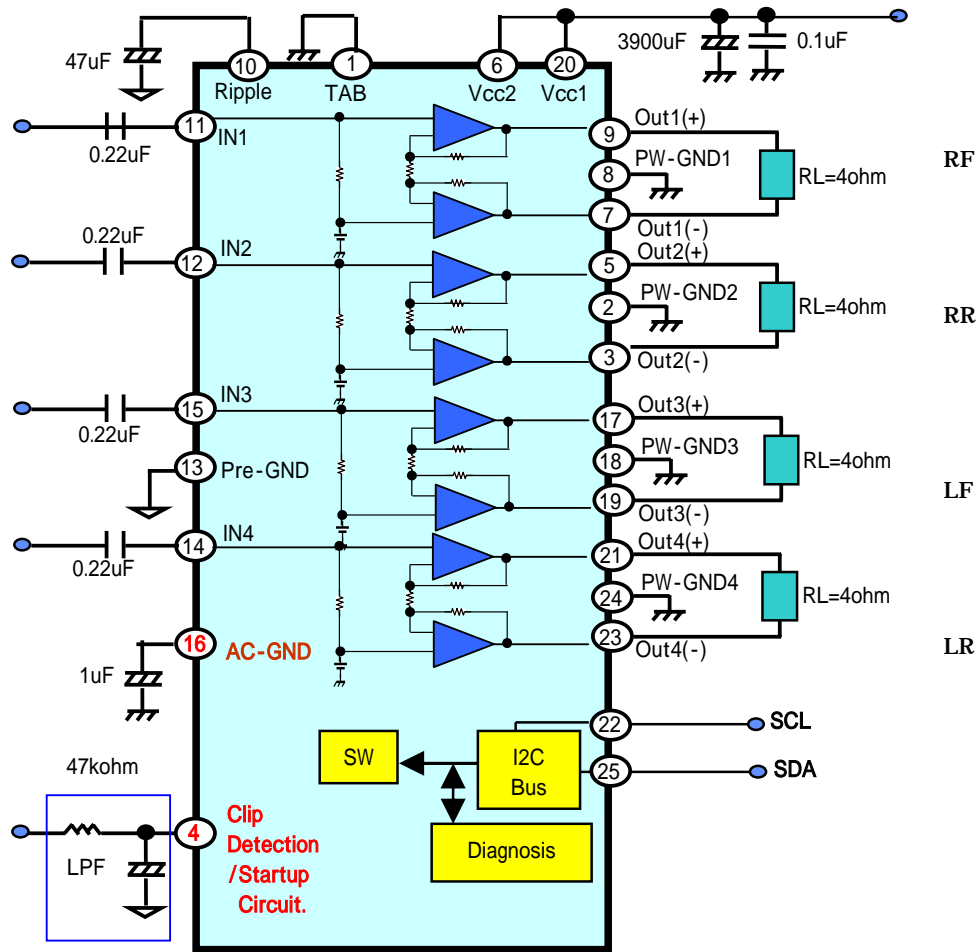
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Quiescent current	I_{CCQ}	—	$V_{IN} = 0$	—	160	320	mA
Output power	$P_{OUT\ MAX\ (1)}$	—	$V_{CC} = 15.2\text{ V}$, max POWER	—	43	—	W
	$P_{OUT\ MAX\ (2)}$	—	$V_{CC} = 14.4\text{ V}$, max POWER	—	41	—	
	$P_{OUT\ (1)}$	—	$V_{CC} = 14.4\text{ V}$, THD = 10%	24	27	—	
	$P_{OUT\ (2)}$	—	THD = 10%	—	23	—	
Output power ($R_L = 2\ \Omega$)	$P_{OUT\ MAX\ (3)}$	—	$V_{CC} = 14.4\text{ V}$, max POWER	—	70	—	W
	$P_{OUT\ MAX\ (4)}$	—	$V_{CC} = 13.7\text{ V}$, max POWER	—	64	—	
	$P_{OUT\ (3)}$	—	$V_{CC} = 14.4\text{ V}$, THD = 10%	42	45	—	
	$P_{OUT\ (4)}$	—	THD = 10%	—	39	—	
Total harmonic distortion	THD (1)	—	$P_{OUT} = 5\text{ W}$	—	0.007	0.1	%
	THD (2)	—	$V_O = 2V_{rms}$, $G_v = 12\text{ dB}$	—	0.005	0.1	
Voltage gain	$G_V\ (1)$	—	$V_{OUT} = 0.775\text{ V}_{rms}$	25	26	27	dB
	$G_V\ (2)$	—	$V_{OUT} = 0.775\text{ V}_{rms}$, $G_v = 12\text{ dB}$	11	12	13	
Voltage gain ratio	ΔG_V	—	$V_{OUT} = 0.775\text{ V}_{rms}$	-1.0	0	1.0	dB
Output noise voltage	$V_{NO}\ (1)$	—	$R_g = 0\ \Omega$, DIN45405	—	70	—	μV_{rms}
	$V_{NO}\ (2)$	—	$R_g = 0\ \Omega$, BW = 20 Hz~20 kHz	—	60	100	
	$V_{NO}\ (3)$	—	$R_g = 0\ \Omega$, BW = 20 Hz~20 kHz $G_v = 12\text{ dB}$	—	12	30	
Ripple rejection ratio	R.R.	—	$f_{rip} = 100\text{ Hz}$, $R_g = 620\ \Omega$ $V_{rip} = 0.775\text{ V}_{rms}$	50	65	—	dB
Cross talk	C.T.	—	$R_g = 620\ \Omega$ $V_{OUT} = 0.775\text{ V}_{rms}$	—	70	—	dB
Output offset voltage	V_{OFFSET}	—	—	-100	0	100	mV
Input resistance	R_{IN}	—	—	—	90	—	k Ω
Standby current	ISB1	—	Stand-by condition by BUS($V_{th} = \text{low}$)	—	0.01	1	μA
Standby current	ISB2	—	Stand-by condition by BUS($V_{th} = \text{high}$)	—	30	(60)	μA
Start-up controlled voltage (pin4)	Vst H	—	For operation	(2.4)	—	V_{CC}	V
	Vst L	—	For STBY, Pin10=0V	0	—	(1.0)	
Mute attenuation	ATT M	—	Mute: ON $V_{OUT} = 7.75\text{ V}_{rms} \rightarrow$ Mute: OFF	80	90	—	dB
Clip det THD level	CD (1)	—	Low (01H D = 0)	—	1	(2.5)	%
	CD (2)	—	High (01H D = 1)	5	10	15	

Note 20: ISB specification will be decided to after final evaluation on tolerance spls.

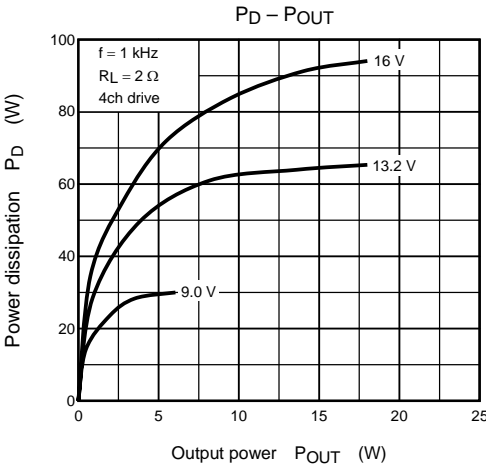
Diagnosis/Bus Specification

Characteristics	Test Condition	Min	Typ.	Max	Unit
Turn on diagnosis (power amplifier mode)					
Short to GND det.	Under stand-by condition	—	—	1.2	V
Short to V _{CC} det.		V _{CC} - 1.2	—	—	V
Shorted load		—	—	0.5	Ω
Open load		85	—	—	Ω
Normal load		1.5	—	45	Ω
Turn on diagnosis (line driver mode)					
Short to GND det.	Under stand-by condition	—	—	1.2	V
Short to V _{CC} det.		V _{CC} - 1.2	—	—	V
Shorted load		—	—	2	Ω
Open load		330	—	—	Ω
Normal load		6	—	180	Ω
Permanent diagnosis (power amplifier and line driver mode)					
Short to GND det.	Power amplifier in mute or play	—	—	1.2	V
Short to V _{CC} det.		V _{CC} - 1.2	—	—	V
Shorted load	Power amp mode only	—	0.5	—	Ω
Offset detection	Power amplifier in play (no signal)	—	+/-2	—	V
Current detector threshold 1		250		500	mA
Current detector threshold 2		100		300	mA
I ² C bus interface					
Clock frequency		—	400	—	kHz

Test Circuit



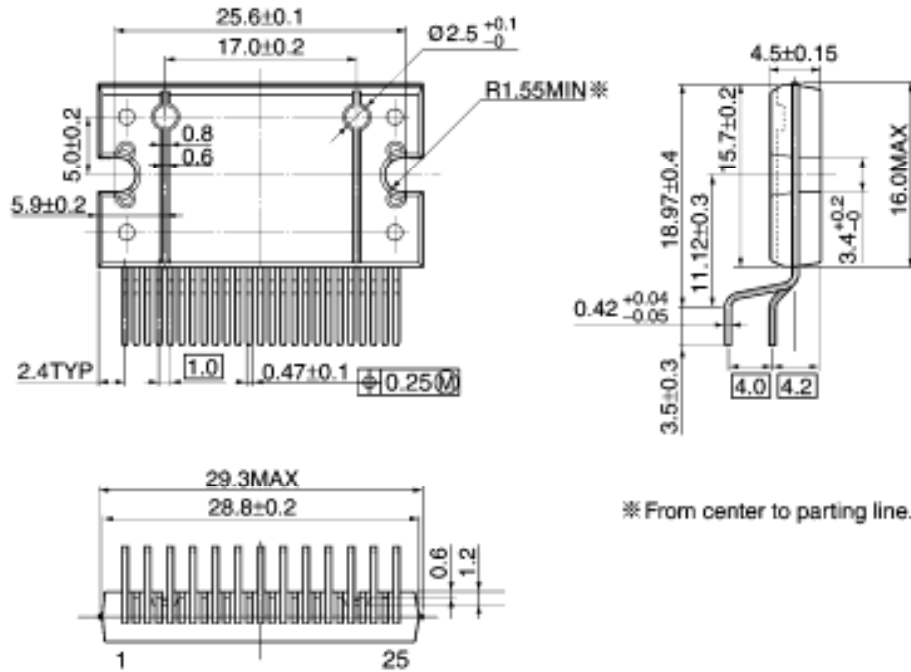
Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.



Package Dimensions

HZIP25-P-1.00F

Unit: mm



* From center to parting line.

Weight: 7.7 g (typ.)

- Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. For details on how to connect a protection circuit such as a current limiting resistor or back electromotive force adsorption diode, refer to individual IC datasheets or the IC databook. IC breakdown may cause injury, smoke or ignition.
- Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.
- Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.
- Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the Thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.
- Heat Radiation Design
When using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.
- Installation to Heat Sink
Please install the power IC to the heat sink not to apply excessive mechanical stress to the IC. Excessive mechanical stress can lead to package cracks, resulting in a reduction in reliability or breakdown of internal IC chip. In addition, depending on the IC, the use of silicon rubber may be prohibited. Check whether the use of silicon rubber is prohibited for the IC you intend to use, or not. For details of power IC heat radiation design and heat sink installation, refer to individual technical datasheets or IC databooks.

About solderability, following conditions were confirmed

- Solderability

- (1) Use of Sn-37Pb solder Bath

- solder bath temperature = 230°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

- (2) Use of Sn-3.0Ag-0.5Cu solder Bath

- solder bath temperature = 245°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

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060116EBA

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