Preliminary

TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

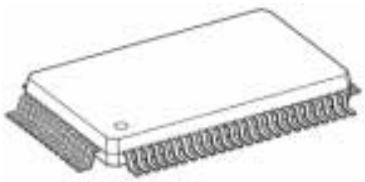
TB1311AFG

Audio SW, Video SW, Sync Separation and H/V Frequency Counter IC for TVs

The TB1311AFG includes audio and video SW blocks, prefilters for A/D converters, sync separators, and an H/V format detector for TV signals.

The TB1311AFG contributes to a reduction in the proportion of the PCB occupied by LCR filters and to the simplification of designs on analog interfaces.

The TB1311AFG has an I^2CBUS interface through which various functions can be controlled.



P-QFP80-1420-0.80C

Weight: 1.6 g (typ.)

Features

Audio SW block
- Audio (L/R) inputs
- Audio (L/R) output: 3 channels

Audio block
- Attenuator

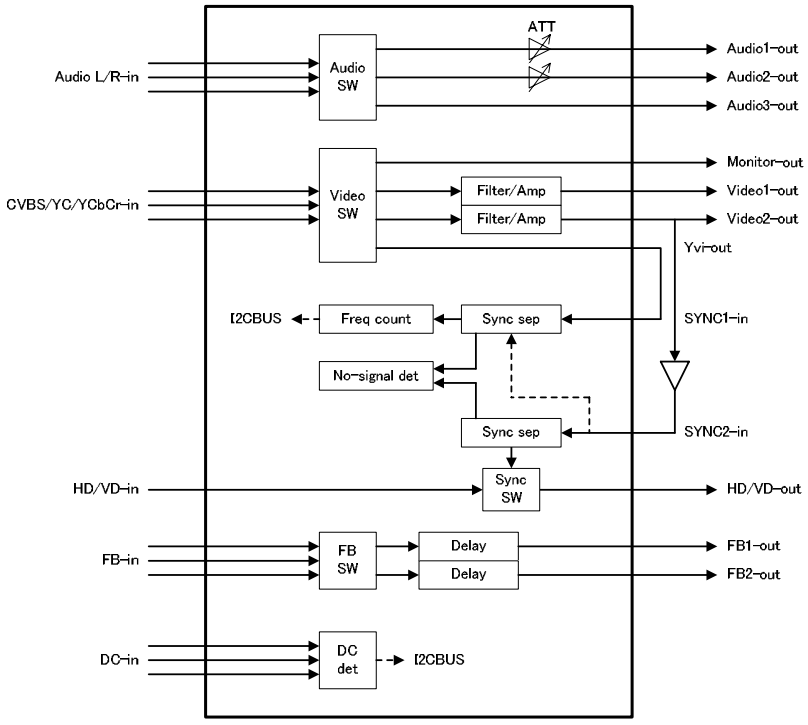
Video SW block
- CVBS inputs
- Y/C inputs
- Component video inputs (co-use as RGB inputs)
- SCART inputs
- Output: 2 channels
- Monitor output

Video block
- Gain switching: -3 dB / 0 dB / +3 dB
- Bandwidth filter: prefilter for ADC; 4.5 to 46 MHz variable

Sync separation block
- Supports 525/30p/60i/60p, 625/50i/50p, 750/50p/60p, 1125/24p/24sf/25p/30p/50i/60i/50p/60p, 1250/50i, VGA @60, SVGA@60, XGA@60, SXGA@60, UXGA@60
- HD/VD input: 1 channel; positive and negative input acceptable
- HD/VD output: positive and negative output selectable
- Masking pseudo-sync for the copyguard signal

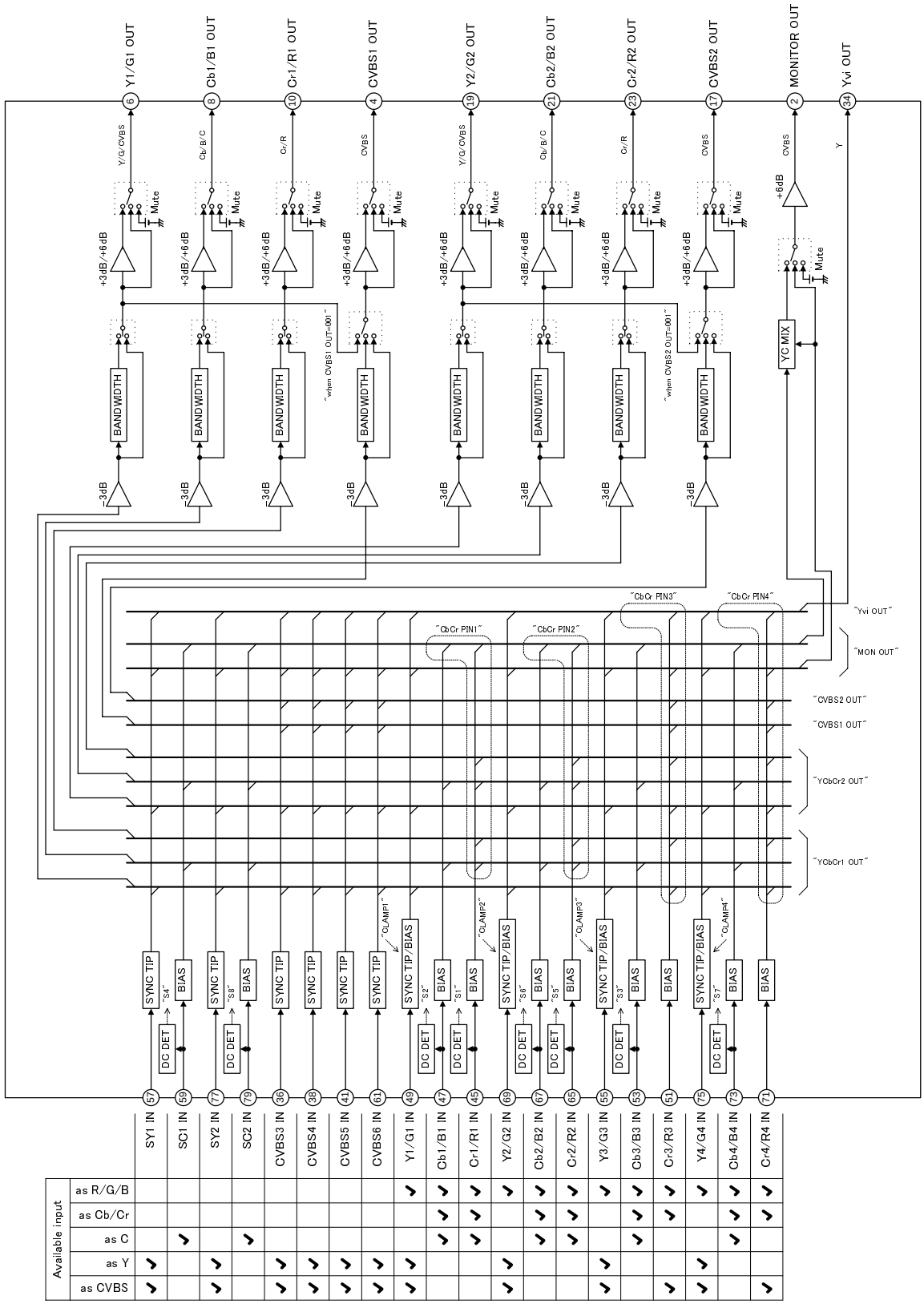
Others
- Line detector for Japanese D-pin
- S2, S1, insertion detection for S-pin
- Horizontal and vertical frequency counter
- Format detection circuit to input signal
- No-input detection
- Automatic sync process switching mode
- Programmable number of audio/video inputs

Block Diagram 1 (Simplified Overview)



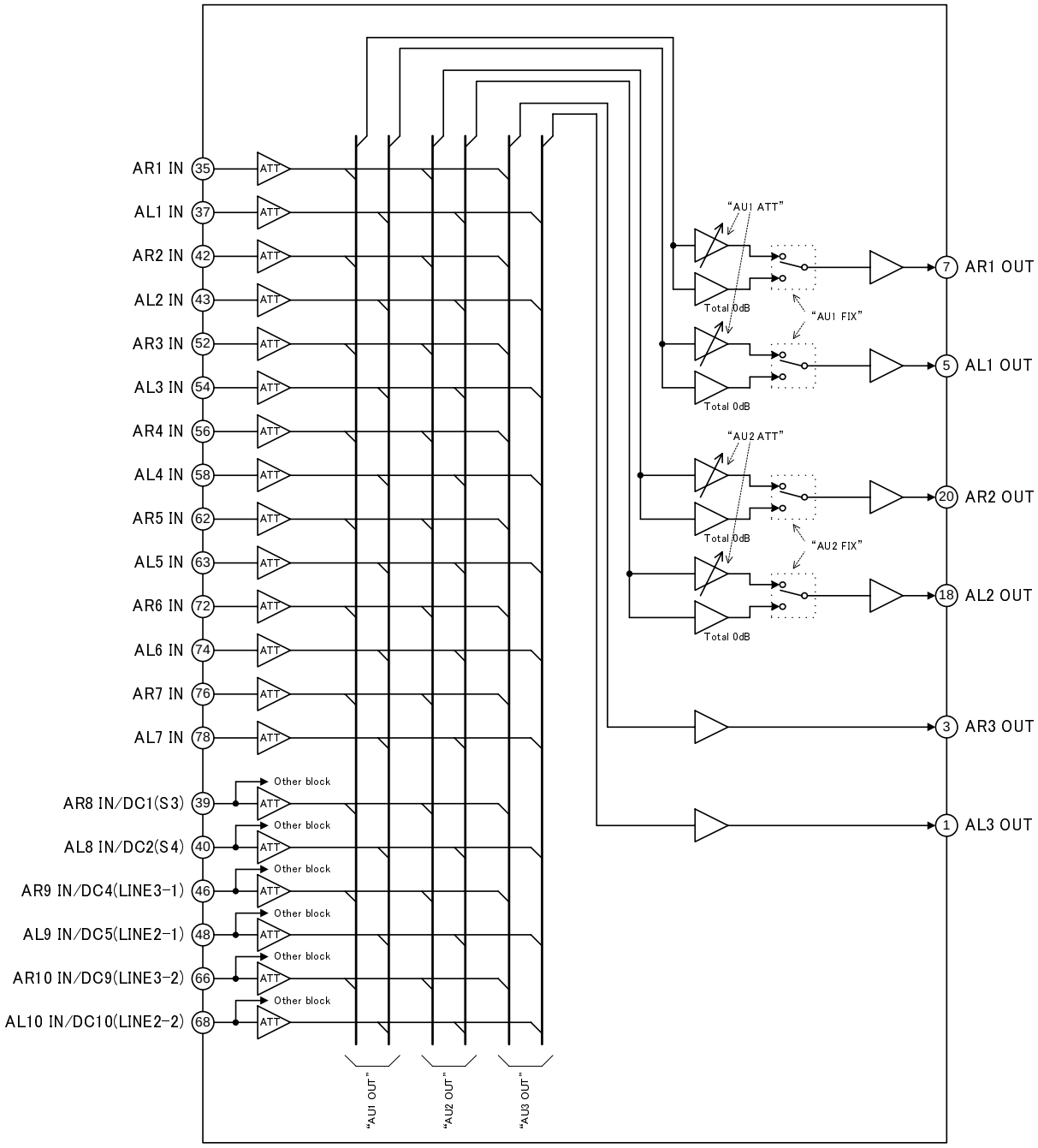
This IC does not support weak signals, ghost signals or other nonstandard signals.
Some functional blocks, circuits, or constants may be omitted or simplified in the block diagram for explanatory purposes.

Block Diagram 2 (Video Block)



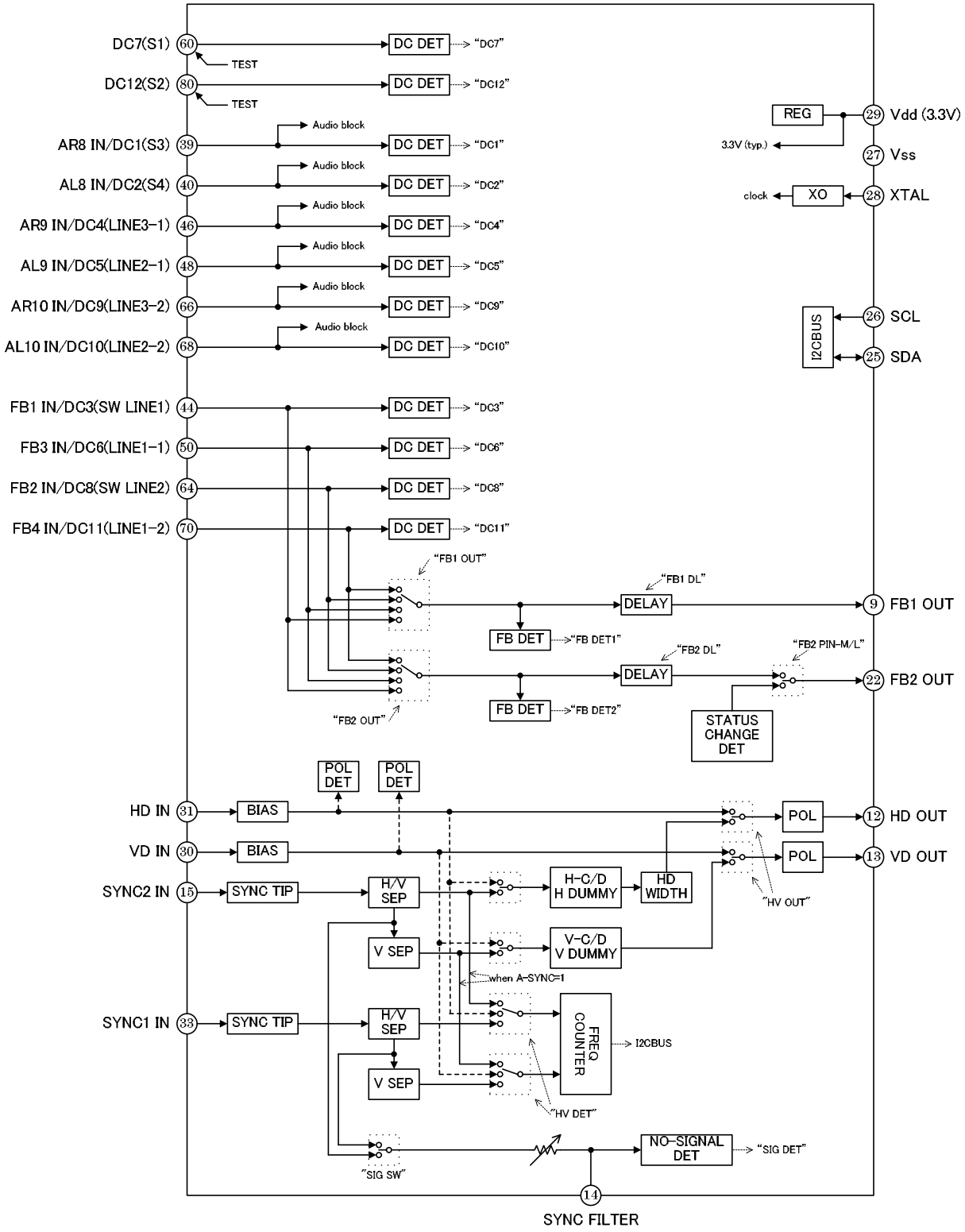
Some functional blocks, circuits, or constants may be omitted or simplified in the block diagram for explanatory purposes.

Block Diagram 3 (Audio Block)



Some functional blocks, circuits, or constants may be omitted or simplified in the block diagram for explanatory purposes.

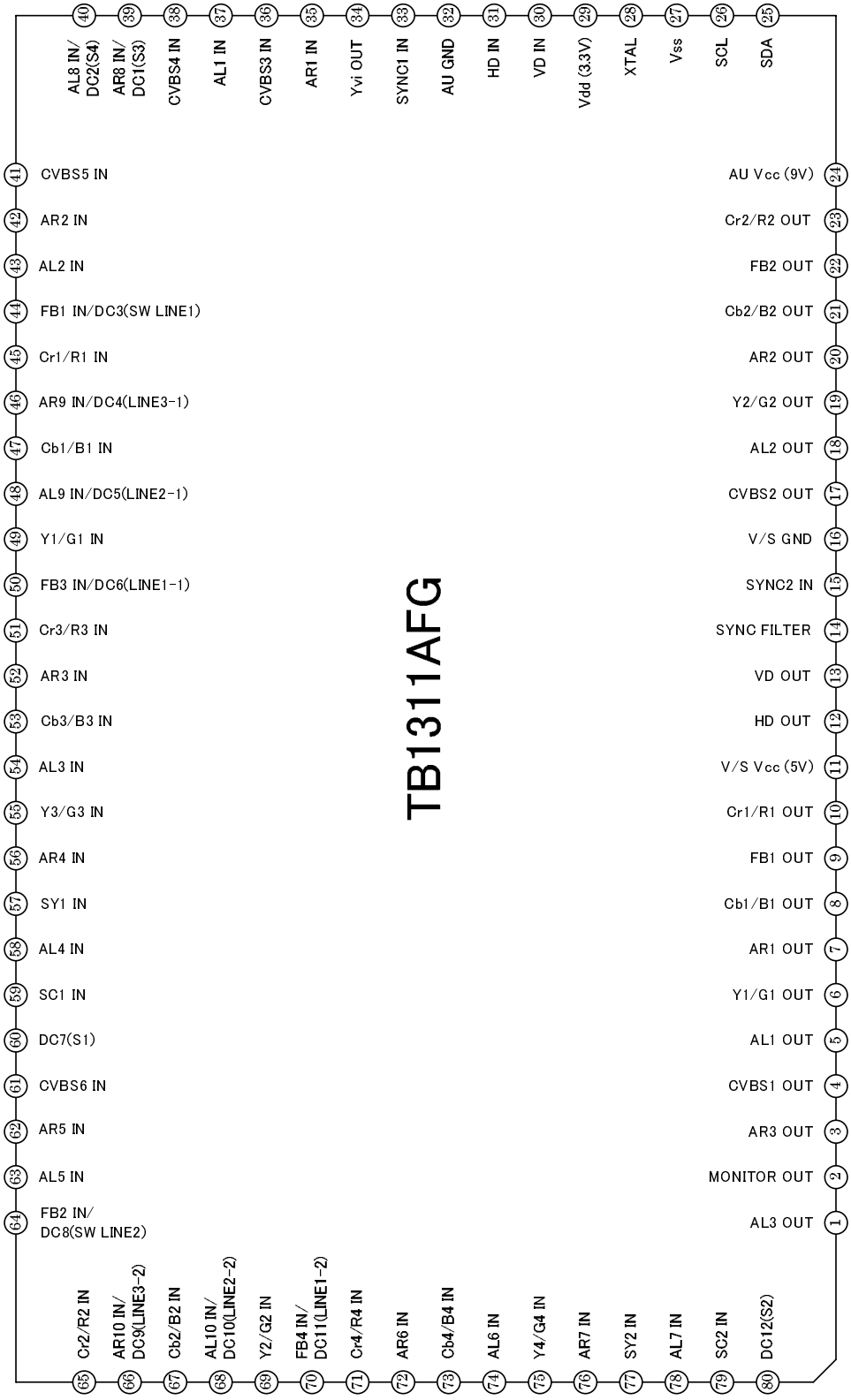
Block Diagram 4 (Other Blocks)



This IC does not support weak signals, ghost signals or other nonstandard signals.

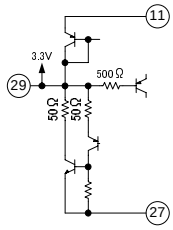
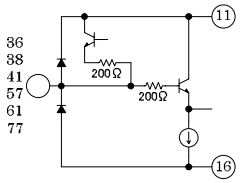
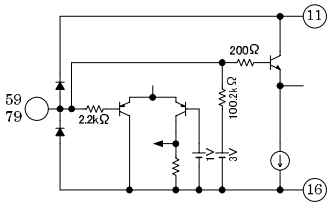
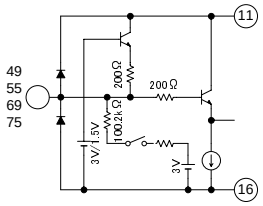
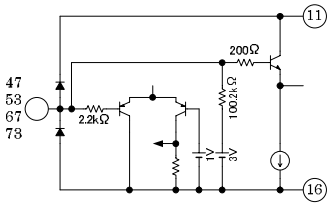
Some functional blocks, circuits, or constants may be omitted or simplified in the block diagram for explanatory purposes.

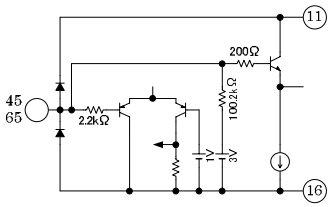
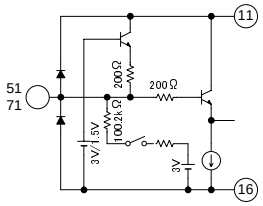
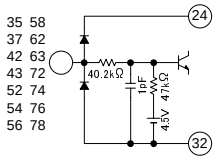
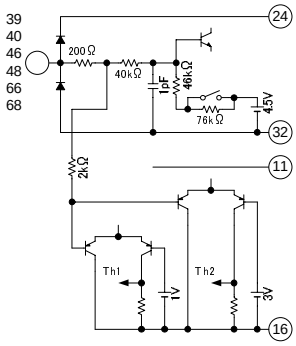
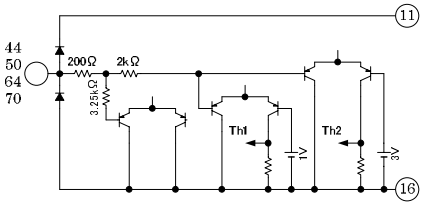
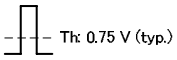
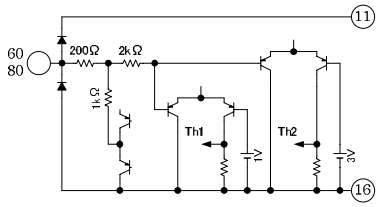
Pin Assignment

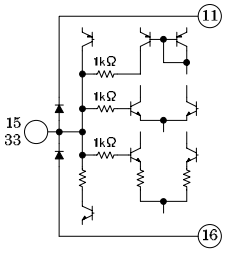
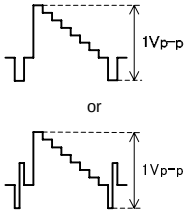
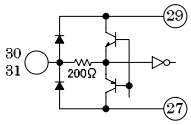
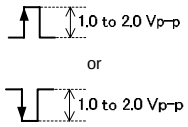
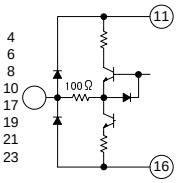
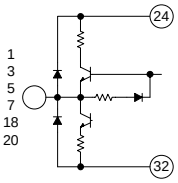
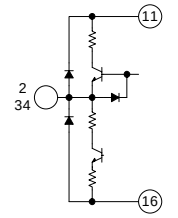
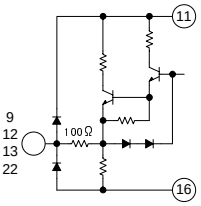
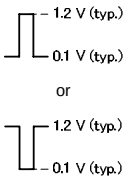
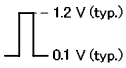
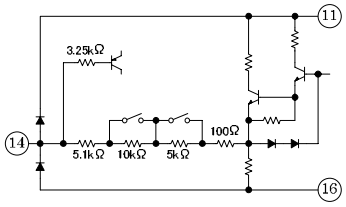


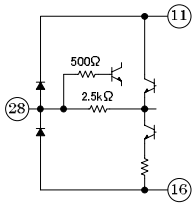
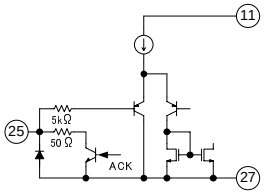
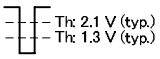
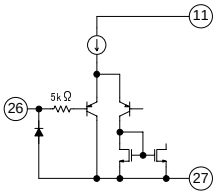
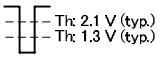
Pin Functions

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
29	V_{dd} (3.3 V)	V_{CC} pin for the logical circuits. Supply power through a resistor from pin 11 as in the Application Circuit. This pin voltage is clipped to 3.3 V (typ.) by the internal regulator.		3.3 V (typ.)
27	Vss	GND pin for the logical circuits.	—	—
11	V/S V_{CC} (5 V)	V_{CC} pin for the sync and video circuits. Connect 5.0 V (typ.)	—	5.0 V (typ.)
16	V/S GND	GND pin for the sync and video circuits.	—	—
24	AU V_{CC} (9 V)	V_{CC} pin for the audio circuits. Connect 9.0 V (typ.)	—	9.0 V (typ.)
32	AU GND	GND pin for the audio circuits.	—	—
36 38 41 57 61 77	CVBS3 IN CVBS4 IN CVBS5 IN CVBS6 IN SY1 IN SY2 IN	CVBS or Y input pin. Input the CVBS or Y signal in NTSC, PAL or SECAM via a clamp capacitor.		Sync tip level: 2.3 V (typ.) Y/CVBS signal amplitude: 1.0 Vp-p (with sync)
59 79	SC1 IN SC2 IN	Chroma signal input pin. Input C signal via a capacitor. The voltage of this pin is detected and the status is returned to the I^2CBUS Read functions, S4 or S8. It is used for detecting whether the S-pin is connected or not.		2.9 V bias (typ.) Burst signal amplitude: 0.3 Vp-p
49 69 55 75	Y1/G1 IN Y2/G2 IN Y3/G3 IN Y4/G4 IN	Y, G or CVBS input pin. Input the signal via a clamp capacitor. The clamp system is selectable by CLAMP1, 2, 3 or 4 registers.		Sync tip level: 2.3 V (typ.) Bias level: 2.9 V (typ.) Y/G/CVBS signal amplitude: 1.0 Vp-p (with sync)
47 67 53 73	Cb1/B1 IN Cb2/B2 IN Cb3/B3 IN Cb4/B4 IN	Cb, B or C input pin. Input the signal via a capacitor.		2.9 V bias (typ.) Cb/B signal amplitude: 0.7 Vp-p (without sync) Burst signal amplitude: 0.3 Vp-p

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
45 65	Cr1/R1 IN Cr2/R2 IN	Cr, R or C input pin. Input the signal via a capacitor.		2.9 V bias (typ.) Cr/R signal amplitude: 0.7 Vp-p (without sync) Burst signal amplitude: 0.3 Vp-p
51 71	Cr3/R3 IN Cr4/R4 IN	Cr, R or CVBS input pin. Input the signal via a capacitor. The clamp system is changed according to CbCr PIN3 or 4 registers.		Sync tip level: 2.3 V (typ.) Bias level: 2.9 V (typ.) Cr/R signal amplitude: 0.7 Vp-p (without sync) CVBS signal amplitude: 1.0 Vp-p (with sync)
35 37 42 43 52 54 56 58 62 63 72 74 76 78	AR1 IN AL1 IN AR2 IN AL2 IN AR3 IN AL3 IN AR4 IN AL4 IN AR5 IN AL5 IN AR6 IN AL6 IN AR7 IN AL7 IN	Audio input pin. Input the signal via a resistor and a capacitor. When the resistor value is 5.6 kΩ, the internal gain becomes 0 dB (typ.).		Bias level: 4.4 V (typ.) Audio input: 2.8 V p-p (100%)
39 40 46 48 66 68	AR8 IN/DC1 AL8 IN/DC2 AR9 IN/DC4 AL9 IN/DC5 AR10 IN/DC9 AL10 IN/DC10	Audio or DC voltage input pin. The input type is changed by AU8 PIN, AU9 PIN or AU10 PIN. In the case of use as audio input, input the signal via a resistor and a capacitor. When the resistor value is 5.6 kΩ, the internal gain becomes 0 dB (typ.). In the case of use as DC voltage input, input the signal via a resistor for protection.		Bias level: 4.4 V (typ.) Audio input: 2.8 V p-p (100%)
44 64 50 70	FB1 IN/DC3 FB2 IN/DC8 FB3 IN/DC6 FB4 IN/DC11	FB (Fast Blanking) signal or DC voltage input pin. Connect a resistor between this pin and GND. In the case of use as DC voltage input, input the signal via a resistor for protection.		FB input: 
60 80	DC7 DC12	DC voltage input. Input the signal via a resistor for protection purposes. This pin is also used as a test signal output pin for shipping only.		DC

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
33 15	SYNC1 IN SYNC2 IN	Composite SYNC input pin to separate into H- and V-SYNC. Input the signal via a clamp capacitor. Remark: SYNC1 IN is not available, when A-SYNC = 1 (ON).		Sync tip level: 1.8 V (typ.) 
31 30	HD IN VD IN	HD or VD input pin. Input a separated horizontal or vertical sync signal (1.0 to 2.0 Vp-p) via a resistor and a coupling capacitor. The polarity of the input signal is detected and its leading edge becomes a timing trigger.		1.45 V bias (typ.) 
4 6 8 10 17 19 21 23	CVBS1 OUT Y1/G1 OUT Cb1/B1 OUT Cr1/R1 OUT CVBS2 OUT Y2/G2 OUT Cb2/B2 OUT Cr2/R2 OUT	Video signal output pin. Refer to Bus Control Functions for details of the output from each pin.		AC: -3, 0 or +3 dB (typ.)
5 7 18 20 1 3	AL1 OUT AR1 OUT AL2 OUT AR2 OUT AL3 OUT AR3 OUT	Audio signal output pin. Refer to Bus Control Functions for details of the output from each pin.		
2	MONITOR OUT	Video signal output pin for a monitor output. Refer to Bus Control Functions for details of the output from the pin.		AC: +6 dB (typ.)
34	Yvi OUT	Video signal output pin for the sync separation circuit. Refer to Bus Control Functions for details of the output from the pin.		AC: 0 dB (typ.)
12 13	HD OUT VD OUT	HD or VD output pin. The polarity of the output is selectable by HV-POL register. The tailing edge of the VD-OUT has a jitter. Use the leading edge only.		
9 22	FB1 OUT FB2 OUT	FB output pin. Note: If necessary, a resistor can be added between the pin and GND to improve the transient of the falling edge. The value of the resistor must be 440 Ω or more. However, when the resistor is added, the leak pulse from FB edges to video signals is also increased.		
14	SYNC FILTER	A filter pin for sync detection. Connect a capacitor between this pin and GND.		—

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
28	XTAL	Crystal connection pin. Connect a 3.579545 MHz crystal for NTSC demodulation to generate internal clocks.		—
25	SDA	SDA pin for I²CBUS.		 H to L: 1.3 V (typ.) L to H: 2.1 V (typ.)
26	SCL	SCL pin for I²CBUS.		 H to L: 1.3 V (typ.) L to H: 2.1 V (typ.)

BUS Control Map

Write Mode Slave Address: DE_H

SA	D7	D6	D5	D4	D3	D2	D1	D0	PRESET
00	CVBS1OUT			fc HALF1	YCbCr1OUT				00000000
01	CVBS2OUT			fc HALF2	YCbCr2OUT				00000000
02	(0)	FILPASS2	FILPASS1	YC MIX	MON OUT				00000000
03	f0 SW1	BANDWIDTH1							00000000
04	f0 SW2	BANDWIDTH2							00000000
05	CVBS2 GAIN		YCbCr2 GAIN		CVBS1 GAIN		YCbCr1 GAIN		00000000
06	CbCr PIN4	CbCr PIN3	CbCr PIN2	CbCr PIN1	CLAMP4	CLAMP3	CLAMP2	CLAMP1	00000000
07	FB2 DL	FB2 MUTE	FB2 OUT		FB1 DL	FB1 MUTE	FB1 OUT		00000000
08	AU2 OUT				AU1 OUT				00010001
09	AU1 FIX	AU1 ATT							00000000
0A	AU2 FIX	AU2 ATT							00000000
0B	AU10 PIN	AU9 PIN	AU8 PIN	(0)	AU3 OUT				00000001
0C	HV-SEP2		HV-SEP1		(0)	(0)	SYNC LPF2	SYNC LPF1	00000000
0D	A-SYNC	SIG LPF	(0)	(0)	Yvi OUT				00000000
0E	(0)	PS MASK	V-DET	HD WIDTH	HV POL	(0)	HV DET	HV OUT	00000000
0F	H DMY	V DMY	FB2 PIN-M	HV FREQ2					00000000
10	H COUNT MAX				(0)	H COUNT MIN			00000000
11	SIG DET N				SIG RESET N				00000000
12	(0)TEST1	FB2 PIN-L	SIG RESET	SIG SW	SIG DET IMPE		SIG DET LVL		00000000
13	(00000000) TEST2								00000000
14	(00000000) TEST3								00000000

Remark: SA = Sub-address.
NOTE: Set 0 (zero) on bits written as (0).

Read Mode Slave Address: DF_H

	D7	D6	D5	D4	D3	D2	D1	D0
0	POR	H FM2	V FM2	H IN	V IN	V-SYNC-W	HD-POL	VD-POL
1	H FORMAT				V FORMAT			*
2	FB DET2	FB DET1	SIG DET	HV-OUT FORMAT				
3	DC4		DC3		DC2		DC1	
4	DC8		DC7		DC6		DC5	
5	DC12		DC11		DC10		DC9	
6	S8	S7	S6	S5	S4	S3	S2	S1
7	H FREQ DET							
8	V FREQ DET							

*: Undefined

Bus Control Functions

Write Mode

Register Name	Function	Preset Value
CVBS1(2)OUT	Selects the output from CVBS1(2) OUT (pin 4 (17)) for SCART connector. 000: Mute 001: Outputs the same Y, selected by YCbCr1(2) OUT 010: CVBS3 (pin 36) 011: CVBS4 (pin 38) 100: CVBS5 (pin 41) 101: CVBS6 (pin 61) 110: Cr3 (as CVBS) (pin 51) 111: Cr4 (as CVBS) (pin 71)	Mute (000)
fc HALF1(2)	Switches the frequency of bandwidth limit filters for Cb/Cr The cutoff frequency of bandwidth limit filters for Cb/Cr is 1/2 to Y. 0: OFF (same for 3 outputs) 1: ON (1/2 fc for Cb/Cr)	OFF (0)
YCbCr1(2)OUT	Selects the output from Y/Cb/Cr OUT1(2) (pins 6, 8, 10 (19, 21, 23)). (Y OUT, Cb OUT, Cr OUT) = 0000: Mute (mute, mute, mute) 0001: SY1 (pin 57), SC1 (pin 59), mute 0010: SY2 (pin 77), SC2 (pin 79), mute 0011: CVBS3 (pin 36), mute, mute 0100: CVBS4 (pin 38), mute, mute 0101: CVBS5 (pin 41), mute (Cr1; pin 45, when CbCr PIN1 = 1), mute 0110: CVBS6 (pin 61), mute (Cr2; pin 65, when CbCr PIN2 = 1), mute 0111: Y1 (pin 49), Cb1 (pin 47), Cr1; pin 45 (mute, when CbCr PIN1 = 1) 1000: Y2 (pin 69), Cb2 (pin 67), Cr2; pin 65 (mute, when CbCr PIN2 = 1) 1001: Y3 (pin 55), Cb3 (pin 53), Cr3; pin 51 (mute, when CbCr PIN3 = 1) 1010: Y4 (pin 75), Cb4 (pin 73), Cr4; pin 71 (mute, when CbCr PIN4 = 1) 1011: Cr3 (as CVBS) (pin 51), mute, mute 1100: Cr4 (as CVBS) (pin 71), mute, mute 1101 to 1111: Not available Refer also to Function Descriptions.	Mute (0000)
FILPASS1(2)	Switches the bandwidth limit filter 1 (2). 0: OFF (filters active) 1: ON (bypass)	OFF (0)
YC MIX	Mixes Y with C for MONITOR OUT (pin 2). 0: OFF (for CVBS) 1: MIX (Y+C)	OFF (0)
MON OUT	Selects the output from MONITOR OUT (pin 2). When YC MIX = 1, a mixed signal is output. 0000: Mute 0001: SY1 (pin 57) (+SC1 (pin 59)) 0010: SY2 (pin 77) (+SC2 (pin 79)) 0011: CVBS3 (pin 36) 0100: CVBS4 (pin 38) 0101: CVBS5 (pin 41) (+Cr1 (pin 45), when CbCr PIN1 = 1) 0110: CVBS6 (pin 61) (+Cr2 (pin 65), when CbCr PIN2 = 1) 0111: Y1 (pin 49) (+Cb1 (pin 47)) 1000: Y2 (pin 69) (+Cb2 (pin 67)) 0001: Y3 (pin 55) (+Cb3 (pin 53)) 1010: Y4 (pin 75) (+Cb4 (pin 73)) 1011: Cr3 (CVBS) (pin 51)) 1100: Cr4 (CVBS) (pin 71)) 1101 to 1111: Not available Refer also to Function Descriptions.	Mute (0000)
f0 SW1(2)	Switches the f0 of the bandwidth limit filter for YCbCr(RGB) 0: LOW 1: HIGH Note: This function is not valid for the filter for CVBS. For the CVBS filter, this data is fixed to 0: LOW.	LOW (0)
BANDWIDTH1(2)	Switches the f0 of the bandwidth limit filter for YCbCr(RGB) and CVBS 0000000: MIN (low) 1111111: MAX (high) Note: While HD, VD or FB-out is output, according as the f0 is set to lower, the crosstalk from HD, VD, FB or SYNC-in to video-outs becomes bigger.	MIN (0000000)

Register Name	Function	Preset Value
CVBS1(2) GAIN	Switches output gain. Gain of CVBS1(2)-OUT output (pin 4 (17)) is controlled. 00: 0 dB 01: -3 dB 10: +3 dB 11: Not available	0 dB (00)
YCbCr1(2) GAIN	Switches output gain. Gain of YCbCr1(2)-OUT outputs (pins 6,8,10 (19, 21, 23)) are controlled. 00: 0 dB 01: -3 dB 10: +3 dB 11: Not available Remark: GAIN = 01 (-3 dB) is recommended for the 1125/50p/60p format since this offers superior frequency characteristics to those of other modes.	0 dB (00)
CbCr PIN1	Changes CbCr1-IN pins function. 0: Component Cb/Cr input (pin 49: Y/G, pin 47: Cb/B, pin 45: Cr/R, pin 41: CVBS) 1: Separated C input (pin 49: Y, pin 47: C, pin 41: Y, pin 45: C)	Cb/Cr input (0)
CbCr PIN2	Changes CbCr2-IN pins function. 0: Component Cb/Cr input (pin 69: Y/G, pin 67: Cb/B, pin 65: Cr/R, pin 61: CVBS) 1: Separated C input (pin 69: Y, pin 67: C, pin 61: Y, pin 65: C)	Cb/Cr input (0)
CbCr PIN3	Changes CbCr3-IN pins function. 0: Component Cb/Cr input (pin 55: Y/G, pin 53: Cb/B, pin 51: Cr/R) 1: Separated C input (pin 55: Y, pin 53: C, pin 51: CVBS)	Cb/Cr input (0)
CbCr PIN4	Changes CbCr4-IN pins function. 0: Component Cb/Cr input (pin 75: Y/G, pin 73: Cb/B, pin 71: Cr/R) 1: Separated C input (pin 75: Y, pin 73: C, pin 71: CVBS)	Cb/Cr input (0)
CLAMP1(2,3,4)	Switches Y1 (2, 3, 4) clamping mode. The clamping mode for pin 49 (69, 55, 75) is set. 0: SYNC TIP CLAMP (for Y/G with sync) 1: BIAS (for RGB without sync)	SYNC TIP (0)
FB1(2) DL	Turns on the delay to FB1 (2)-OUT (pin 9 (22)). 0: OFF 1: ON (+30 ns)	OFF (0)
FB1(2) MUTE	Mutes FB1 (2)-OUT (pin 9 (22)). 0: OFF 1: MUTE	OFF (0)
FB1(2) OUT	Switches the output from FB1(2)-OUT (pin 9 (22)). 00: FB1 (pin 44) 01: FB2 (pin 64) 10: FB3 (pin 50) 11: FB4 (pin 70)	FB1 (00)
AU1(2,3) OUT	Switches audio outputs from AL/AR1 (2,3)-OUT (pins 5/7 (18/20, 1/3)). 0000: MUTE 0001: AL/AR1 (pins 37/35) 0010: AL/AR2 (pins 43/42) 0011: AL/AR3 (pins 54/52) 0100: AL/AR4 (pins 58/56) 0101: AL/AR5 (pins 63/62) 0110: AL/AR6 (pins 74/72) 0111: AL/AR7 (pins 78/76) 1000: AL/AR8 (pins 40/39) 1001: AL/AR9 (pins 48/46) 1010: AL/AR10 (pins 68/66) 1011 to 1111: Not available	AL/AR1 (0001)

Register Name	Function	Preset Value
AU1(2) FIX	Sets audio volume to AL/AR1 (2)-OUT (pin 5/7 (18/20)) fixed. 0: Fixed gain (0 dB) 1: OFF (Attenuated by AU1(2) ATT) Note: The DC offset on audio outputs occurs when this function is turned on or off. While audio outputs are valid, switching of this function is not available. Remark: The gain is defined where the series-connected resistor is 5.6 kΩ.	Fixed (0)
AU1(2) ATT	Attenuates audio volume to AL/AR1(2)-OUT (pins 5/7 (18/20)). 0000000: MIN 1111111: MAX	MIN (0000000)
AU8 PIN	Changes the AL/AR8-IN pin function. 0: DC input for S-pin (pin 39: DC1(S3), pin 40: DC2(S4)) 1: Audio-IN8 (pin 39: AR8, pin 40: AL8)	DC (0)
AU9 PIN	Changes the AL/AR9-IN pin function. 0: DC input for D-pin (pin 46: DC4(LINE2), pin 48: DC5(LINE1)) 1: Audio-IN9 (pin 46: AR9, pin 48: AL9)	DC (0)
AU10 PIN	Changes the AL/AR10-IN pin function. 0: DC input for D-pin (pin 66: DC9(LINE2), pin 68: DC10(LINE1)) 1: Audio-IN10 (pin 66: AR10, pin 68: AL10)	DC (0)
HV-SEP1(2)	Switches the separation level. The H/V sync separation level to SYNC1(2)-IN (pin 33 (15)) is switched. 00: LOW 11: HIGH Remark: The separation level is changed according to a ratio of negative sync width per 1H period.	LOW (00)
SYNC LPF1(2)	Turns on the LPF for the sync-tip clamp. SYNC LPF1(2) for SYNC1(2)-IN pin changes the speed of the sync-tip clamp response. Turn this function on for no-input detection. 0: OFF 1: ON	OFF (0)
A-SYNC	Automatic sync processing mode. Sync processing mode is changed in accordance with the results obtained by the internal format detection circuits. Format detection is performed for SYNC2-IN or HD/VD-IN signal selected by HV DET. The result of detection is returned to H FORMAT, V FORMAT, H FM2 and V FM2. HV FREQ setting is invalid when this mode is active. 0: OFF (Manual switching mode by HV FREQ2 setting) 1: ON Remark: SYNC1-IN (pin 33) is not available when A-SYNC = 1 (ON). Format detection and H/V separation are then executed for SYNC2-IN (pin 15).	OFF (0)
SIG LPF	Turns on the LPF for the sync input pin (pin 33; SYNC1-IN). When no-input detection for weak strength signals is required, turn this function on to reduce noise on the input. Turn this function off for detections such as H FORMAT, V FORMAT, H FREQ DET and V FREQ DET. 0: OFF 1: ON	OFF (0)
Yvi OUT	Switches the output from Yvi-OUT (pin 34). 0000: MUTE 0001: SY1 (pin 57) 0010: SY2 (pin 77) 0011: CVBS3 (pin 36) 0100: CVBS4 (pin 38) 0101: CVBS5 (pin 41) 0110: CVBS6 (pin 61) 0111: Y1 (pin 49) 1000: Y2 (pin 69) 1001: Y3 (pin 55) 1010: Y4 (pin 75) 1011: Cr3 (as CVBS) (pin 51) 1100: Cr4 (as CVBS) (pin 71) 1101 to 1111: Not available	MUTE (0000)
PS MASK	Switches the mask mode for pseudo-sync. 0: ON (Normal) 1: OFF (for “Sync on G”) (1) OFF mode is used for “Sync on G” input.	ON (0)

<table>
<tr><th>Register Name</th><th>Function</th><th>Preset Value</th></tr>
<tr><td>V-DET</td><td>Switches the V format detection mode.
0: 50/60Hz only 1: Full detection</td><td>50/60 only
(0)</td></tr>
<tr><td>HD WIDTH</td><td>Switches the width of HD-OUT (pin 12) from SYNC2-IN (pin 15).
0: WIDE 1: NARROW
Remark: HD WIDTH = 1 (NARROW) is recommended for the 1125/50p/60p format owing to crosstalk from HD-OUT to video signals so that spike noises on video signals will occur.</td><td>WIDE
(0)</td></tr>
<tr><td>HV-POL</td><td>Switches the polarity of HD/VD output.
The polarity of HD/VD OUT (pin 12, 13) is set.
0: Positive 1: Negative</td><td>Positive
(0)</td></tr>
<tr><td>HV DET</td><td>Selects the input for format detection.
When A-SYNC = 0 (Manual Mode)
0: SYNC1-IN (pin 33) 1: HD/VD-IN (pins 31/30)
When A-SYNC = 1 (Automatic Mode)
This function is invalid. The input is selected by HV OUT.</td><td>SYNC
(0)</td></tr>
<tr><td>HV OUT</td><td>Switches the outputs from HD/VD-OUT (pin 12/13).
0: SYNC2-IN (pin 15) 1: HD/VD-IN (pins 31/30)</td><td>SYNC2-IN
(0)</td></tr>
<tr><td>H DMY</td><td>Outputs the dummy HD at no input.
The frequency of the dummy HD output depends on the HV FREQ2 setting (when A-SYNC = OFF) or HV-OUT FORMAT (when A-SYNC = ON). No-input detection is based on H IN result.
0: OFF 1: ON (Dummy HD output at no input)
Note: The HD output does not synchronize with input sync, when A-SYNC = OFF and when a sync is input.</td><td>OFF
(0)</td></tr>
<tr><td>V DMY</td><td>Outputs the dummy VD at no input.
The frequency of the dummy VD output depends on HV FREQ2 setting (when A-SYNC = OFF) or HV-OUT FORMAT (when A-SYNC = ON). No-input detection is based on the V IN result.
0: OFF 1: ON (Dummy VD output at no input)
Note: The VD output does not synchronize with input sync, when A-SYNC = OFF and when a sync is input.</td><td>OFF
(0)</td></tr>
<tr><td>FB2 PIN-M, L</td><td>Changes FB2-OUT pin (pin 22) function.
In FB2 PIN-M/L = ON, the level of pin 22 becomes HIGH when the Read registers below change. The level of pin 22 becomes LOW after the I^2CBUS reading. The pin voltage is used for a sign to detect input signal changes for a microprocessor. For FB2 PIN-M/L = ON, set A-SYNC = 1 (ON) and FB2 MUTE = 1 (MUTE).
<table>
<tr><th>FB2 PIN-M</th><th>FB2 PIN-L</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>OFF (FB2-OUT)</td></tr>
<tr><td>0</td><td>1</td><td>Mode 1 for no-input detection</td></tr>
<tr><td>1</td><td>0</td><td>Mode 2 for format detection</td></tr>
<tr><td>1</td><td>1</td><td>Not available</td></tr>
</table>
Referential Read registers for FB2 PIN-M/L = Mode 1:
FB-DET1, SIG-DET
Referential Read registers for FB2 PIN-M/L = Mode 2:
H-FM2, V-FM2, H-IN, V-IN, HV-OUT FORMAT</td><td>OFF
(00)</td></tr>
</table>

Register Name	Function	Preset Value
HV FREQ2	Input format setting. Set the horizontal and vertical mode according to the format that is input. When A-SYNC = ON mode, this setting is invalid. 00000: 15.625 kHz, 50 Hz (625i) 00001: 15.75 kHz, 60 Hz (525i) 00010: 31.25 kHz, 50 Hz (625p) 00011: 31.5 kHz, 60 Hz (525p, VGA @60 Hz) 00100: 28.125 kHz, 50 Hz (1125/50i) 00101: 33.75 kHz, 60 Hz (1125/60i) 00110: 37.5 kHz, 50 Hz (750/50p) 00111: 45 kHz, 60 Hz (750/60p, XGA @60 Hz) 01000: 31.25 kHz, 50 Hz (1250i) 01001: 37.9 kHz, 60 Hz (SVGA @60 Hz) 01010: 64 kHz, 60 Hz (1125/60p, SXGA @60 Hz) 01011: 75 kHz, 60 Hz (UXGA @60 Hz) 01100: 56.25 kHz, 50 Hz (1125/50p) 01101 to 01111: Not available 10000: 15.734 kHz, 30 Hz (525/30p) 10001: 27 kHz, 24 Hz (1125/24p) 10010: 28.125 kHz, 25 Hz (1125/25p) 10011: 33.75 kHz, 30 Hz (1125/30p) 10100: 27 kHz, 48 Hz (1125/24sf) 10101 to 11111: Not available	15.625 kHz, 50 Hz (00000)
H COUNT MAX	Selects the H-sync count number for the higher threshold for the no-input detection. 0000: 32 counts 1111: 62 counts (2 counts / step)	32 counts (0000)
H COUNT MIN	Selects the H-sync count number for the lower threshold for the no-input detection. 000: 16 counts 111: 30 counts (2 counts / step)	16 counts (000)
SIG DET N	Selects the number of signal detections for the input existence threshold of the no-input detection. 0000: 1 count 0001: 2 counts to 1111: 30 counts (2 counts / step)	1 count (0000)
SIG RESET N	Selects the number of signal detection for input non-existence threshold of the no-input detection. 0000: 1 count 0001: 2 counts to 1111: 30 counts (2 counts / step)	1 count (0000)
SIG RESET	Resets the counter for no-input detection. When 1 is sent, the counter for no-input detection is cleared at that time. 0: Normal 1: Reset	Normal (0)
SIG SW	Selects the input to the counter for no-input detection. 0: SYNC2-IN (pin 15) 1: SYNC1-IN (pin 33)	SYNC2-IN (0)
SIG DET IMPE	Changes the internal impedance for no-input detection. The time constant of LPF for no-input detection is changed by this function and the capacitor value of SYNC FILTER (pin 14). 00: 20 kΩ 01: 15 kΩ 10: 10 kΩ 11: 6 kΩ	20 kΩ (00)
SIG DET LVL	Changes the threshold for no-input detection. 00: 0.55 V 01: 0.80 V 10: 1.05 V 11: 1.30 V	0.55 V (00)
TEST1,2,3	Test modes for shipping test. Set all zero.	all 0

Read Mode

Register Name	Function
POR	Power On Reset 0: Normal 1: Register preset After power on, 1 is returned at first read. 0 is returned at second and subsequent reads.
H FM2	Horizontal format detection 2 0: Known 1: Unknown Detects whether an input is in one of the defined formats or not. This is based on H FORMAT data.
V FM2	Vertical format detection 2 0: Known 1: Unknown Detects whether an input is in one of the defined formats or not. This is based on V FORMAT data.
H IN	Input detection to horizontal syncs 0: No input 1: Signal detected
V IN	Input detection to vertical syncs 0: No input 1: Signal detected
V-SYNC-W	V-SYNC width detection 0: Wide 1: Narrow Detects V-SYNC width for detecting 1250i format. Under A-SYNC = 1 (ON), V-SYNC-W shows 1 when VD width from VD-IN pin is narrower than approx 69 µs, or when V-SYNC width from SYNC-IN pin is narrower than approx 54 µs.
HD-POL	Polarity detection to HD-IN 0: Positive 1: Negative Detects the width from the HD-IN pin to determine whether it is negative or not. When the High level of the input is wider than approx 13.5 us, HD-POL shows 1.
VD-POL	Polarity detection to VD-IN 0: Positive 1: Negative Detects the width from the VD-IN pin to determine whether it is negative or not. When the High level of the input is wider than approx 4.5 ms, VD-POL shows 1.
H FORMAT	Horizontal format detection 0000: 15.625/15.75 kHz 0001: 28.125 kHz 0010: 31.25/31.5 kHz 0011: 33.75 kHz 0100: 37.5/37.9 kHz 0101: 45/48 kHz 0110: 56.25 kHz 0111: 64/67.5 kHz 1000: 75 kHz 1001 to 1111: Undefined Detects a horizontal format (horizontal frequency).
V FORMAT	Vertical format detection 000: 50 Hz 001: 60 Hz 010: 48 Hz 011: 30 Hz 100: 25 Hz 101: 24 Hz 110 to 111: Undefined Detects a vertical format (horizontal frequency) according to V FREQ DET data.
FB DET1(2)	Voltage detection of FB pin for SCART connector 0: Not always high 1: Always high Detects the voltage of FB-IN pin, selected by FB1(2) OUT (to pin 9 (22)) to determine whether the voltage is always high or not.
SIG DET	No-input detection. 0: No input 1: A signal detected The signal to the no-input detection circuit is selected by SIG SW. Refer to the relevant functions for H COUNT MAX, H COUNT MIN, SIG DET N, SIG RESET N, SIG RESET, SIG DET IMPE and SIG DET LVL.

Register Name	Function
HV-OUT FORMAT	Format detection result. H and V dummy output frequencies depend on this result. 00000: 15.625 kHz, 50 Hz (625i) 00001: 15.75 kHz, 60 Hz (525i) 00010: 31.25 kHz, 50 Hz (625p) 00011: 31.5 kHz, 60 Hz (525p, VGA @60 Hz) 00100: 28.125 kHz, 50 Hz (1125/50i) 00101: 33.75 kHz, 60 Hz (1125/60i) 00110: 37.5 kHz, 50 Hz (750/50p) 00111: 45 kHz, 60 Hz (750/60p, XGA @60 Hz) 01000: 31.25 kHz, 50 Hz (1250i) 01001: 37.9 kHz, 60 Hz (SVGA @60 Hz) 01010: 64 kHz, 60 Hz (1125/60p, SXGA @60 Hz) 01011: 75 kHz, 60 Hz (UXGA @60 Hz) 01100: 56.25 kHz, 50 Hz (1125/50p) 01101 to 01111: Not available 10000: 15.734 kHz, 30 Hz (525/30p) 10001: 27 kHz, 24 Hz (1125/24p) 10010: 28.125 kHz, 25 Hz (1125/25p) 10011: 33.75 kHz, 30 Hz (1125/30p) 10100: 27 kHz, 48 Hz (1125/24sf) 10101 to 11111: Not available
DC1 to 12	DC voltage detection for D-pin or S-pin 00: Low (0 V) 01: Mid (2.2 V) 10: Undefined 11: High (5 V) Remark 1: See below for the relationship between this function number and the pin number. DC1 - pin 39, DC2 - pin 40, DC3 - pin 44, DC4 - pin 46, DC5 - pin 48, DC6 - pin 50, DC7 - pin 60, DC8 - pin 64, DC9 - pin 66, DC10 - pin 68, DC11 - pin 70, DC12 - pin 80 Remark 2; D-pin SW LINE: 00: Connected 01: ---- 10: ---- 11: Not connected LINE1: 00: 525 (480) 01: 750 (720) 10: ---- 11: 1125 (1080) LINE2: 00: Interlace 01: ---- 10: ---- 11: Progressive LINE3: 00: 4:3 01: 4:3 letter box 10: ---- 11: 16:9 Remark 3; about S-pin 00: 4:3 01: 4:3 letter box 10: ---- 11: 16:9
S1 to 8	Detects whether S-pin is connected or not. 0: Low (not connected) 1: Open (connected) Remark 1: An external circuit is necessary to use this function. Refer to the Function description. Remark 2: See below for the relationship between this function number and the pin number. S1 - pin 45, S2 - pin 47, S3 - pin 53, S4 - pin 59, S5 - pin 65, S6 - pin 67, S7 - pin 73, S8 - pin 79
V FREQ DET	Counts the vertical frequency of an input selected by SYNC SW. When V-DET = 0: 00000000: over 3.5 kHz 01001111: 44 Hz or less 01010000 to 11111111: No input When V-DET = 1: 00000000: over 3.5 kHz 10011001: 23 Hz or less 10011010 to 11111111: No input How to calculate a vertical frequency (Y): Convert data read from V FREQ DET into a decimal value and call it X. $\underline{\text{Vertical frequency (Y)} = 1 \div (X \times 2.8607 \times 10^{-4})\ \text{[Hz]}}$ The error range of X is –1 to +1.
H FREQ DET	Counts the horizontal frequency of an input selected by SYNC SW. When for SYNC-IN; 00000001: No input 11111111: over 85 kHz When for HD/VD-IN; 00000000: No input 11111111: over 85 kHz How to calculate a horizontal frequency (Y): Convert data read from H FREQ DET into a decimal value and call it X. $\underline{\text{Horizontal frequency (Y)} = 1 \div (0.003 \div X)\ \text{[Hz]}}$ The error range of X is –1 to +1.

Note 1: In determining the decision algorithms (detection range, detection times, and so on) for H/V frequency detection, it is necessary to take into account both previously mentioned cautions and other factors such as signal conditions and I^2CBUS data transmission in the course of prototype TV set evaluation.

Note 2: The READ BUS flags indicate that a certain signal is detected at a given moment. However, the detection result will not be very reliable if only one flag is checked. To obtain accuracy, it is recommended that a judgment should be made on the basis of confirming several times and verifying agreement among the majority of flags read in a sequence and/or at the same time.

Function Descriptions

Output selections

Outputs are switched by I2CBUS registers, as in the following tables.

YCbCr1 OUT

Register Settings					Outputs			Available Input		
CbCr1 OUT	CbCr PIN4	CbCr PIN3	bCr PIN2	CbCr PIN1	Y1/G1 OUT (Pin 6)	Cb1/B1 OUT (Pin 8)	Cr1/R1 OUT (Pin 10)	CVBS	YC	YCbCr RGB
0000	*	*	*	*	Mute	Mute	Mute			
0001	*	*	*	*	SY1 (pin 57)	SC1 (pin 59)	Mute	y	y	
0010	*	*	*	*	SY2 (pin 77)	SC2 (pin 79)	Mute	y	y	
0011	*	*	*	*	CVBS3 (pin 36)	Mute	Mute	y		
0100	*	*	*	*	CVBS4 (pin 38)	Mute	Mute	y		
0101	*	*	*	0	CVBS5 (pin 41)	Mute	Mute	y		
	*	*	*	1	CVBS5 (pin 41)	Cr1 (pin 45)	Mute	y	y	
0110	*	*	0	*	CVBS6 (pin 61)	Mute	Mute	y		
	*	*	1	*	CVBS6 (pin 61)	Cr2 (pin 65)	Mute	y	y	
0111	*	*	*	0	Y1 (pin 49)	Cb1 (pin 47)	Cr1 (pin 45)	y	y	y
	*	*	*	1	Y1 (pin 49)	Cb1 (pin 47)	Mute	y	y	
1000	*	*	0	*	Y2 (pin 69)	Cb2 (pin 67)	Cr2 (pin 65)	y	y	y
	*	*	1	*	Y2 (pin 69)	Cb2 (pin 67)	Mute	y	y	
1001	*	0	*	*	Y3 (pin 55)	Cb3 (pin 53)	Cr3 (pin 51)	y	y	y
	*	1	*	*	Y3 (pin 55)	Cb3 (pin 53)	Mute	y	y	
1010	0	*	*	*	Y4 (pin 75)	Cb4 (pin 73)	Cr4 (pin 71)	y	y	y
	1	*	*	*	Y4 (pin 75)	Cb4 (pin 73)	Mute	y	y	
1011	*	*	*	*	Cr3 (pin 51)	Mute	Mute	y		
1100	*	*	*	*	Cr4 (pin 71)	Mute	Mute	y		
1101 to 1111	*	*	*	*	Not available					

*: Don't care

YCbCr2 OUT

Register Settings					Outputs			Available Input		
CbCr1 OUT	bCr PIN4	CbCr PIN3	bCr PIN2	CbCr PIN1	Y2/G2 OUT (Pin 19)	Cb2/B2 OUT (Pin 21)	Cr2/R2 OUT (Pin 23)	CVBS	YC	YCbCr RGB
0000	*	*	*	*	Mute	Mute	Mute			
0001	*	*	*	*	SY1 (pin 57)	SC1 (pin 59)	Mute	y	y	
0010	*	*	*	*	SY2 (pin 77)	SC2 (pin 79)	Mute	y	y	
0011	*	*	*	*	CVBS3 (pin 36)	Mute	Mute	y		
0100	*	*	*	*	CVBS4 (pin 38)	Mute	Mute	y		
0101	*	*	*	0	CVBS5 (pin 41)	Mute	Mute	y		
	*	*	*	1	CVBS5 (pin 41)	Cr1 (pin 45)	Mute	y	y	
0110	*	*	0	*	CVBS6 (pin 61)	Mute	Mute	y		
	*	*	1	*	CVBS6 (pin 61)	Cr2 (pin 65)	Mute	y	y	
0111	*	*	*	0	Y1 (pin 49)	Cb1 (pin 47)	Cr1 (pin 45)	y	y	y
	*	*	*	1	Y1 (pin 49)	Cb1 (pin 47)	Mute	y	y	
1000	*	*	0	*	Y2 (pin 69)	Cb2 (pin 67)	Cr2 (pin 65)	y	y	y
	*	*	1	*	Y2 (pin 69)	Cb2 (pin 67)	Mute	y	y	
1001	*	0	*	*	Y3 (pin 55)	Cb3 (pin 53)	Cr3 (pin 51)	y	y	y
	*	1	*	*	Y3 (pin 55)	Cb3 (pin 53)	Mute	y	y	
1010	0	*	*	*	Y4 (pin 75)	Cb4 (pin 73)	Cr4 (pin 71)	y	y	y
	1	*	*	*	Y4 (pin 75)	Cb4 (pin 73)	Mute	y	y	
1011	*	*	*	*	Cr3 (pin 51)	Mute	Mute	y		
1100	*	*	*	*	Cr4 (pin 71)	Mute	Mute	y		
1101 to 1111	*	*	*	*	Not available					

*: Don't care

MONITOR OUT

Register Settings						Outputs	Available Input	
MON OUT	YC MIX	CbCr PIN4	CbCr PIN3	CbCr PIN2	CbCr PIN1	MONITOR OUT (Pin 2)	CVBS	YC
0000	*	*	*	*	*	Mute		
0001	0	*	*	*	*	SY1 (pin 57)	y	
	1					SY1 (pin 57) + SC1 (pin 59)		y
0010	0	*	*	*	*	SY2 (pin 77)	y	
	1					SY2 (pin 77) + SC2 (pin 79)		y
0011	*	*	*	*	*	CVBS3 (pin 36)	y	
0100	*	*	*	*	*	CVBS4 (pin 38)	y	
0101	*	*	*	*	0	CVBS5 (pin 41)	y	
	0	*	*	*	1	CVBS5 (pin 41)	y	
	1					CVBS5 (pin 41) + Cr1 (pin 45)		y
0110	*	*	*	0	*	CVBS6 (pin 61)	y	
	0	*	*	1	*	CVBS6 (pin 61)	y	
	1					CVBS6 (pin 61) + Cr2 (pin 65)		y
0111	0	*	*	*	*	Y1 (pin 49)	y	
	1					Y1 (pin 49) + Cb1 (pin 47)		y
1000	0	*	*	*	*	Y2 (pin 69)	y	
	1					Y2 (pin 69) + Cb2 (pin 67)		y
1001	0	*	*	*	*	Y3 (pin 55)	y	
	1					Y3 (pin 55) + Cb3 (pin 53)		y
1010	0	*	*	*	*	Y4 (pin 75)	y	
	1					Y4 (pin 75) + Cb4 (pin 73)		y
1011	*	*	*	*	*	Cr3 (pin 51)	y	
1100	*	*	*	*	*	Cr4 (pin 71)	y	
1101 to 1111	*	*	*	*	*	Not available		

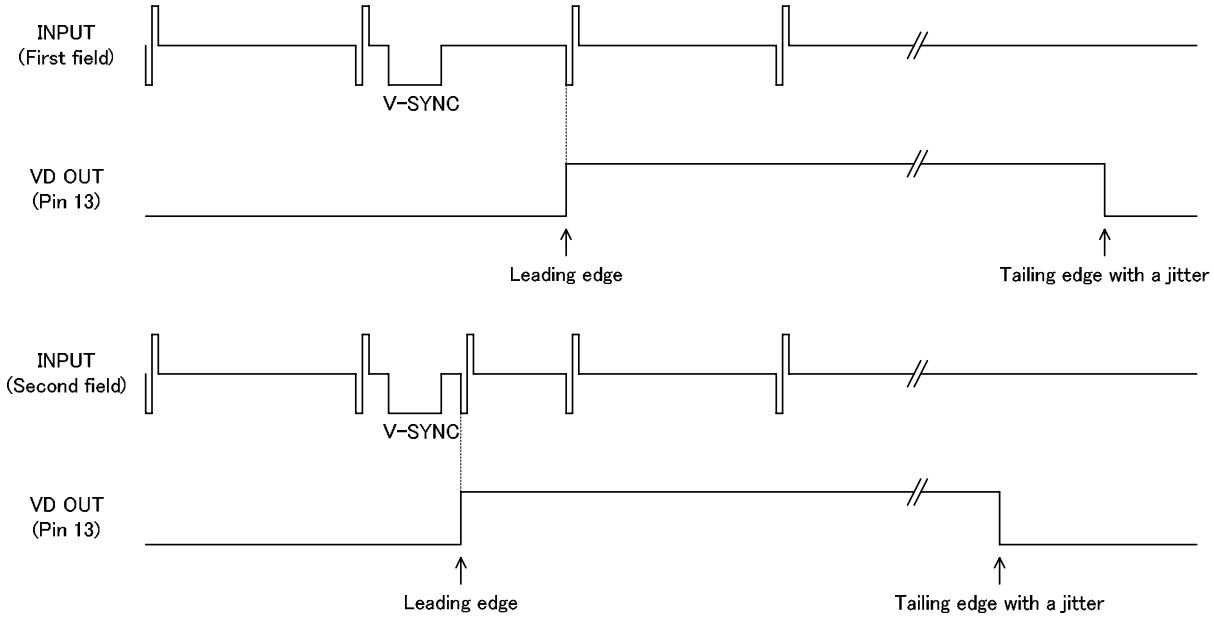
*: Don't care

Vertical sync separation for 1250i/50

When HV FREQ2 = 01000, the vertical sync separation for the 1250i/50 is accomplished through the use of a special circuit. The phase of the VD-out (pin 13) depends on the H-SYNC timing shown in the figure below. There is no VD-out when there is no H-SYNC input.

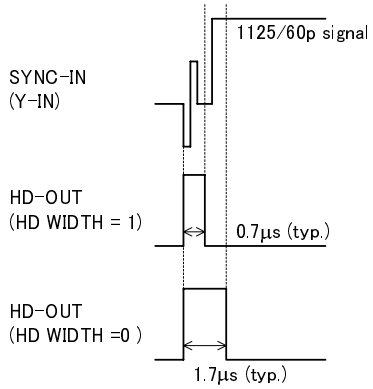
In the manual sync processing mode (A-SYNC = OFF), use READ BUS functions, V-SYNC-W and H, V FORMAT (or H, V FREQ DET) to detect the 1250i/50.

Note: The tailing edge of the VD-OUT has a jitter. Use the leading edge only.



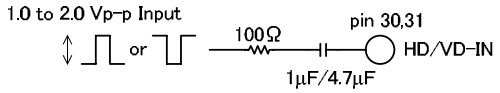
HD width

HD-OUT width is selectable by HD WIDTH as below. A setting in which HD WIDTH = 1 (NARROW) is recommended for the 1125/50p/60p format owing to crosstalk from HD-OUT to video signals causing spike noise on video signals.

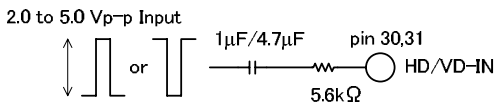


HD/VD input amplitude

When a 5.6 kΩ is added before the input pin like the following figure, 5.0 Vp-p pulse input is allowed. However, the acceptable minimum amplitude then becomes 2.0 Vp-p.



Normal application



For large-input application

Automatic sync processing mode (A-SYNC)

Counted horizontal and vertical frequency data to input signal are returned to READ BUS functions, H, V FREQ DET. Also, the detected format is returned to H, V FORMAT and H, V FM2 when the H/V frequencies are in internal defined ranges. Input detection results for H, V-SYNC or HD,VD, which indicate whether or not input exists, are returned to H,V IN. HV-OUT FORMAT indicates the active mode.

In automatic sync processing mode (when A-SYNC = ON), this device operates as indicated in the following table according to these READ data. Then, the SYNC1-IN pin is not used for format detection.

Input Condition	HV-OUT FORMAT, H, V FORMAT Status	H, V FM2 Status	H, V IN Status	HD, VD Outputs
Standard format	The format as input	Known	Signal	The separated sync as input
Nonstandard format	The status indicates not the current condition but the last detected format.	Unknown	Signal	The separated sync as input
No input	The status indicates not the current condition but the last detected format.	Known: The status indicates not the current condition but the last detected format.	No input	Dummy HD and VD, of which the frequency depends on the HV-OUT FORMAT status

Note 3: Dummy HD and VD may become unstable while the mode is changing from one format to another.

Manual sync processing mode (A-SYNC = OFF)

In this mode, the SYNC1-IN pin is used only for detecting the input format and the SYNC2-IN pin is used only for separating H and V syncs for HD and VD outputs. It is possible to detect some input formats by means of time-sharing while separating syncs to another input.

The following is an example of how to detect H/V frequency when A-SYNC = OFF.

1. Input the signal from Yvi-OUT pin into the SYNC1-IN pin.
2. Read data such as H, V FREQ DET and H, V FORMAT.
3. Detect the H/V frequency by microprocessor or similar means, depending on the data obtained.
4. Input the detected signal into the SYNC2-IN pin and set HV FREQ2 and so on for the SYNC2-IN pin to the detected mode.
5. Continue to monitor the obtained data for the SYNC1-IN pin, such as H, V FREQ DET and H, V FORMAT. When any alterations are recognized, re-set HV FREQ2 and so on for the SYNC2-IN pin.

Decision algorithms (for detection range, detection times and so on) for H/V frequency detection should be determined taking into account the above-mentioned errors in measuring H/V frequencies and other factors such as signal conditions and I^2CBUS data transmission in the course of prototype TV set evaluation.

By the way, in A-SYNC = OFF and H, V DMY = ON mode, dummy HD and VD are output according to the HV FREQ2 setting when there is no input.

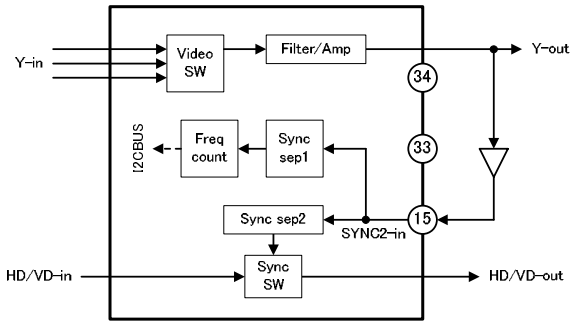


Fig. Signal route when A-SYNC = ON

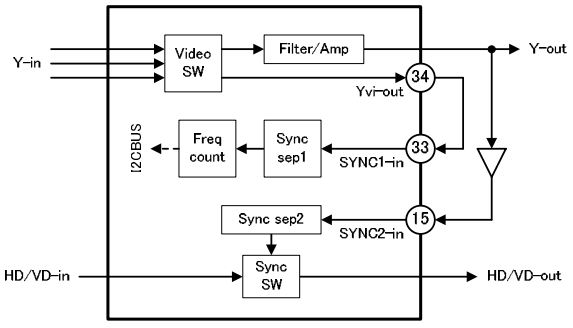


Fig. Signal route when A-SYNC = OFF

Sync separation level

The sync separation level is changed according to the ratio of H-sync width to one line. Typical sync separation levels for each format are as follows.

HV-SEP data	00	01	10	11
625/50i	18	26	31	43
525/60i	18	26	31	43
625/50p	19	27	32	44
525/60p	19	27	32	44
1125/50i	27	34	40	52
1125/60i	25	33	38	50
750/50p	25	32	38	50
750/60p	24	31	36	49
1250/50i	22	30	36	48
1125/50p	28	36	41	52
1125/60p	27	34	39	52
525/30p	18	26	31	43
1125/24p	27	34	40	52
1125/25p	27	34	40	52
1125/30p	26	32	38	50
1125/24sf	28	34	40	52
VGA/60	20	26	32	43
SVGA/60	20	27	33	44
XGA/60	20	27	33	44
SXGA/60	22	29	34	45

Expressed as percentages, where 286 mVp-p sync applies to 525/60i and 300 mVp-p sync applies otherwise

The format detection and sync separation performances are changed due to the separation level set by HV-SEP setting and the connected coupling capacitor value. The careful evaluations are required to set the separation level under consideration of expected input conditions such as a suppressed sync input, an input with V-sag, and APL (Average Picture Level) fluctuations.

For “Sync on G” signal, HD-OUT is not output during the V-sync period because there is no H-sync during the V-sync period.

No-input detection

This function detects whether there is input or not. It is useful for detecting no-input of 525i or 625i even if which is a weakened signal strength.

(1)0 (no-input) → 1 (detected)

When Nmin ≦ N1 ≦ Nmax, and when N2 ≧ Ndet, SIG DET returns 1.

Where, Nmin: the number set by H COUNT MIN

Nmax: the number set by H COUNT MAX

Ndet: the number set by SIG DET N

N1: the number of the H-sync count in the counter during an internal window (approx. 2 ms)

N2: the number of conditions that "Nmin ≦ N1 ≦ Nmax" is detected

(2) 1 (detected) → 0 (no-input)

When N1 ≦ Nmin, N1 ≧ Nmax, and when N3 ≧ Nreset, SIG DET returns 0.

Where, Nreset: the number set by SIG RESET N

N3: the number of conditions that "N1 ≦ Nmin and N1 ≧ Nmax" is detected

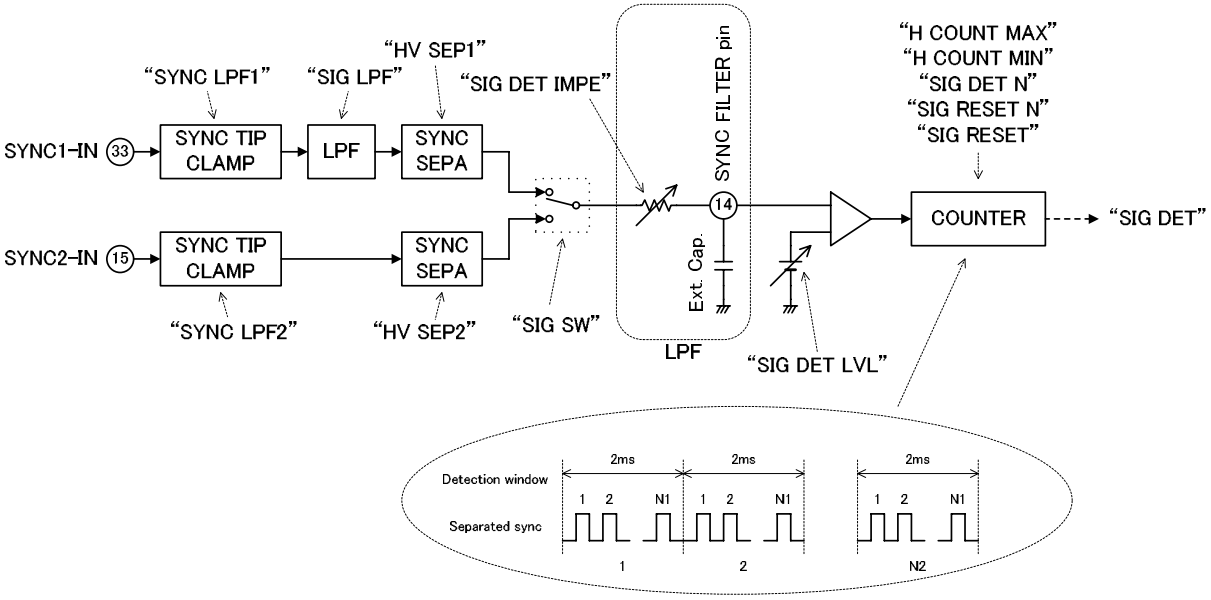


Fig. Block diagram for no-input detection

Decide how to use no-input detection after making a thorough evaluation using a prototype TV set.

S-pin insertion detection

C-IN pins detect the DC level to determine whether the S-pin is inserted or not.

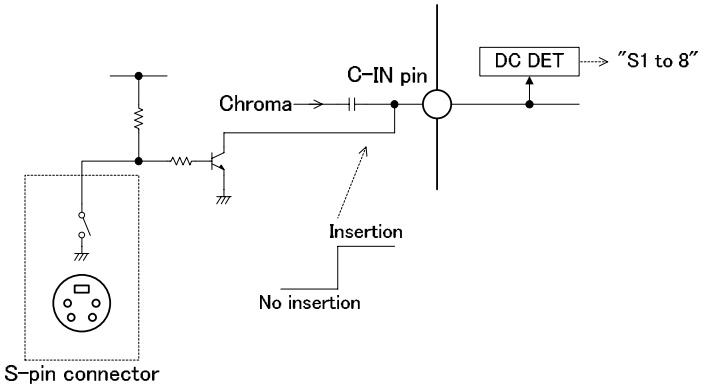
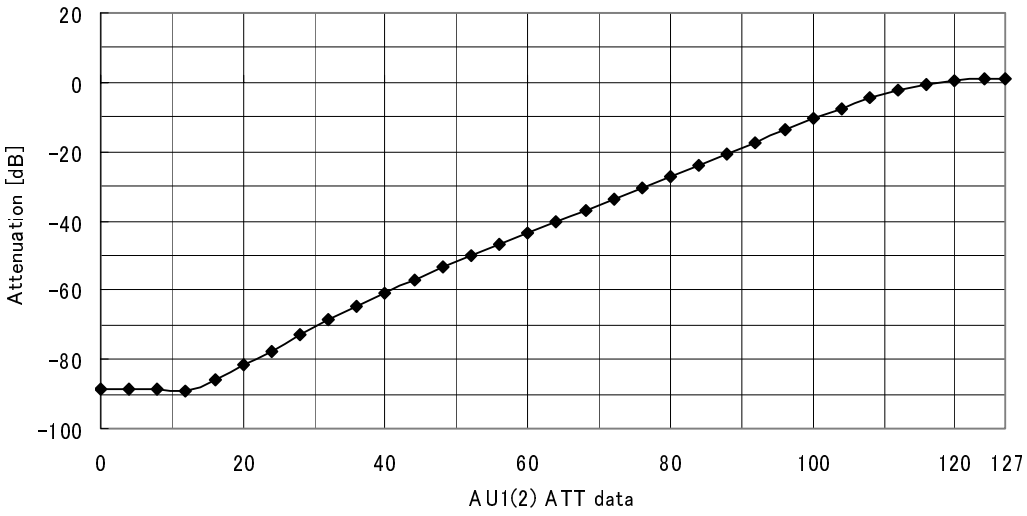


Fig. Application of S-pin insertion detection

Audio gain

Audio gain is controlled by AU1(2) ATT. The following figure shows the typical characteristic, where the series-connected resistor is 5.6 kΩ.



Typical characteristics

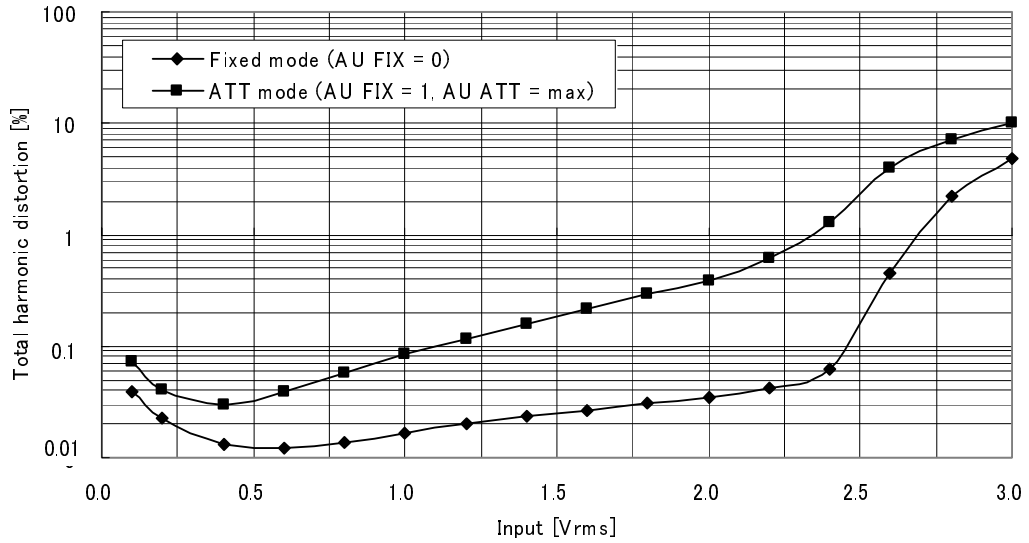


Fig. Audio total harmonic distortion (input resistance: 5.6 kΩ)

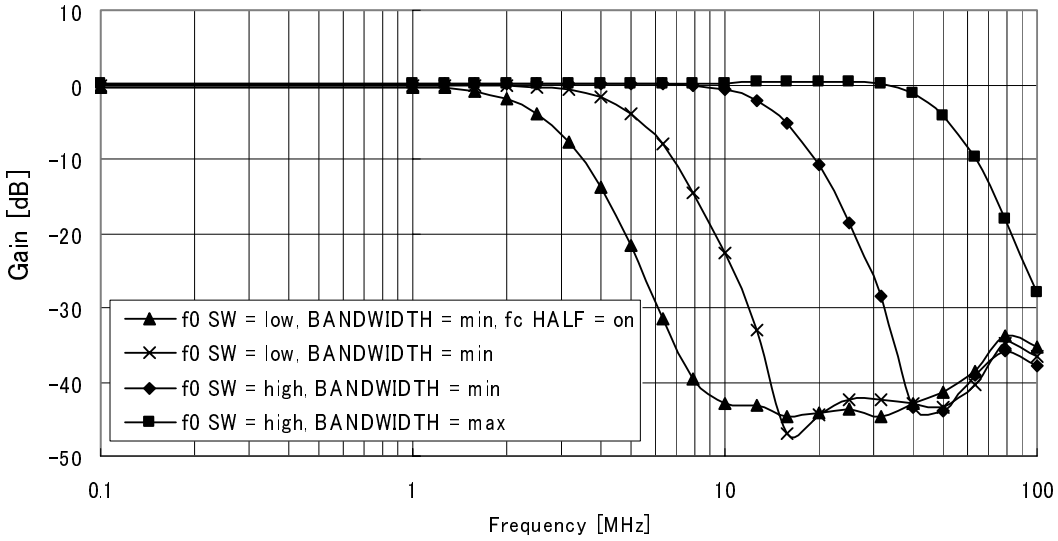


Fig. Typical prefilter frequency characteristics

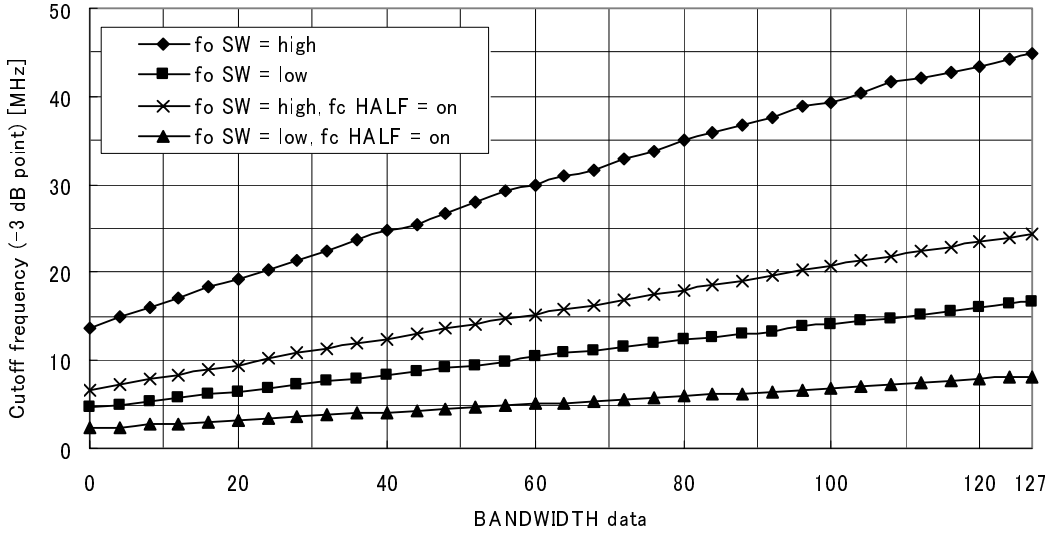


Fig. Typical cutoff frequency (-3 dB point) characteristics of prefilter

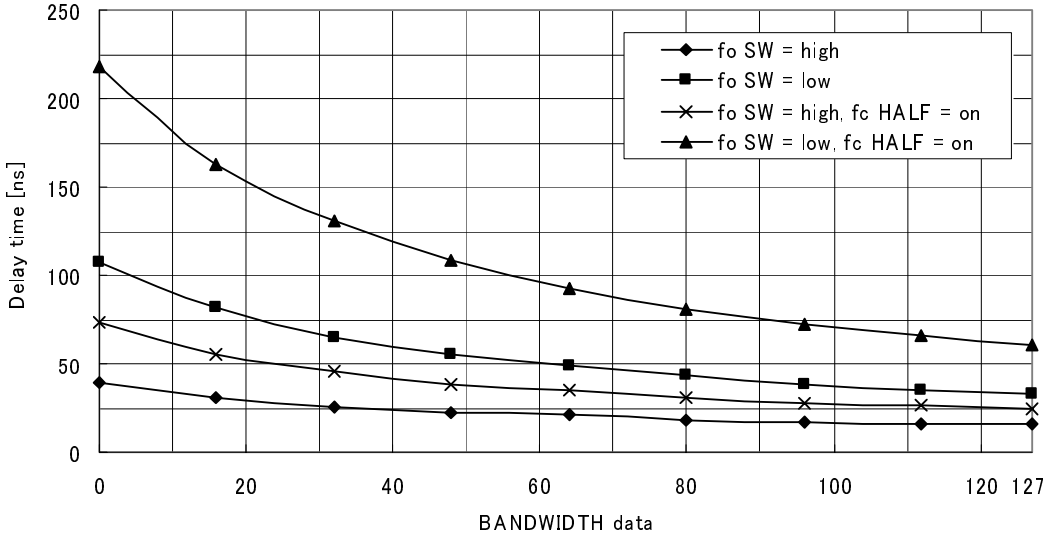


Fig. Typical delay-time (group delay @ 1 MHz) characteristics of prefilter

Recommended crystal oscillator

When a connected crystal oscillator is used for the XO, the following oscillation specifications are required.

Oscillation frequency (fundamental): 3.579545 MHz (for NTSC decoding)

Frequency tolerance: +/- 50 ppm

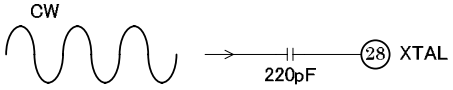
External CW input into crystal oscillator pin

Instead of connecting a crystal oscillator, it is possible to input an external CW (Continual Wave) into pin 28 through a capacitor as below.

The required specs on the CW are as follows.

Input frequency (fundamental): 3.579545 MHz +/- 50 ppm

Input amplitude: 1.0Vp-p +/- 0.5Vp-p



How to deal with unused pins

Unused pins should be dealt with as below. Pins not mentioned below should be connected properly.

Pin No.	Pin Name	Procedure	Pin No.	Pin Name	Procedure
1	AL3 OUT	Procedure 3	46	AR9 IN/DC4	Procedure 1
2	MONITOR OUT	Procedure 3	47	Cb1/B1 IN	Procedure 1
3	AR3 OUT	Procedure 3	48	AL9 IN/DC5	Procedure 1
4	CVBS1 OUT	Procedure 3	49	Y1/G1 IN	Procedure 1
5	AL1 OUT	Procedure 3	50	FB3 IN/DC6	Procedure 2
6	Y1/G1 OUT	Procedure 3	51	Cr3/R3 IN	Procedure 1
7	AR1 OUT	Procedure 3	52	AR3 IN	Procedure 1
8	Cb1/B1 OUT	Procedure 3	53	Cb3/B3-IN	Procedure 1
9	FB1 OUT	Procedure 3	54	AL3 IN	Procedure 1
10	Cr1/R1 OUT	Procedure 3	55	Y3/G3 IN	Procedure 1
12	HD OUT	Procedure 3	56	AR4 IN	Procedure 1
13	VD OUT	Procedure 3	57	SY1 IN	Procedure 1
14	SYNC FILTER	Procedure 3	58	AL4 IN	Procedure 1
15	SYNC2 IN	Procedure 1	59	SC1 IN	Procedure 1
17	CVBS2 OUT	Procedure 3	60	DC7	Procedure 2
18	AL2 OUT	Procedure 3	61	CVBS6 IN	Procedure 1
19	Y2/G2 OUT	Procedure 3	62	AR5 IN	Procedure 1
20	AR2 OUT	Procedure 3	63	AL5 IN	Procedure 1
21	Cb2/B2 OUT	Procedure 3	64	FB2 IN/DC8	Procedure 2
22	FB2 OUT	Procedure 3	65	Cr2/R2 IN	Procedure 1
23	Cr2/R2 OUT	Procedure 3	66	AR10 IN/DC9	Procedure 1
30	VD IN	Procedure 4	67	Cb2/B2 IN	Procedure 1
31	HD IN	Procedure 4	68	AL10 IN/DC10	Procedure 1
33	SYNC1 IN	Procedure 1	69	Y2/G2 IN	Procedure 1
34	Yvi OUT	Procedure 3	70	FB4 IN/DC11	Procedure 2
35	AR1 IN	Procedure 1	71	Cr4/R4 IN	Procedure 1
36	CVBS3 IN	Procedure 1	72	AR6 IN	Procedure 1
37	AL1 IN	Procedure 1	73	Cb4/B4-IN	Procedure 1
38	CVBS4 IN	Procedure 1	74	AL6 IN	Procedure 1
39	AR8 IN/DC1	Procedure 1	75	Y4/G4 IN	Procedure 1
40	AL8 IN/DC2	Procedure 1	76	AR7 IN	Procedure 1
41	CVBS5 IN	Procedure 1	77	SY2 IN	Procedure 1
42	AR2 IN	Procedure 1	78	AL7 IN	Procedure 1
43	AL2 IN	Procedure 1	79	SC2 IN	Procedure 1
44	FB1 IN/DC3	Procedure 2	80	DC12	Procedure 2
45	Cr1/R1 IN	Procedure 1	—	—	—

Procedure 1: Connect a 0.01 μF capacitor between this pin and GND.
Procedure 2: Connect to GND.
Procedure 3: Leave open.
Procedure 4: Connect a 10 kΩ resistor between this pin and GND.

How to start the I^2CBUS

After power on, send bus data as follows. Use software to handle the procedure.

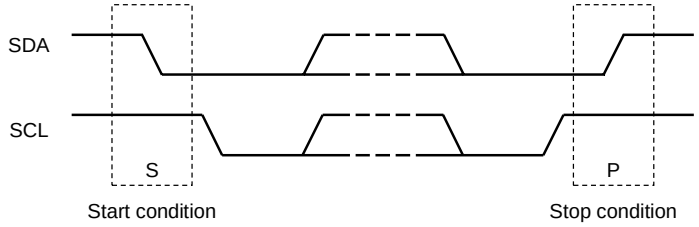
1. Turn on the power.
2. Transmit all the write data.

How to transmit/receive via the I^2CBUS

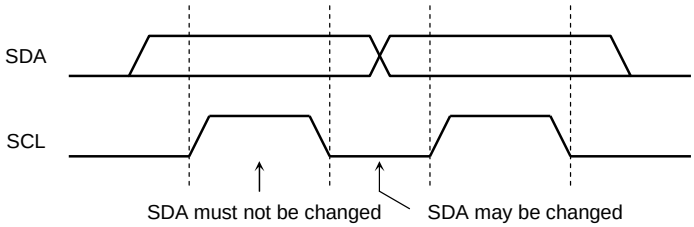
Slave Address: DE_H / DF_H

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	1	0/1

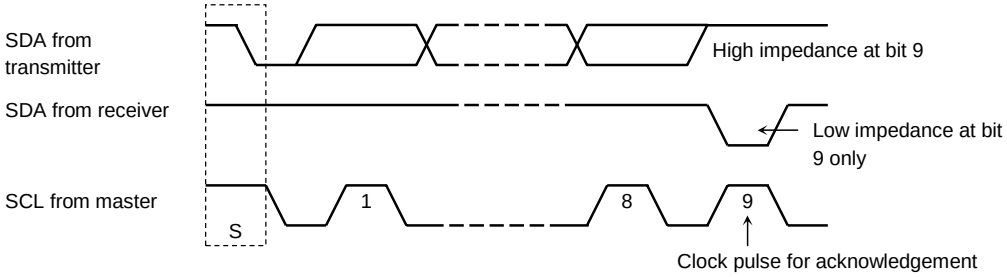
Start and Stop Conditions



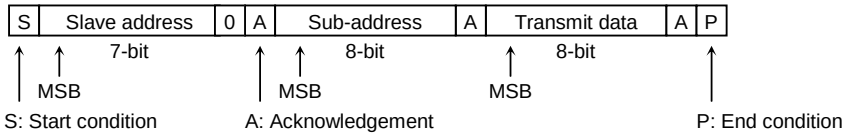
Bit Transmission



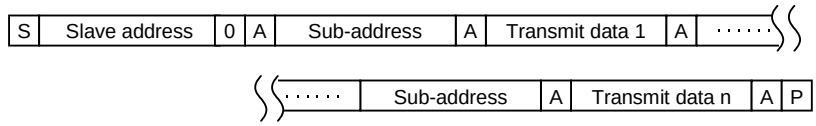
Acknowledgement



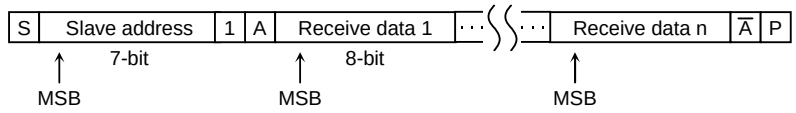
Data Transmit Format 1



Data Transmit Format 2



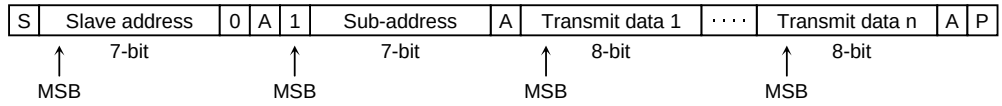
Data Receive Format



To receive data, the master transmitter changes to a receiver immediately after the first acknowledgement. The slave receiver changes to a transmitter.

The end condition is always created by the master.

Optional Data Transmit Format (Automatic Increment Mode)



In this way, sub-addresses are automatically incremented from the specified sub-address and data are set.

I^2CBUS Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Low level input voltage	V_{IL}	0	–	1.1	V
High level input voltage	V_{IH}	2.4	–	V/S-Vcc	V
Hysteresis of Schmitt trigger inputs	V_{hys}	–	0.7	–	V
Low level output voltage at 3 mA sink current	V_{OL1}	0	–	0.4	V
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDD	I_i	-10	–	10	µA
Capacitance for each I/O pin	C_i	–	–	10	pF
SCL clock frequency	f_{SCL}	0	–	400	kHz
Hold time START condition	$t_{HD;STA}$	0.6	–	–	µs
Low period of SCL clock	t_{LOW}	1.3	–	–	µs
High period of SCL clock	t_{HIGH}	0.6	–	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	–	µs
Data hold time	$t_{HD;DAT}$	0	–	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	–	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	–	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	–	µs

Note: This parameter is not tested during production and is provided only as information to assist the design of applications.

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Supply voltage	9 V Vcc	V_{CCmax9}	12.0	V
	5 V Vcc	V_{CCmax5}	6.0	
	3.3 V Vcc	V_{CCmax3}	6.0	
Input pin voltage		V_{in}	GND – 0.3 to Vcc + 0.3	V
Y or Sync input amplitude (pin 15, 33, 36, 38, 41, 49, 51, 55, 57, 61, 69, 71, 75, 77)		Y_{in}	2.0	Vp-p
Power dissipation		P_D(Note 4)	2451	mW
Power dissipation reduction rate		1/θja	19.6	mW/°C
Operating temperature		T_{opr}	–20 to 75	°C
Storage temperature		T_{stg}	–55 to 150	°C

Note 4: Refer to the figure below. Note, however, that the condition applies only where the device is mounted on a board 114.3 x 76.2 x t:1.6 mm, Cu 20%. Mount the devive on a board which is larger than it.

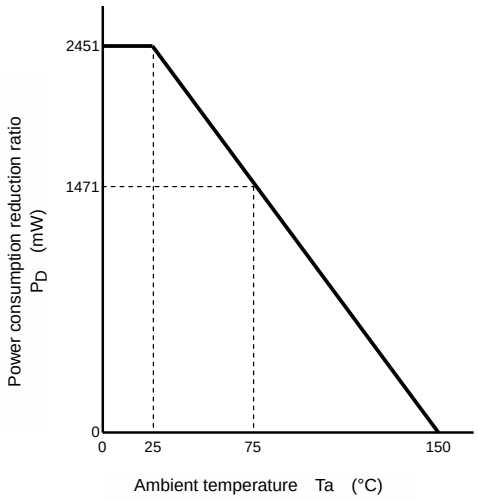


Figure P_D - Ta Curve

Note 5: Install the product correctly. Otherwise, it may result in break down, damage and/or degration to the product or equipment.

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.

Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

Operating conditions

Characteristic		Description		Min	Typ.	Max	Unit
Supply voltage (V_{CC})		Pin 24		8.5	9.0	9.5	V
		Pin 11		4.7	5.0	5.3	
		Pin 29; Supply power from V/S Vcc (pin 11) via a resistor.		3.1	3.3	3.5	
Y/G signal input amplitude		Pins 49, 55, 69, 75; with sync		—	1.0	—	V_{p-p}
CVBS/SY input amplitude		Pins 36, 38, 41, 49, 55, 57, 61, 69, 75, 77 (51, 71); with sync		—	1.0	—	V_{p-p}
Y/G signal input frequency		Pins 49, 55, 69, 75		0	—	60	MHz
CVBS/SY input frequency		Pins 36, 38, 41, 49, 55, 57, 61, 69, 75, 77 (51, 71)		0	—	8	MHz
SC (Chroma) signal input amplitude		Pin 59, 79 (45, 47, 53, 65, 67, 73)		—	—	2	V_{p-p}
Cb, Cr, Pb, Pr signal input amplitude		Pins 45, 47, 51, 53, 65, 67, 71, 73; 100% color bar signal		—	0.7	—	V_{p-p}
Cb, Cr, Pb, Pr signal input frequency		Pins 45, 47, 51, 53, 65, 67, 71, 73		0	—	60	MHz
R, G, B signal input amplitude		Pins 45, 47, 49, 51, 53, 55, 65, 67, 69, 71, 73, 75; 100% white signal without sync		—	0.7	—	V_{p-p}
R, G, B signal input frequency		Pins 45, 47, 49, 51, 53, 55, 65, 67, 69, 71, 73, 75		0	—	60	MHz
HD, VD signal input amplitude		Pins 30, 31		1.0	—	2.0	V_{p-p}
HD input frequency		Pins 31 for freq counter		0	—	85	kHz
VD input frequency		Pins 30 for freq counter		23	—	3500	Hz
FB input level		Pins 44, 50, 64, 70	H	1.0	—	3.0	V
			L	GND	—	0.4	
FB input width		Pins 44, 50, 64, 70		80	—	—	ns
DC detection input voltage	DC1 to 12	Pins 39, 40, 44, 46, 48, 50, 60, 64, 66, 68, 70, 80	H	3.5	—	V/S Vcc	V
			M	1.4	2.2	2.4	
			L	GND	—	0.6	
	S1 to 8	Pins 45, 47, 53, 59, 65, 67, 73, 79	L	GND	—	0.6	V
SDA input current		Pins 25		—	—	3	mA

Remark: Supply power to all Vcc pins (pin 11, 24, 29).

Electrical Characteristics

(Unless otherwise specified, AU V_{CC} = 9 V, V/S V_{CC} = 5 V, V_{dd} = 3.3 V, Ta = 25°C, I^2CBUS data: preset values)

Current Consumption (AU8/9/10 PIN = 1, f0 SW1/2 = 1, BANDWIDTH1/2 = max)

Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
AU V_{CC} (pin 24)	I_{CCAU}	—	7.5	9.5	12.5	mA
V/S V_{CC} (pin 11)	I_{CCVS}	—	100	125	165	
V_{dd} (pin 29)	I_{CCD}	Resistance to 5 V; R = 180 Ω	6.3	9.4	12.8	

Pin Voltage (test condition: no signal input)

Pin No.	Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
1	AL3 OUT	V_1	–	3.8	4.1	4.4	V
2	MONITOR OUT	V_2	–	0.9	1.2	1.5	
3	AR3 OUT	V_3	–	3.8	4.1	4.4	
4	CVBS1 OUT	V_4	–	1.0	1.3	1.6	
5	AL1 OUT	V_5	–	3.8	4.1	4.4	
6	Y1/G1 OUT	V_6	–	1.0	1.3	1.6	
7	AR1 OUT	V_7	–	3.8	4.1	4.4	
8	Cb1/B1 OUT	V_8	–	1.0	1.3	1.6	
10	Cr1/R1 OUT	V_{10}	–	1.0	1.3	1.6	
14	SYNC FILTER	V_{14}	–	3.0	3.3	3.6	
15	SYNC2 IN	V_{15}	–	1.5	1.8	2.1	
17	CVBS2 OUT	V_{17}	–	1.0	1.3	1.6	
18	AL2 OUT	V_{18}	–	3.8	4.1	4.4	
19	Y2/G2 OUT	V_{19}	–	1.0	1.3	1.6	
20	AR2 OUT	V_{20}	–	3.8	4.1	4.4	
21	Cb2/B2 OUT	V_{21}	–	1.0	1.3	1.6	
23	Cr2/R2 OUT	V_{23}	–	1.0	1.3	1.6	
28	XTAL	V_{28}	–	3.8	4.05	4.3	
30	VD IN	V_{30}	–	1.2	1.45	1.7	
31	HD IN	V_{31}	–	1.2	1.45	1.7	
33	SYNC1 IN	V_{33}	–	1.5	1.8	2.1	
34	Yvi OUT	V_{34}	–	1.9	2.2	2.5	
35	AR1 IN	V_{35}	–	4.2	4.4	4.6	
36	CVBS3 IN	V_{36}	–	2.0	2.3	2.6	
37	AL1 IN	V_{37}	–	4.2	4.4	4.6	
38	CVBS4 IN	V_{38}	–	2.0	2.3	2.6	
39	AR8 IN/DC1	V_{39}	–	4.2	4.4	4.6	
40	AL8 IN/DC2	V_{40}	–	4.2	4.4	4.6	

Pin No.	Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
41	CVBS5 IN	V_{41}	–	2.0	2.3	2.6	V
42	AR2 IN	V_{42}	–	4.2	4.4	4.6	
43	AL2 IN	V_{43}	–	4.2	4.4	4.6	
45	Cr1/R1 IN	V_{45}	–	2.6	2.9	3.2	
46	AR9 IN/DC4	V_{46}	–	4.2	4.4	4.6	
47	Cb1/B1 IN	V_{47}	–	2.6	2.9	3.2	
48	AL9 IN/DC5	V_{48}	–	4.2	4.4	4.6	
49	Y1/G1 IN	V_{49}	–	2.0	2.3	2.6	
51	Cr3/R3 IN	V_{51}	–	2.6	2.9	3.2	
52	AR3 IN	V_{52}	–	4.2	4.4	4.6	
53	Cb3/B3 IN	V_{53}	–	2.6	2.9	3.2	
54	AL3 IN	V_{54}	–	4.2	4.4	4.6	
55	Y3/G3 IN	V_{55}	–	2.0	2.3	2.6	
56	AR4 IN	V_{56}	–	4.2	4.4	4.6	
57	SY1 IN	V_{57}	–	2.0	2.3	2.6	
58	AL4 IN	V_{58}	–	4.2	4.4	4.6	
59	SC1 IN	V_{59}	–	2.6	2.9	3.2	
61	CVBS6 IN	V_{61}	–	2.0	2.3	2.6	
62	AR5 IN	V_{62}	–	4.2	4.4	4.6	
63	AL5 IN	V_{63}	–	4.2	4.4	4.6	
65	Cr2/R2 IN	V_{65}	–	2.6	2.9	3.2	
66	AR10 IN/DC9	V_{66}	–	4.2	4.4	4.6	
67	Cb2/B2 IN	V_{67}	–	2.6	2.9	3.2	
68	AL10 IN/DC10	V_{68}	–	4.2	4.4	4.6	
69	Y2/G2 IN	V_{69}	–	2.0	2.3	2.6	
71	Cr4/R4 IN	V_{71}	–	2.6	2.9	3.2	
72	AR6 IN	V_{72}	–	4.2	4.4	4.6	
73	Cb4/B4 IN	V_{73}	–	2.6	2.9	3.2	
74	AL6 IN	V_{74}	–	4.2	4.4	4.6	
75	Y4/G4 IN	V_{75}	–	2.0	2.3	2.6	
76	AR7 IN	V_{76}	–	4.2	4.4	4.6	
77	SY2 IN	V_{77}	–	2.0	2.3	2.6	
78	AL7 IN	V_{78}	–	4.2	4.4	4.6	
79	SC2 IN	V_{79}	–	2.6	2.9	3.2	

Audio Block

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
I/O gain for Fixed mode (AL/AR1, AL/AR2, AL/AR3)		Gauf	Input = 2.8 Vp-p, 1 kHz, input resistance 5.6 kΩ	-1.0	0	1.0	dB
I/O gain for ATT mode (AL/AR1, AL/AR2)	AU ATT = min	Gaumin		—	-90	-80	
	AU ATT = max	Gaumax		0	1.0	2.0	
I/O frequency characteristic		fau	-3 dB point, Note A	100	—	—	kHz
Total harmonic distortion Fixed mode (AL/AR1, AL/AR2, AL/AR3)		thdf	input = 2.8 Vp-p 1 kHz, Note A	—	0.02	0.05	%
Total harmonic distortion for ATT mode (AL/AR1, AL/AR2)	AU ATT = max	thdmax		—	0.1	0.3	
Input dynamic range		Vdyau	Note A, Note B	5.6	6.5	—	Vp-p
Output offset voltage		Vauswof	Offset on AU1(2,3) OUT between AU1(2,3) OUT = 0000 to 1010	-30	0	30	mV
ATT Control offset		Vattof	Offset on AU1(2) OUT between AU1(2) ATT = max to min	-100	0	100	mV
Ripple rejection ratio		Vrrr	100 Hz and 100 mVp-p ripple is added to AU Vcc, Note A	30	45	—	dB
Mute mode attenuation		Gaumute	Input = 2.8Vp-p, 1 kHz, Note A	75	85	—	dB
Crosstalk among inputs		Gaucrs	Input = 2.8Vp-p, 1 kHz, Note A	75	85	—	dB
S/N ratio		Gausn	Input = 2.8Vp-p, 1 kHz, Note A	80	90	—	dB
Input impedance of input pins		Imau1	Pins 35, 37, 42, 43, 52, 54, 56, 58, 62, 63, 72, 74, 76, 78	65	87	109	kΩ
		Imau2	AU8/9/10 = 1 (Audio input mode), Pins 39, 40, 46, 48, 66, 68	65	87	109	
		Imaudc	AU8/9/10 = 0 (DC input mode), Pins 39, 40, 46, 48, 66, 68	122	163	204	

Note A: This parameter is not tested during production and is provided only as information to assist the design of applications.

Note B: Input = 1 kHz. The amplitude when the total harmonic distortion becomes 1%.

Video Block

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Input dynamic range	Sync-tip clamp mode	Vdsync	FILPASS = 0, BANDWIDTH = max, Sine wave input for Bias mode, Y with sync for others.	1.5	1.7	—	Vp-p
	Bias mode	Vdbias		1.4	2.1	—	
	Monitor out	Vdmoni		1.35	1.5	—	
I/O gain	GAIN = -3 dB	G-3	CVBS-OUT, YCbCr-OUT FILPASS = 0/1, input = 0.2Vp-p 10 kHz, BANDWIDTH = cnt, f0 SW = 1	-3.5	-3.0	-2.5	dB
	GAIN = 0 dB	G0		-0.5	0	0.5	
	GAIN = +3 dB	G+3		2.5	3.0	3.5	
	GAIN = +6 dB	G+6	MONITOR OUT	5.5	6.0	6.5	
	Yvi-OUT	Gyvi	Yvi-OUT	-0.5	0	0.5	
YC MIX gain		Gycmy	SY-IN to MONITOR-OUT, no input into SC-IN, YC MIX = 1	5.5	6.0	6.5	dB
		Gycmc	SC-IN to MONITOR-OUT, no input into SY-IN, YC MIX = 1	5.5	6.0	6.5	

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
I/O frequency characteristic 1-1 (YCbCr)	YCbCr GAIN = -3 dB	fg-3	FILPASS = 1, 0.2 Vp-p input, -3 dB point, Note A	80	100	—	MHz
	YCbCr GAIN = 0 dB	fg0		80	100	—	
	YCbCr GAIN = +3 dB	fg+3		80	100	—	
I/O frequency characteristic 1-2 (YCbCr)	BANDWIDTH = max	fLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, 0.2 Vp-p input, -3 dB point, Note A	14.0	16.5	18.0	MHz
	BANDWIDTH = cnt	fLcnt		9.5	10.5	11.5	
	BANDWIDTH = min	fLmin		4.2	4.7	5.2	
I/O frequency characteristic 1-3 (YCbCr)	BANDWIDTH = max	fHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, 0.2 Vp-p input, -3 dB point, Note A	41	46	51	MHz
	BANDWIDTH = cnt	fHcnt		27	30.3	34	
	BANDWIDTH = min	fHmin		12	13.4	15	
I/O frequency characteristic 1-4 (CbCr)	BANDWIDTH = max	fhfLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, fc HALF = 1, -3 dB point, Note A	7.4	8.3	9.1	MHz
	BANDWIDTH = cnt	fhfLcnt		4.6	5.2	5.8	
	BANDWIDTH = min	fhfLmin		2.1	2.4	2.6	
I/O frequency characteristic 1-5 (CbCr)	BANDWIDTH = max	fhfHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, fc HALF = 1, 0.2 Vp-p input, -3 dB point, Note A	21	24.1	27	MHz
	BANDWIDTH = cnt	fhfHcnt		14	15.7	18	
	BANDWIDTH = min	fhfHmin		6.0	6.8	8.0	
Differential 1-1 of frequency characteristic among YCbCr outputs	YCbCr GAIN = -3 dB	fdg-3	FILPASS = 1, 0.2 Vp-p input, -3 dB point, Note A	—	0	—	MHz
	YCbCr GAIN = 0 dB	fdg0		—	0	—	
	YCbCr GAIN = +3 dB	fdg+3		—	0	—	
Differential 1-2 of frequency characteristic among YCbCr outputs	BANDWIDTH = max	fdHmax	FILPASS = 0, f0 SW = 0, 0.2 Vp-p input, -3 dB point, Note A	-0.90	0	0.90	MHz
	BANDWIDTH = cnt	fdLcnt		-0.5	0	0.5	
	BANDWIDTH = min	fdHmin		-0.23	0	0.23	
Differential 1-3 of frequency characteristic among YCbCr outputs	BANDWIDTH = max	fdHmax	FILPASS = 0, f0 SW = 1, 0.2 Vp-p input, -3 dB point, Note A	-3.2	0	3.2	MHz
	BANDWIDTH = cnt	fdHcnt		-1.05	0	1.05	
	BANDWIDTH = min	fdHmin		-0.70	0	0.70	
I/O delay time 1-1 (YCbCr)	YCbCr GAIN = -3 dB	TdL-3	FILPASS = 1, 1 MHz, Note A	—	4	10	ns
	YCbCr GAIN = 0 dB	TdL0		—	4	10	
	YCbCr GAIN = +3 dB	TdL+3		—	4	10	
I/O delay time 1-2 (YCbCr)	BANDWIDTH = max	TdLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, 1 MHz, Note A	28	33	38	ns
	BANDWIDTH = cnt	TdLcnt		45	48	55	
	BANDWIDTH = min	TdLmin		96	107	120	
I/O delay time 1-3 (YCbCr)	BANDWIDTH = max	TdHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, 1 MHz, Note A	10	16	20	ns
	BANDWIDTH = cnt	TdHcnt		15	20	25	
	BANDWIDTH = min	TdHmin		35	39	45	

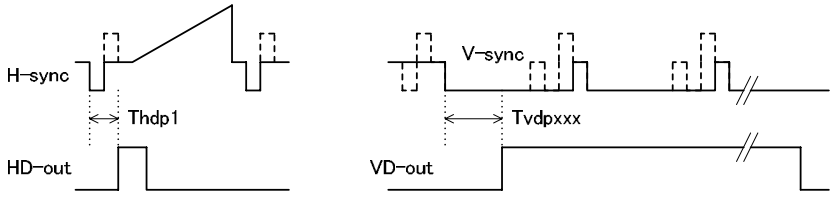
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
I/O delay time 1-4 (CbCr)	BANDWIDTH = max	TdhfLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, fc HALF = 1, 1 MHz, Note A	55	60	65	ns
	BANDWIDTH = cnt	TdhfLcnt		80	91	100	
	BANDWIDTH = min	TdhfLmin		190	220	260	
I/O delay time 1-5 (CbCr)	BANDWIDTH = max	TdhfHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, fc HALF = 1, 1 MHz, Note A	20	24	30	ns
	BANDWIDTH = cnt	TdhfHcnt		29	34	39	
	BANDWIDTH = min	TdhfHmin		66	72	80	
Differential 1-1 of delay time among YCbCr outputs	YCbCr GAIN = -3 dB	Tddg-3	FILPASS = 1, 1 MHz, Note A	-10	0	10	ns
	YCbCr GAIN = 0 dB	Tddg0		-10	0	10	
	YCbCr GAIN = +3 dB	Tddg+3		-10	0	10	
Differential 1-2 of delay time among YCbCr outputs	BANDWIDTH = max	TddHmax	FILPASS = 0, f0 SW = 0, 1 MHz, Note A	-10	0	10	ns
	BANDWIDTH = cnt	TddHcnt		-10	0	10	
	BANDWIDTH = min	TddHmin		-10	0	10	
Differential 1-3 of delay time between Y and Cb/Cr outputs	BANDWIDTH = max	TddHmax	FILPASS = 0, f0 SW = 1, fc HALF = 1, 1 MHz, Note A	0	8	20	ns
	BANDWIDTH = cnt	TddHcnt		5	14	20	
	BANDWIDTH = min	TddHmin		25	33	45	
Differential 1-4 of delay time between Cb and Cr outputs	BANDWIDTH = max	TddHmax	FILPASS = 0, f0 SW = 0, fc HALF = 1, 1 MHz, Note A	-10	0	10	ns
	BANDWIDTH = cnt	TddHcnt		-10	0	10	
	BANDWIDTH = min	TddHmin		-20	0	20	
I/O frequency characteristic 2-1 (CVBS)	CVBS GAIN = -3 dB	fg-3c	FILPASS = 1, 0.2 Vp-p input, -3 dB point, Note A	60	80	—	MHz
	CVBS GAIN = 0 dB	fg0c		60	80	—	
	CVBS GAIN = +3 dB	fg+3c		60	80	—	
I/O frequency characteristic 2-2 (CVBS)	BANDWIDTH = max	fmaxc	FILPASS = 0, GAIN = 00, 0.2 Vp-p input, -3 dB point, Note A	14.0	16.4	18.0	MHz
	BANDWIDTH = cnt	fcntc		9.5	10.6	11.5	
	BANDWIDTH = min	fminc		4.1	4.6	4.9	
I/O delay time 2-1 (CVBS)	CVBS GAIN = -3 dB	TdL-3	FILPASS = 1, 1 MHz, Note A	—	5	10	ns
	CVBS GAIN = 0 dB	TdL0		—	5	10	
	CVBS GAIN = +3 dB	TdL+3		—	5	10	
I/O delay time 2-2 (CVBS)	BANDWIDTH = max	Tdmaxc	FILPASS = 0, GAIN = 00, 1 MHz, Note A	30	34	40	ns
	BANDWIDTH = cnt	Tdcntc		45	49	55	
	BANDWIDTH = min	Tdminc		100	108	120	
I/O frequency characteristic 3 (MONITOR)		fgm	0.2 Vp-p input, -3 dB point, Note A	60	80	—	MHz
I/O frequency characteristic 4 (Yvi)		fgm	0.2 Vp-p input, -3 dB point, Note A	80	100	—	MHz
Mute mode attenuation		Gmute	5 MHz sin wave input, Note A	—	-70	-60	dB
Crosstalk	Among input channels	Gcrschs	5 MHz sin wave input, Note A	—	-70	-60	dB
	Among inputs in a channel	Gcrsins		—	-60	-55	
	HD, VD, FB or SYNC-in to Video-outs	Gcrsync	While HD, VD or FB-out is output. BANDWIDTH=min, NOTE A	—	3	—	mV

Synchronization Block (Test Condition: A-SYNC = 1 (ON))

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
H/V-sync separation level	525/60i	Vsep100	HV-SEP = 00, Note A, Note C	12	18	24	%
		Vsep101	HV-SEP = 01, Note A, Note C	20	26	32	
		Vsep110	HV-SEP = 10, Note A, Note C	26	31	38	
		Vsep111	HV-SEP = 11, Note A, Note C	38	43	50	
	1125/60i	Vsep200	HV-SEP = 00, Note A, Note C	20	25	30	%
		Vsep201	HV-SEP = 01, Note A, Note C	28	33	38	
		Vsep210	HV-SEP = 10, Note A, Note C	33	38	43	
		Vsep211	HV-SEP = 11, Note A, Note C	45	50	55	
	SVGA/60	Vsep300	HV-SEP = 00, Note A, Note C	14	20	26	%
		Vsep301	HV-SEP = 01, Note A, Note C	21	27	33	
		Vsep310	HV-SEP = 10, Note A, Note C	27	33	39	
		Vsep311	HV-SEP = 11, Note A, Note C	38	44	50	
Threshold amplitude for HD input		VthHD	HV OUT = 1	0.8	—	—	Vp-p
Threshold amplitude for VD input		VthVDn	HV OUT = 1	0.9	—	—	Vp-p
HD-OUT voltage		VhdH	High level	1.0	1.2	1.4	V
		VhdL	Low level	—	0.1	0.4	
HD-OUT width		Thdw0	HD WIDTH = 0	1.6	1.7	1.8	µs
		Thdw1	HD WIDTH = 1	0.6	0.7	0.8	
HD-OUT phase	H sync-in to HD-out	Thdp1	HV OUT = 0, 1125/60p input, Note D	70	90	110	ns
	HD-in to HD-out	Thdp2	HV OUT = 1, Note A	25	34	40	ns
VD-OUT voltage		VvdH	High level	1.0	1.2	1.4	V
		VvdL	Low level	—	0.1	0.4	
VD-OUT width	Sync sep	Tvdws	Separated VD-OUT	—	290	—	µs
	1250i ODD	Tvdwodd	When 1250i input	—	285	—	µs
	1250i EVEN	Tvdweven		—	270	—	
	Free-run 1	Tvdwfi	Free-run VD-OUT in interlace mode	—	4	—	H
	Free-run 2	Tvdwfp	Free-run VD-OUT in progressive mode	—	8	—	
VD-OUT phase	V sync-in to VD-out	Tvdp	Except 1250/50i input, Note D	0.15	0.20	0.25	H
	H sync-in to VD-out	Tvdp1250	1250/50i input, H sync-in to VD-out, Note D	310	320	330	ns
	VD-in to VD-out	Tvdphv	HV OUT = 1, Note A	25	34	40	ns

Note C: 286 mVp-p sync input for 525/60i, 0.3 Vp-p sync input for 1125/60i and SVGA/60.

Note D: See the figures below.



Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Dummy HD-OUT frequency	fh156	HV FREQ2 = 00000, H DMY = 1	—	15.564	—	kHz
	fh157/60i	HV FREQ2 = 00001, H DMY = 1	—	15.701	—	
	fh312	HV FREQ2 = 00010, H DMY = 1	—	31.401	—	
	fh315	HV FREQ2 = 00011, H DMY = 1	—	31.401	—	
	fh281/50i	HV FREQ2 = 00100, H DMY = 1	—	27.966	—	
	fh337/60i	HV FREQ2 = 00101, H DMY = 1	—	33.771	—	
	fh375	HV FREQ2 = 00110, H DMY = 1	—	37.288	—	
	fh450	HV FREQ2 = 00111, H DMY = 1	—	44.746	—	
	fh1250	HV FREQ2 = 01000, H DMY = 1	—	31.401	—	
	fh379	HV FREQ2 = 01001, H DMY = 1	—	37.288	—	
	fh640	HV FREQ2 = 01010, H DMY = 1	—	66.288	—	
	fh750	HV FREQ2 = 01011, H DMY = 1	—	74.577	—	
	fh562	HV FREQ2 = 01100, H DMY = 1	—	55.932	—	
	fh157/30p	HV FREQ2 = 10000, H DMY = 1	—	15.700	—	
	fh270	HV FREQ2 = 10001, H DMY = 1	—	27.117	—	
	fh281/25p	HV FREQ2 = 10010, H DMY = 1	—	27.965	—	
	fh337/30p	HV FREQ2 = 10011, H DMY = 1	—	33.769	—	
	fh270/48sf	HV FREQ2 = 10100, H DMY = 1	—	27.965	—	
Dummy VD-OUT frequency	fv625i	HV FREQ2 = 00000, V DMY = 1	—	312.5	—	H
	fv525i	HV FREQ2 = 00001, V DMY = 1	—	262.5	—	
	fv625p	HV FREQ2 = 00010, V DMY = 1	—	625	—	
	fv525p	HV FREQ2 = 00011, V DMY = 1	—	525	—	
	fv1125i50	HV FREQ2 = 00100, V DMY = 1	—	562.5	—	
	fv1125i60	HV FREQ2 = 00101, V DMY = 1	—	562.5	—	
	fv750p50	HV FREQ2 = 00110, V DMY = 1	—	750	—	
	fv750p60	HV FREQ2 = 00111, V DMY = 1	—	750	—	
	fv1250iO	HV FREQ2 = 01000, V DMY = 1, ODD	—	624.5	—	
	fv1250iE	HV FREQ2 = 01000, V DMY = 1, EVEN	—	625.5	—	
	fvsvga	HV FREQ2 = 01001, V DMY = 1	—	628	—	
	fvsxga	HV FREQ2 = 01010, V DMY = 1	—	1066	—	
	fvuxga	HV FREQ2 = 01011, V DMY = 1	—	1250	—	
	fv1125p50	HV FREQ2 = 01100, V DMY = 1	—	1125	—	
	fv525p30	HV FREQ2 = 10000, V DMY = 1	—	525	—	
	fv1125p24	HV FREQ2 = 10001, V DMY = 1	—	1125	—	
	fv1125p25	HV FREQ2 = 10010, V DMY = 1	—	1125	—	
	fv1125p30	HV FREQ2 = 10011, V DMY = 1	—	1125	—	
	fv1125s24	HV FREQ2 = 10100, V DMY = 1	—	562.5	—	

Other Blocks

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
XTAL oscillation amplitude		Vosc	Note A, Note E	—	0.4	—	Vp-p
FB input threshold voltage		VthFB	Pins 44, 50, 64, 70	0.6	0.75	0.9	V
FB-OUT voltage		VfbH	High level	1.0	1.2	1.4	V
		VfbL	Low level	—	0.1	0.4	
I/O delay time for FB	DL OFF	Tfbdoff	FB DL = 0	20	40	60	ns
	DL ON	Tfbdon	FB DL = 1	50	70	90	
No signal detection filter		tnsfil1	SIG LPF = 1, Note F, Note A	0.5	1.3	1.8	μs
Impedance for no-signal detection filter		Imnsfil200	SIG DET IMPE = 00, Note G	14	20	26	kΩ
		Imnsfil201	SIG DET IMPE = 01, Note G	11	15	19	
		Imnsfil210	SIG DET IMPE = 10, Note G	7	10	13	
		Imnsfil211	SIG DET IMPE = 11, Note G	4.2	6.0	7.8	
No signal detection threshold voltage		Vthns00	SIG DET LVL = 00, Note H	0.45	0.55	0.65	V
		Vthns01	SIG DET LVL = 01, Note H	0.70	0.80	0.90	
		Vthns10	SIG DET LVL = 10, Note H	0.95	1.05	1.15	
		Vthns11	SIG DET LVL = 11, Note H	1.20	1.30	1.40	
DC detection threshold (DC)	L⇔M	VdcthLM	Pins 39, 40, 44, 46, 48, 50, 60, 64, 66, 68, 70, 80	0.8	1.0	1.2	V
	M⇔H	VdcthMH		2.8	3.0	3.2	
DC detection threshold (S)		VdcthS	Pins 45, 47, 53, 59, 65, 67, 73, 79	0.8	1.0	1.2	V

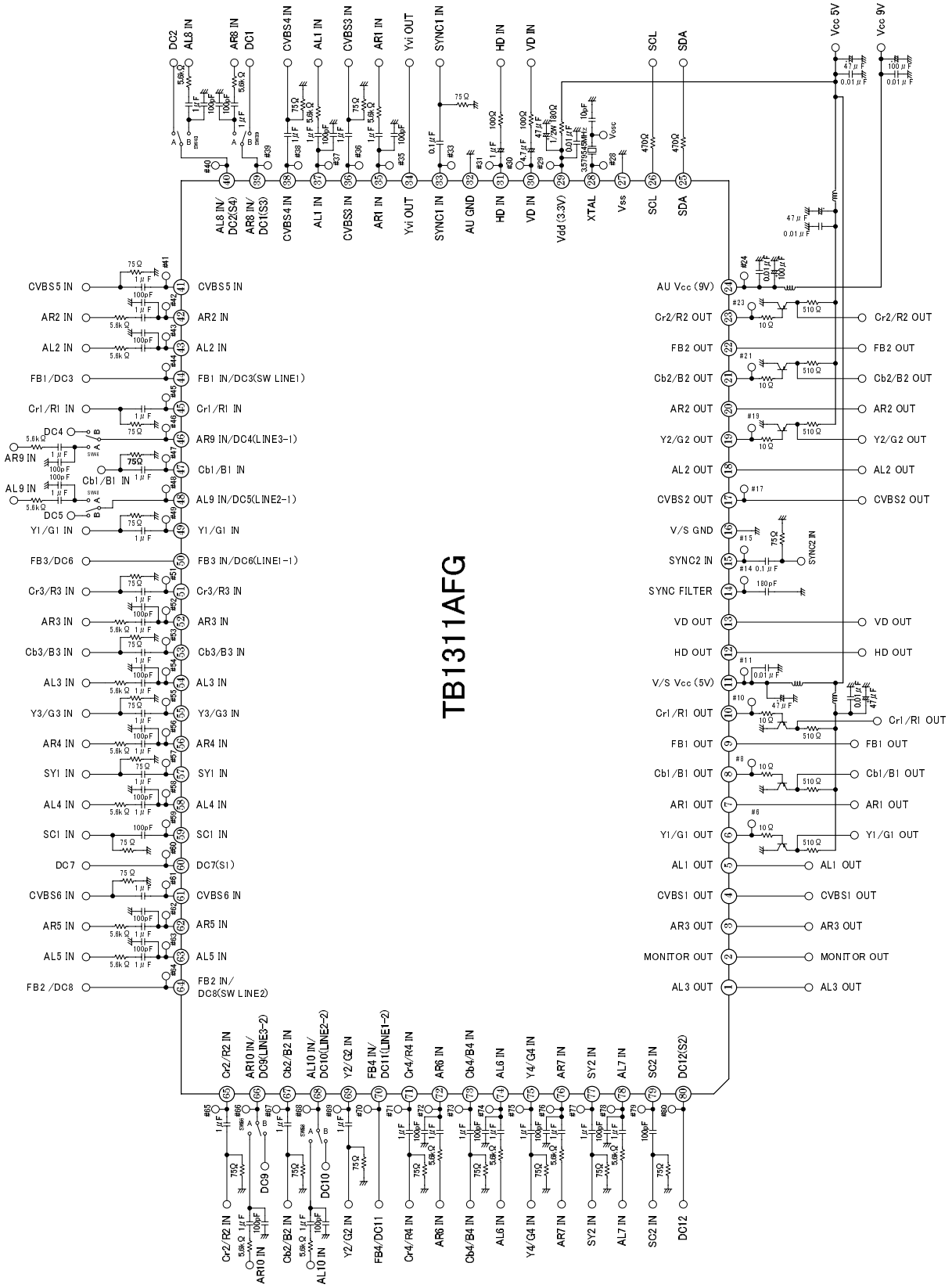
Note E: This is the amplitude of the oscillation wave at the point between the crystal and the series capacitor.

Note F: Remove the external capacitor connected with the SYNC FILTER pin (pin 14), HV SEP1 = 00, SIG DET IMPE = 11. The delay time from SYNC1-IN input (525/60i) to the SYNC FILTER waveform.

Note G: Remove the external capacitor connected with the SYNC FILTER pin (pin 14). Connect 10 kΩ resistor between the SYNC FILTER pin and GND. No input into SYNC1-IN. Measure the current (Ir) on the resistor. Imnsfil2xx = 3.3 / Ir – 10 kΩ.

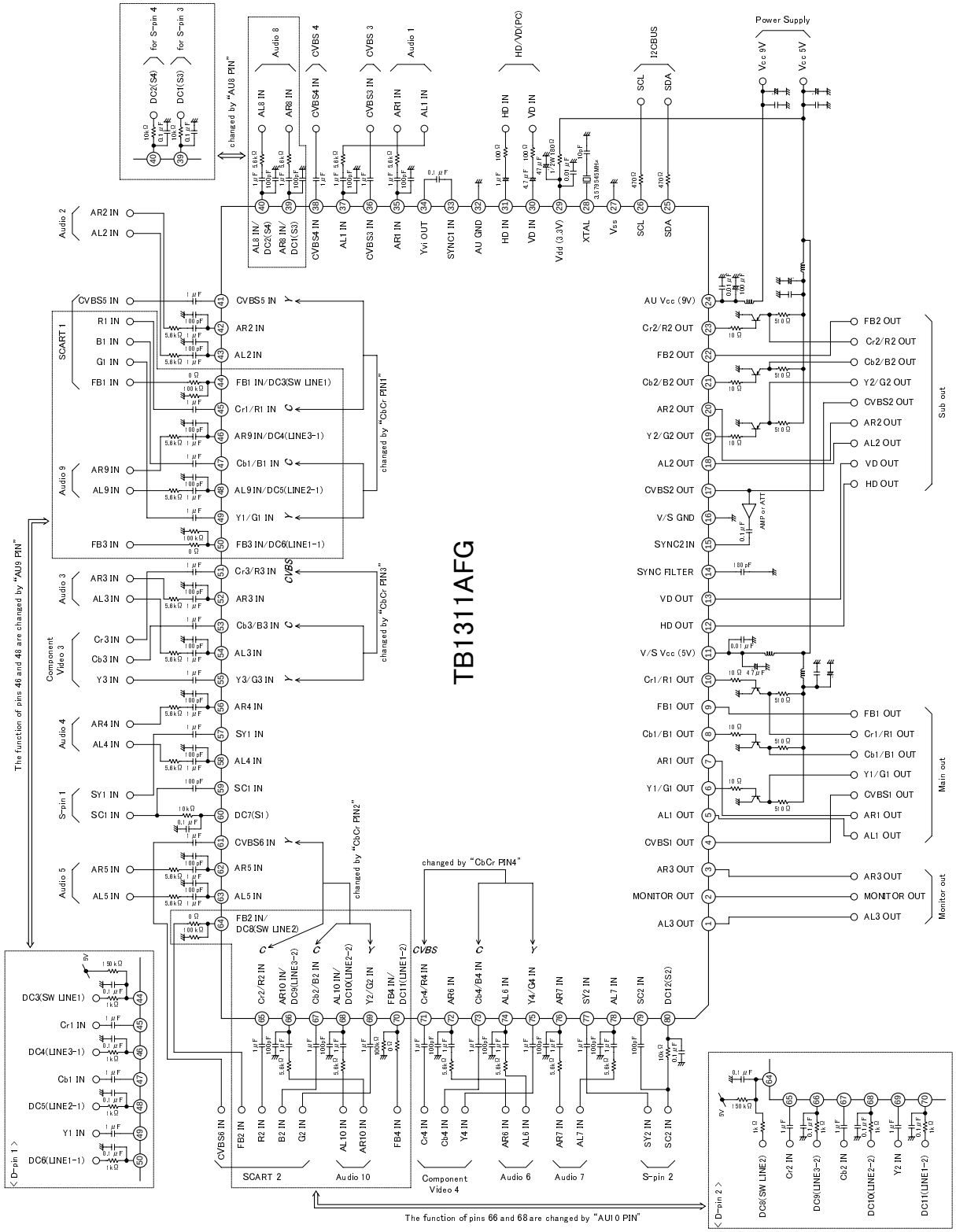
Note H: Remove the external capacitor connected with the SYNC FILTER pin (pin 14). Input a 0 V - Vthnsxx [V] pulse of 15.7 kHz into the SYNC FILTER pin. The pulse voltage during SIG DET status changes.

Test Circuit



Components in test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure in the application equipment.

Application Circuit 1 (Typical Values)



Input video signals driven with low impedance.

The application circuits shown in this document are examples provided for reference purposes only. Thorough evaluation is required in the mass production design phase.
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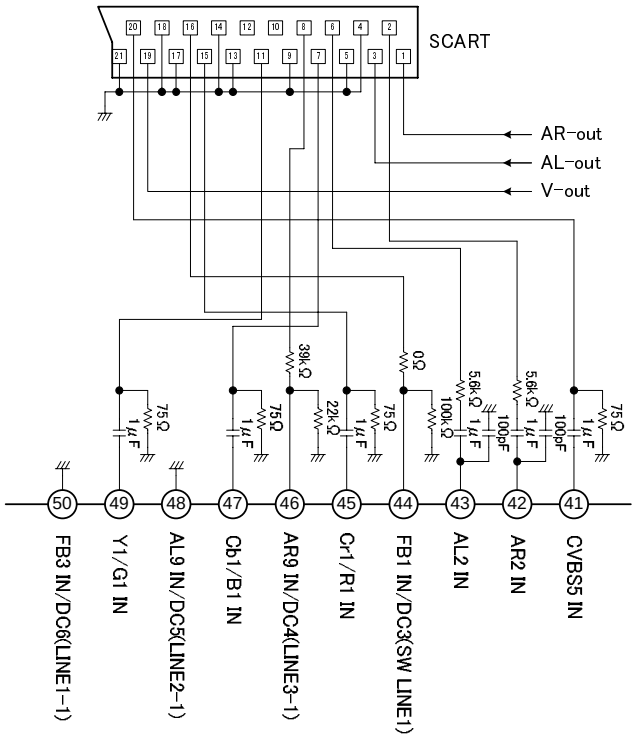
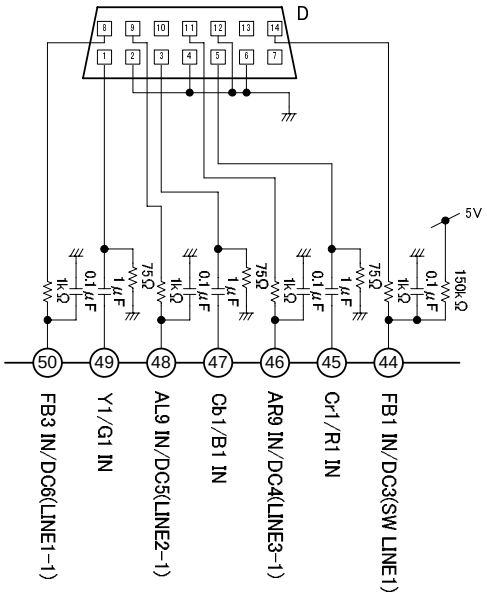
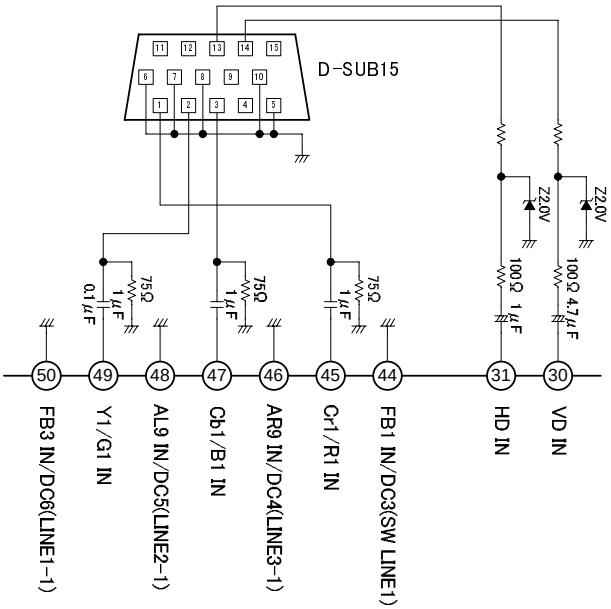
Application Circuit 2 (Examples of Connectors)



SCART connector



D-pin



D-SUB15

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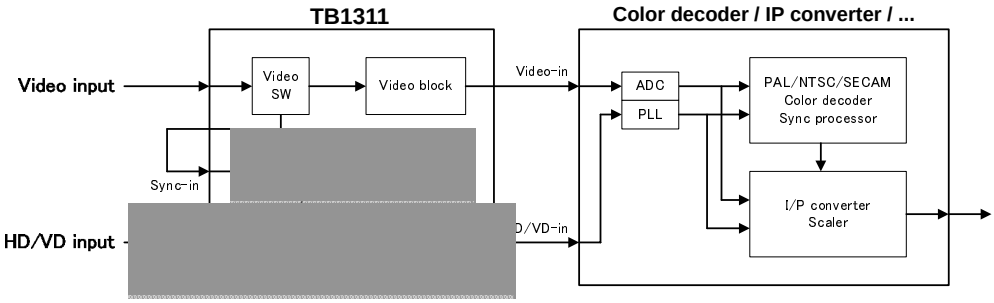
Application Circuit 3 (System Configuration)

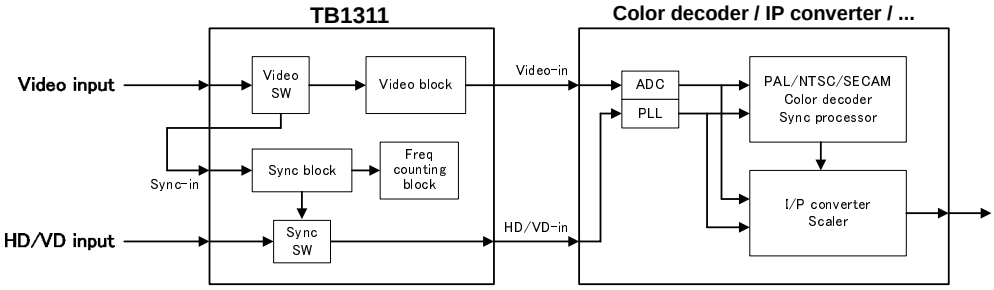
(1) For nonstandard signals such as CVBS, YC (S-video), 525i, 625i or so.



The TB1311AFG does not support weak signals, ghost signals or other nonstandard signals. Therefore, these signals should be dealt with through the use of another device capable of handling these signals, such as a color-decoder. In these cases, the signal switcher and the video circuits of the TB1311AFG can be used. In some cases, “no-input detection” can be also used for these signals.

The TB1311AFG cannot distinguish between component and RGB video. The different kinds of input signal should be separated through the use of different signal-specific input pins; for example, specific-purpose pins for RGB video input only or component video input only.

(2) For standard component video (SMPTE STANDARD) and standard RGB video (VESA STANDARD)



The TB1311AFG can detect a format type for standard signal inputs.

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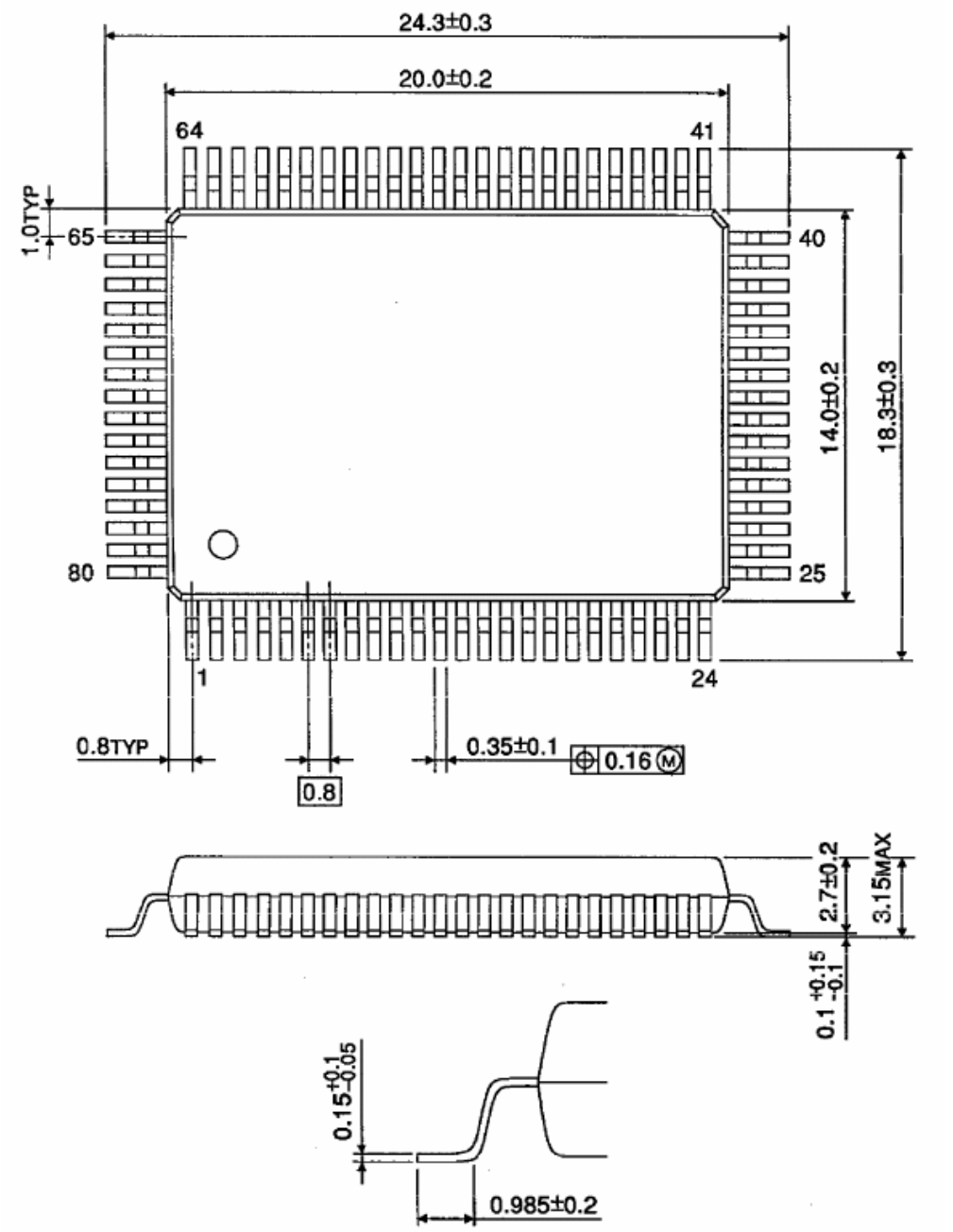
Package Dimensions

P-QFP80-1420-0.80C Unit: mm



Weight: 1.6 g (typ.)

About solderability, following conditions were confirmed

Solderability

(1) Use of Sn-37Pb solder Bath
- solder bath temperature = 230°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- solder bath temperature = 245°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

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