

2N5060 Series

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Annular PNP devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92/TO-226AA package which is readily adaptable for use in automatic insertion equipment.

Features

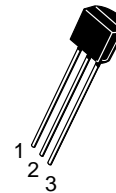
- Sensitive Gate Trigger Current – 200 μ A Maximum
- Low Reverse and Forward Blocking Current – 50 μ A Maximum, $T_C = 110^\circ\text{C}$
- Low Holding Current – 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Device Marking: Device Type, e.g., 2N5060, Date Code
- Pb-Free Packages are Available*



ON Semiconductor®

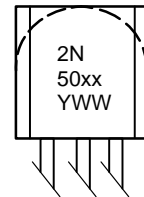
<http://onsemi.com>

SILICON CONTROLLED RECTIFIERS 0.8 A RMS, 30 – 200 V



TO-92
CASE 29
STYLE 10

MARKING DIAGRAM



50xx Specific Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

2N5060 Series

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to 110°C , Sine Wave, 50 to 60 Hz, Gate Open) 2N5060 2N5061 2N5062 2N5064	V_{DRM} , V_{RRM}	30 60 100 200	V
On-State Current RMS (180° Conduction Angles; $T_C = 80^\circ\text{C}$)	$I_{\text{T(RMS)}}$	0.8	A
*Average On-State Current (180° Conduction Angles) ($T_C = 67^\circ\text{C}$) ($T_C = 102^\circ\text{C}$)	$I_{\text{T(AV)}}$	0.51 0.255	A
*Peak Non-repetitive Surge Current, $T_A = 25^\circ\text{C}$ (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	A
Circuit Fusing Considerations ($t = 8.3$ ms)	I^2t	0.4	A^2s
*Average On-State Current (180° Conduction Angles) ($T_C = 67^\circ\text{C}$) ($T_C = 102^\circ\text{C}$)	$I_{\text{T(AV)}}$	0.51 0.255	A
*Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec ; $T_A = 25^\circ\text{C}$)	P_{GM}	0.1	W
*Forward Average Gate Power ($T_A = 25^\circ\text{C}$, $t = 8.3$ ms)	$P_{\text{G(AV)}}$	0.01	W
*Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec ; $T_A = 25^\circ\text{C}$)	I_{GM}	1.0	A
*Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μsec ; $T_A = 25^\circ\text{C}$)	V_{RGM}	5.0	V
*Operating Junction Temperature Range	T_J	-40 to +110	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-40 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta\text{JC}}$	75	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta\text{JA}}$	200	$^\circ\text{C/W}$
Lead Solder Temperature (Lead Length $\geq 1/16''$ from case, 10 s Max)	-	+230	$^\circ\text{C}$

- This measurement is made with the case mounted "flat side down" on a heatsink and held in position by means of a metal clamp over the curved surface.

*Indicates JEDEC Registered Data.

2N5060 Series

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

*Peak Repetitive Forward or Reverse Blocking Current (Note 3) ($V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$)	I_{DRM}, I_{RRM}	-	-	10	μA
$T_C = 25^\circ\text{C}$					
$T_C = 110^\circ\text{C}$		-	-	50	μA

ON CHARACTERISTICS

*Peak Forward On-State Voltage (Note 4) ($I_{TM} = 1.2 \text{ A peak @ } T_A = 25^\circ\text{C}$)	V_{TM}	-	-	1.7	V
Gate Trigger Current (Continuous DC) (Note 5) *($V_{AK} = 7.0 \text{ Vdc}, R_L = 100 \Omega$)	I_{GT}	-	-	200	μA
		-	-	350	
Gate Trigger Voltage (Continuous DC) (Note 5) *($V_{AK} = 7.0 \text{ Vdc}, R_L = 100 \Omega$)	V_{GT}	-	-	0.8	V
		-	-	1.2	
*Gate Non-Trigger Voltage ($V_{AK} = \text{Rated } V_{DRM}, R_L = 100 \Omega$) $T_C = 110^\circ\text{C}$	V_{GD}	0.1	-	-	V
Holding Current (Note 5) *($V_{AK} = 7.0 \text{ Vdc}$, initiating current = 20 mA)	I_H	-	-	5.0	mA
		-	-	10	
Turn-On Time Delay Time Rise Time ($I_{GT} = 1.0 \text{ mA}, V_D = \text{Rated } V_{DRM}$, Forward Current = 1.0 A, $di/dt = 6.0 \text{ A}/\mu\text{s}$)	t_d t_r	-	3.0 0.2	-	μs
Turn-Off Time (Forward Current = 1.0 A pulse, Pulse Width = 50 μs , 0.1% Duty Cycle, $di/dt = 6.0 \text{ A}/\mu\text{s}$, $dv/dt = 20 \text{ V}/\mu\text{s}, I_{GT} = 1 \text{ mA}$)	t_q	-	-	-	μs
	2N5060, 2N5061 2N5062, 2N5064	-	10	-	
		-	30	-	

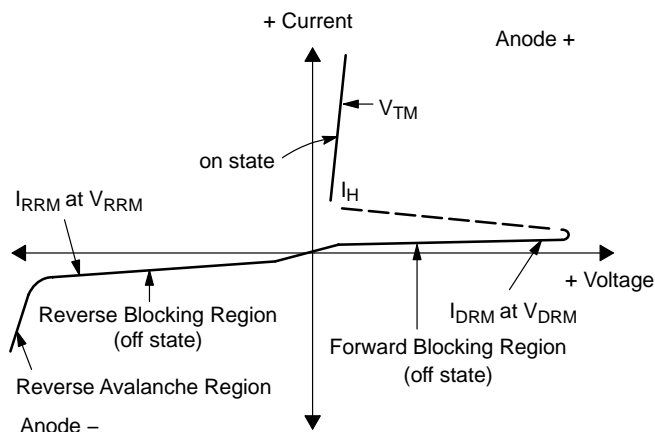
DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (Rated V_{DRM} , Exponential)	dv/dt	-	30	-	$\text{V}/\mu\text{s}$
---	---------	---	----	---	------------------------

3. $R_{GK} = 1000 \Omega$ is included in measurement.
 4. Forward current applied for 1 ms maximum duration, duty cycle $\leq 1\%$.
 5. R_{GK} current is not included in measurement.
- *Indicates JEDEC Registered Data.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current



2N5060 Series

CURRENT DERATING

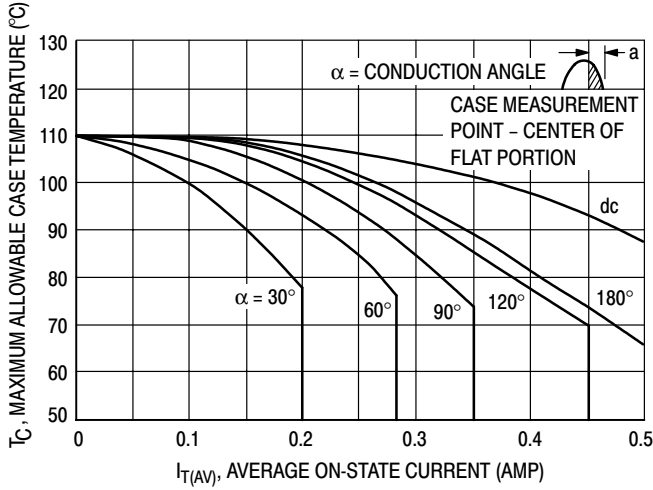


Figure 1. Maximum Case Temperature

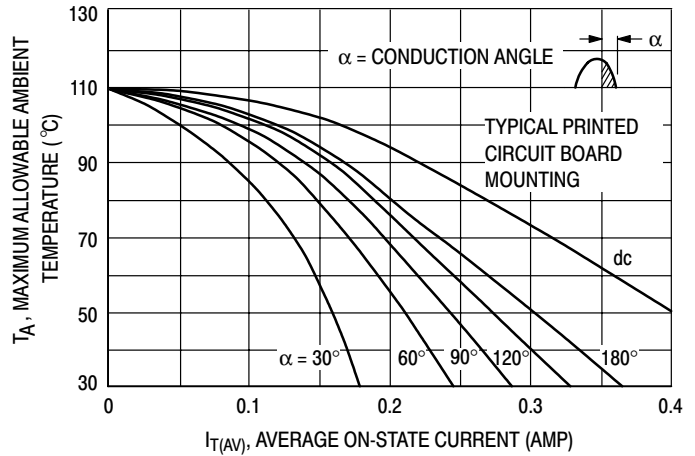


Figure 2. Maximum Ambient Temperature

CURRENT DERATING

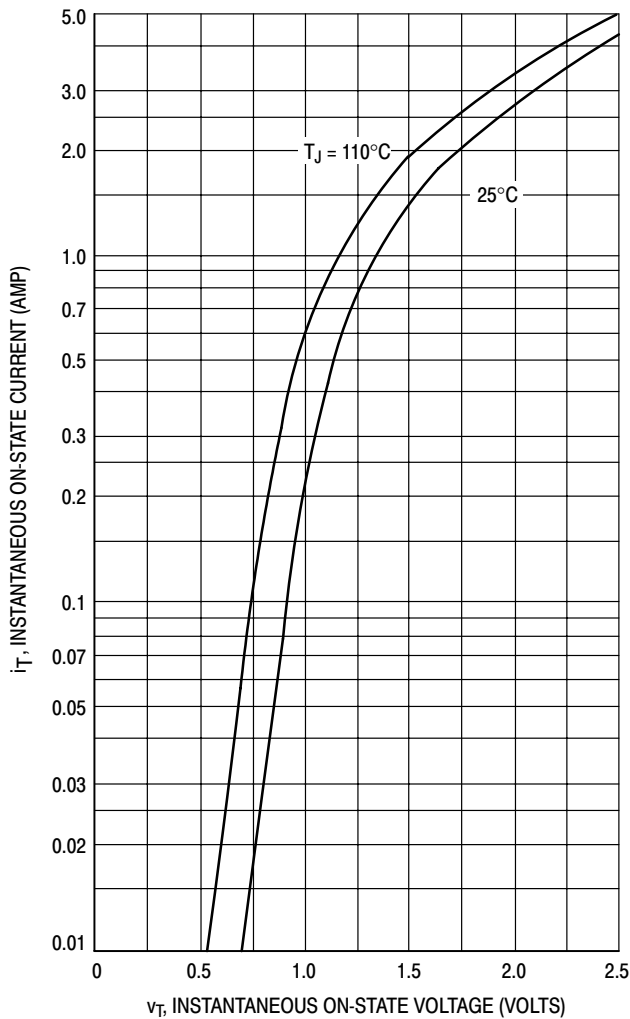


Figure 3. Typical Forward Voltage

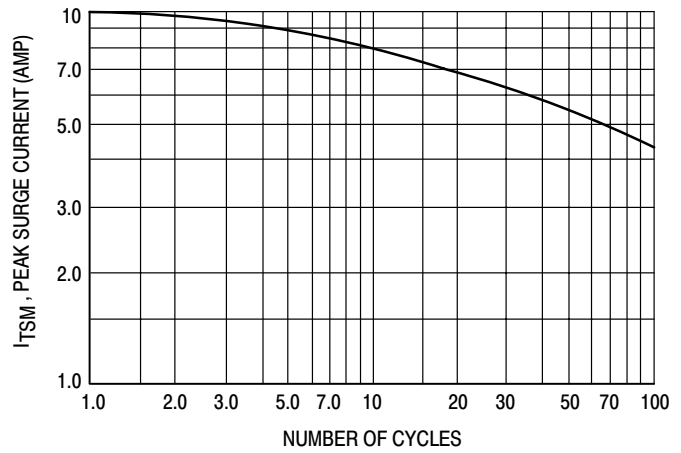


Figure 4. Maximum Non-Repetitive Surge Current

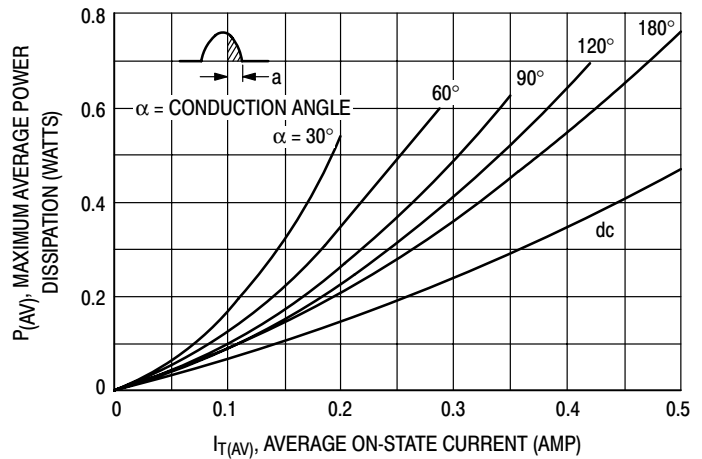


Figure 5. Power Dissipation

2N5060 Series

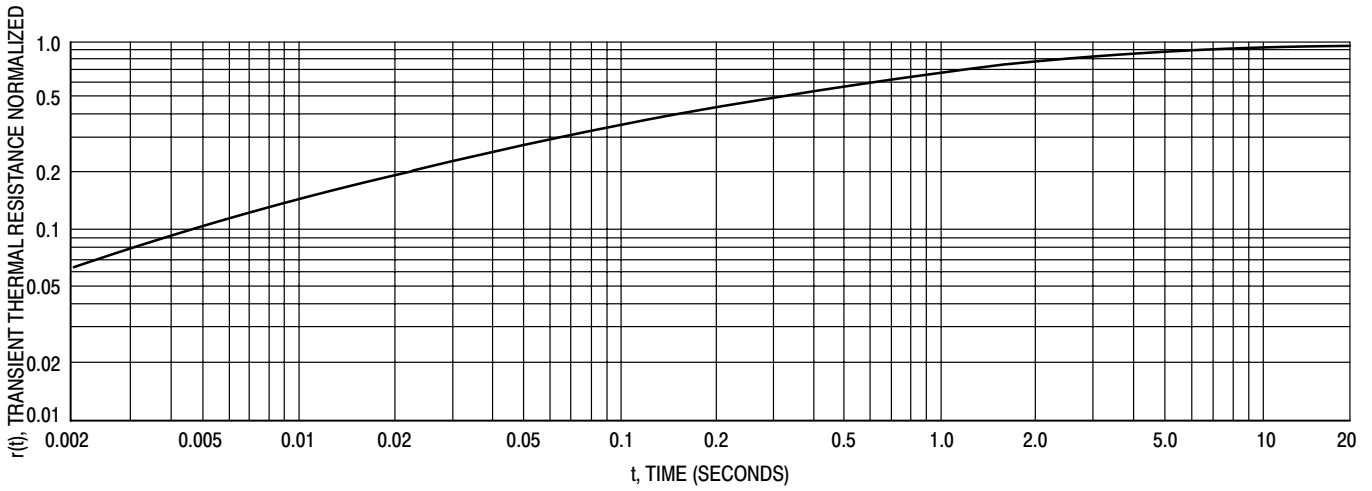


Figure 6. Thermal Response

TYPICAL CHARACTERISTICS

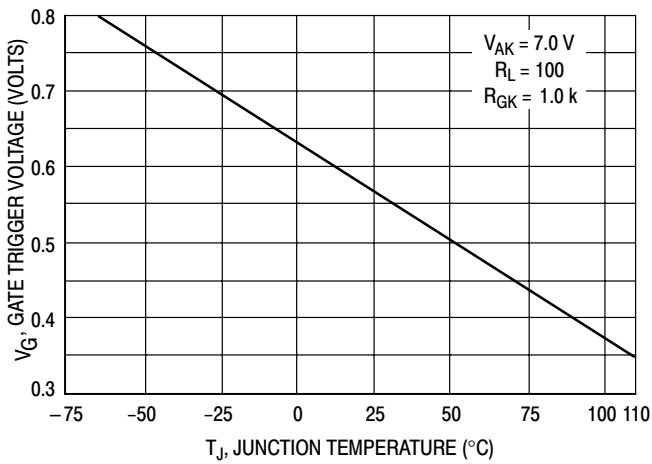


Figure 7. Typical Gate Trigger Voltage

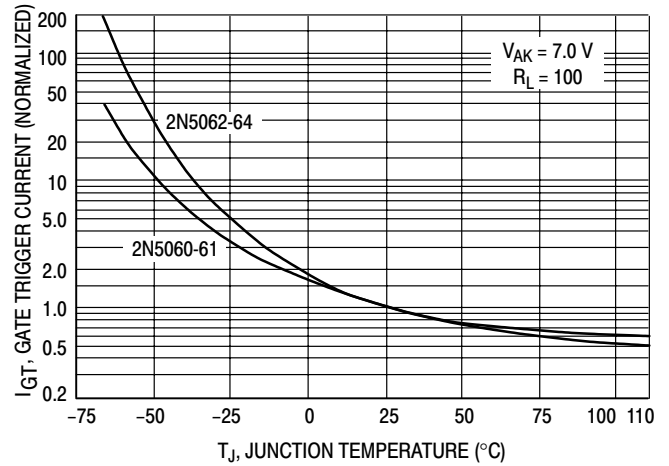


Figure 8. Typical Gate Trigger Current

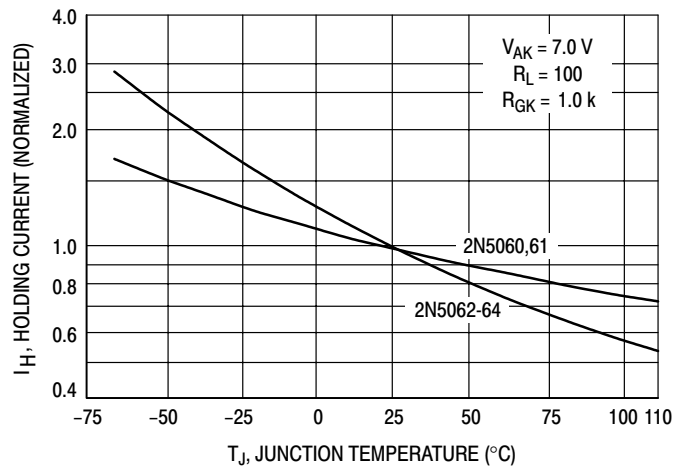


Figure 9. Typical Holding Current

2N5060 Series

ORDERING INFORMATION

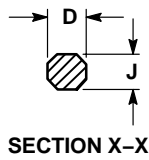
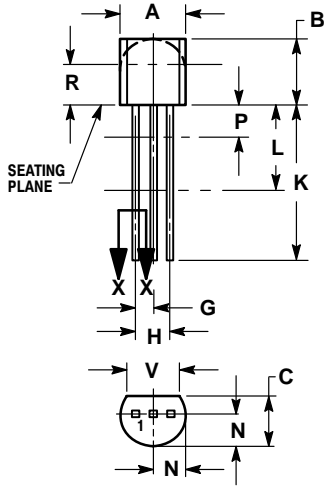
Device	Package	Shipping†
2N5060	TO-92	5,000 Units / Box
2N5060RLRA	TO-92	2,000 / Tape & Reel
2N5060RLRAG	TO-92 (Pb-Free)	2,000 / Tape & Reel
2N5060RLRM	TO-92	2,000 / Ammo Pack
2N5061	TO-92	5,000 Units / Box
2N5061G	TO-92 (Pb-Free)	5,000 Units / Box
2N5061RLRA	TO-92	2,000 / Tape & Reel
2N5061RLRAG	TO-92 (Pb-Free)	2,000 / Tape & Reel
2N5061RLRM	TO-92	2,000 / Ammo Pack
2N5062	TO-92	5,000 Units / Box
2N5062G	TO-92 (Pb-Free)	5,000 Units / Box
2N5062RLRA	TO-92	2,000 / Tape & Reel
2N5062RLRAG	TO-92 (Pb-Free)	2,000 / Tape & Reel
2N5064	TO-92	5,000 Units / Box
2N5064RLRA	TO-92	2,000 / Tape & Reel
2N5064RLRM	TO-92	2,000 / Ammo Pack
2N5064RLRMG	TO-92 (Pb-Free)	2,000 / Ammo Pack
2N5060RL1	TO-92	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2N5060 Series

PACKAGE DIMENSIONS

TO-92
TO-226AA
CASE 29-11
ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 10:

- PIN 1. CATHODE
2. GATE
3. ANODE

2N5060 Series

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.

2N5060/D