



ELECTRONICS, INC.
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NTE56015 thru NTE56018 TRIAC, 25 Amp

Description:

The NTE56015 through NTE56018 series of TRIACs are high performance glass passivated PNPN devices in a TO220 type package designed for general purpose applications where moderate gate sensitivity is required.

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Repetitive Peak Off-State Voltage ($T_J = -40^\circ$ to $+125^\circ\text{C}$, $R_{GK} = 1\text{k}\Omega$), V_{DRM}		
NTE56015	200V
NTE56016	400V
NTE56017	600V
NTE56018	800V
On-State Current (All Conduction Angles, $T_C = +85^\circ\text{C}$), $I_{\text{T(RMS)}}$		25A
Non-Repetitive On-State Current (Half Cycle), I_{TSM}		
60Hz	275A
50Hz	250A
Fusing Current ($t = 10\text{ms}$), I^2t		312A ² s
Peak Gate Current ($t = 10\mu\text{s}$ Max), I_{GM}		4A
Peak Gate Dissipation ($t = 10\mu\text{s}$ Max), P_{GM}		10W
Gate Dissipation ($t = 20\text{ms}$ Max), $P_{\text{G(AV)}}$		1W
Operating Junction Temperature Range, T_J		-40° to $+125^\circ\text{C}$
Storage Temperature Range, T_{stg}		-40° to $+125^\circ\text{C}$
Thermal Resistance, Junction-to-Case, R_{thJC}		1.5K/W
Thermal Resistance, Junction-to-Ambient, R_{thJA}		60K/W
Lead Temperature (During Soldering, 1.6mm from case, 10sec max), T_L		$+250^\circ\text{C}$

Electrical Characteristics: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off-State Leakage Current	I_{DRM}	$V_D = V_{\text{DRM}}$, $R_{\text{GK}} = 1\text{k}\Omega$, $T_J = +25^\circ\text{C}$	-	-	10	μA
		$V_D = V_{\text{DRM}}$, $R_{\text{GK}} = 1\text{k}\Omega$, $T_J = +125^\circ\text{C}$	-	-	3	mA
On-State Voltage	V_T	$I_T = 37.5\text{A}$, $T_J = +25^\circ\text{C}$	-	-	1.4	V
On-State Threshold Voltage	$V_{\text{T(TO)}}$	$T_J = +125^\circ\text{C}$	-	-	0.85	V
On-State Slope Resistance	r_T	$T_J = +125^\circ\text{C}$	-	-	13	$\text{m}\Omega$

Electrical Characteristics (Cont'd): ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Gate Trigger Current	I_{GT}	$V_D = 12\text{V}$, Note 1	–	–	50	mA
Gate Trigger Voltage	V_{GT}	$V_D = 12\text{V}$, All Quadrants	–	–	2.5	V
Holding Current	I_H	$R_{GK} = 1\text{k}\Omega$	–	–	50	mA
Critical Rate-of-Rise	dv/dt	$V_D = 0.67 \times V_{DRM}$, $R_{GK} = 1\text{k}\Omega$, $T_J = +125^\circ\text{C}$	500	–	–	V/ μs
Critical Rate-of-Rise, Off-State	dv/dt_c	$I_T = 25\text{A}$, $di/dt = 11\text{A/ms}$, $T_C = +85^\circ\text{C}$	5	–	–	V/ μs

Note 1. For either polarity of gate voltage with reference to electrode MT_1 .

