International
IOR Rectifier

PD -94030A

IRF7752

HEXFET® Power MOSFET

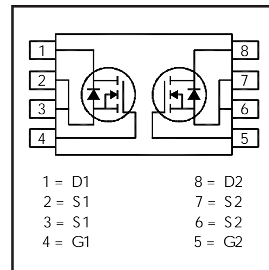
- Ultra Low On-Resistance
- Dual N-Channel MOSFET
- Very Small SOIC Package
- Low Profile (< 1.1mm)
- Available in Tape & Reel

V_{DSS}	$R_{DS(on)}$ max	I_D
30V	0.030@V_{GS} = 10V	4.6A
	0.036@V_{GS} = 4.5V	3.9A

Description

HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design , that International Rectifier is well known for, provides thedesigner with an extremely efficient and reliable device for use in battery and load management.

The TSSOP-8 package, has 45% less footprint area of the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium.
The low profile (<1.1mm) of the TSSOP-8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



TSSOP-8

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	30	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	±4.6	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 10V	±3.7	
I_{DM}	Pulsed Drain Current ①	±37	
P_D @T_A = 25°C	Power Dissipation	1.0	W
P_D @T_A = 70°C	Power Dissipation	0.64	
	Linear Derating Factor	8.0	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	125	°C/W

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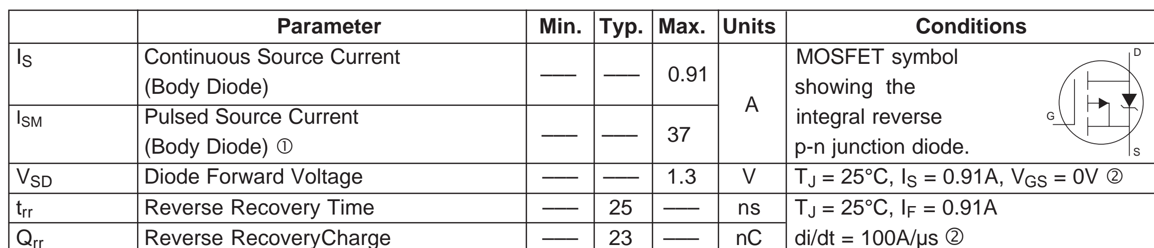
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.030	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.030	Ω	V_{GS} = 10V, I_D = 4.6A ②
		—	—	0.036		V_{GS} = 4.5V, I_D = 3.9A ②
$V_{GS(th)}$	Gate Threshold Voltage	0.60	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	12	—	—	S	V_{DS} = 10V, I_D = 4.6A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 24V, V_{GS} = 0V
		—	—	100		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-200	nA	V_{GS} = -12V
	Gate-to-Source Reverse Leakage	—	—	200		V_{GS} = 12V
Q_g	Total Gate Charge	—	9.0	—	nC	I_D = 4.6A
Q_{gs}	Gate-to-Source Charge	—	2.5	—		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.6	—		V_{GS} = 4.5V②
$t_{d(on)}$	Turn-On Delay Time	—	7.2	—	ns	V_{DD} = 15V
t_r	Rise Time	—	9.1	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		R_G = 6.0Ω
t_f	Fall Time	—	11	—		V_{GS} = 10V②
C_{iss}	Input Capacitance	—	861	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	210	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	25	—		f = 1.0MHz

Source-Drain Ratings and Characteristics



	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.91	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	37		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 0.91A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	25	—	ns	T_J = 25°C, I_F = 0.91A
Q_{rr}	Reverse RecoveryCharge	—	23	—	nC	di/dt = 100A/μs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 300μs; duty cycle ≤ 2%.

③ When mounted on 1 inch square copper board, t<10 sec

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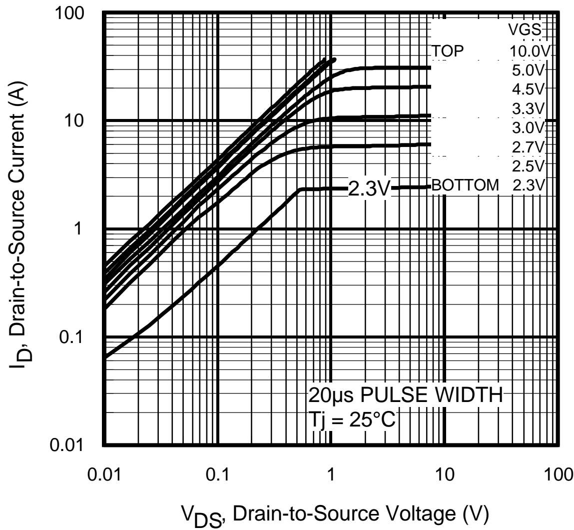

Fig 1. Typical Output Characteristics

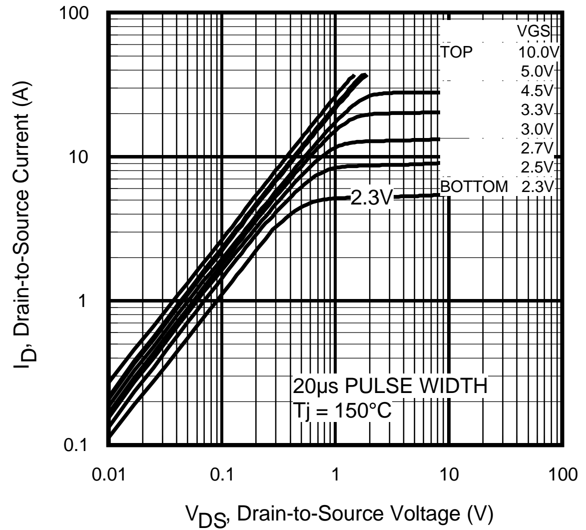

Fig 2. Typical Output Characteristics

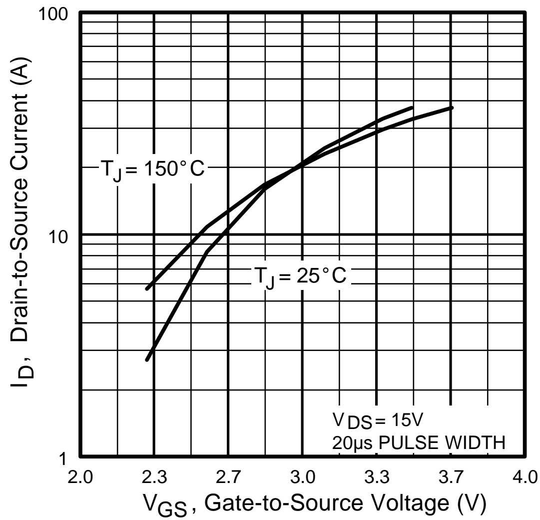

Fig 3. Typical Transfer Characteristics

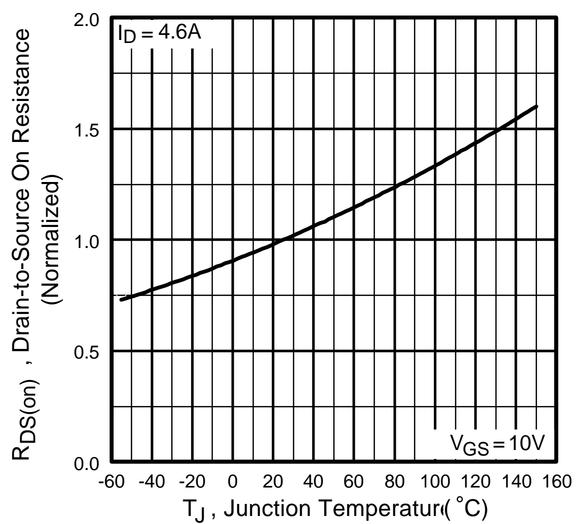

Fig 4. Normalized On-Resistance
Vs. Temperature

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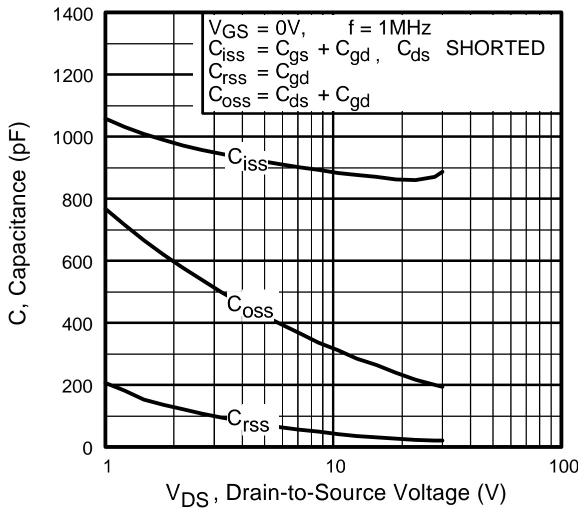

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

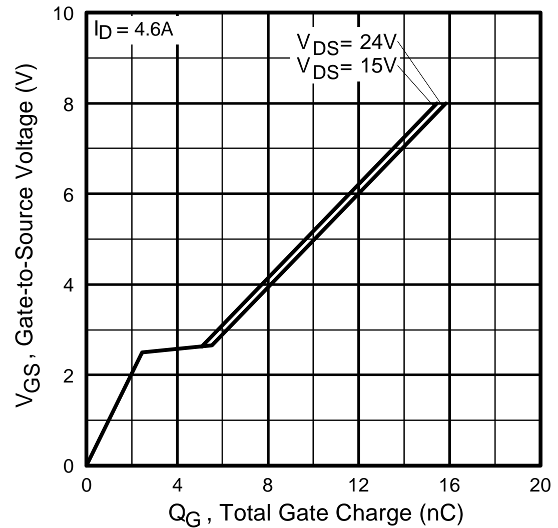

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

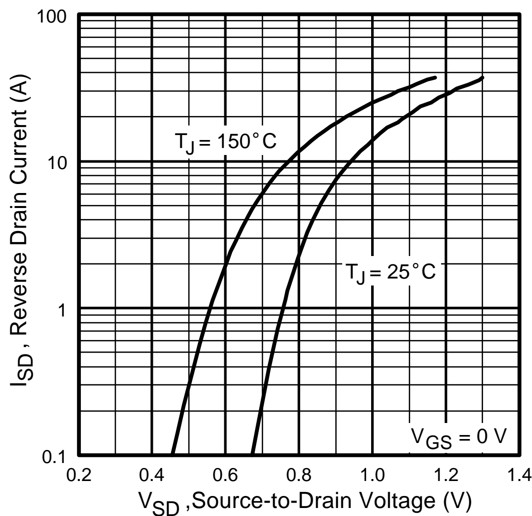

Fig 7. Typical Source-Drain Diode Forward Voltage

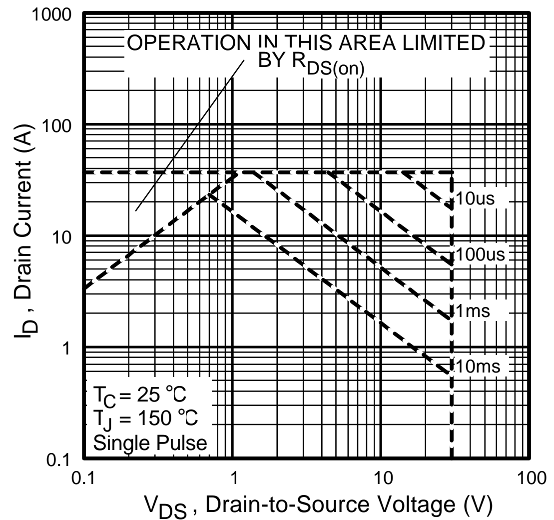

Fig 8. Maximum Safe Operating Area

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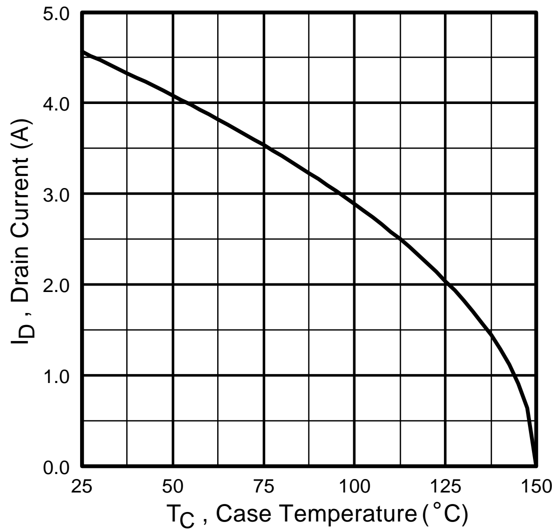

Fig 9. Maximum Drain Current Vs. Case Temperature

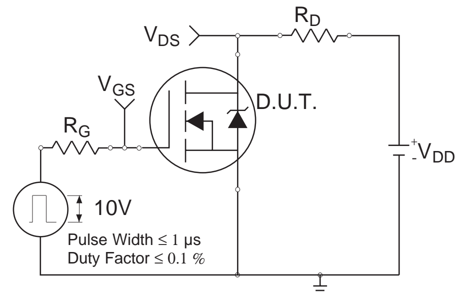

Fig 10a. Switching Time Test Circuit

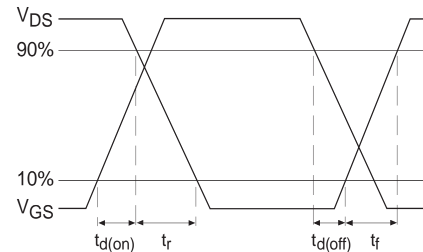

Fig 10b. Switching Time Waveforms

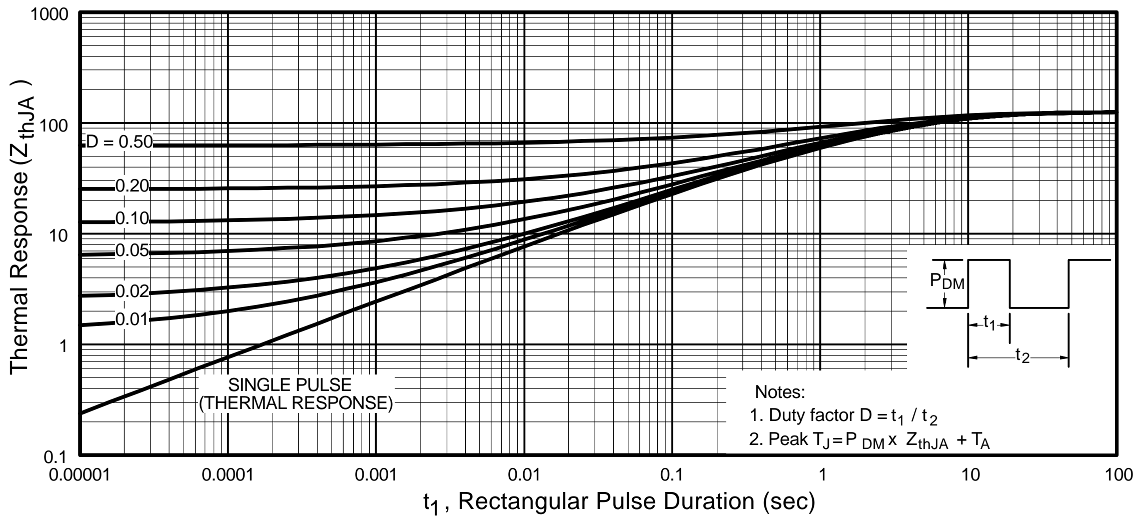

Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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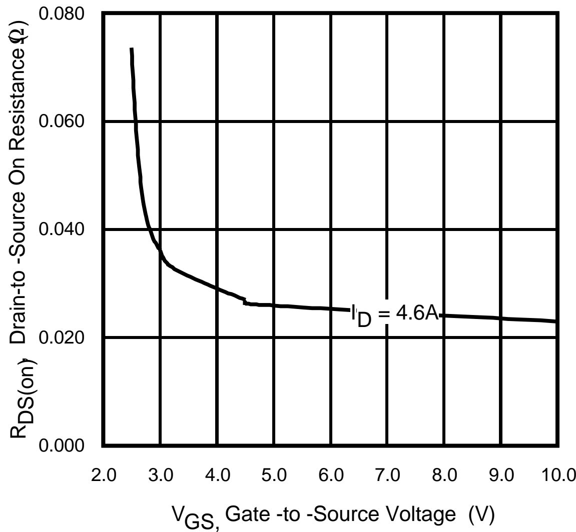

Fig 11. Typical On-Resistance Vs. Gate Voltage

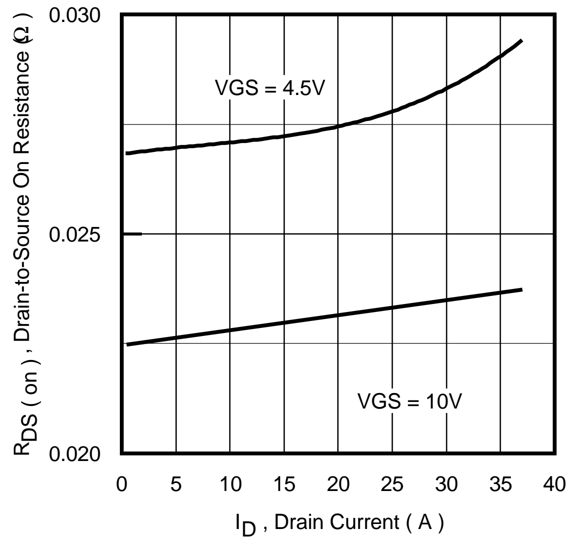

Fig 12. Typical On-Resistance Vs. Drain Current

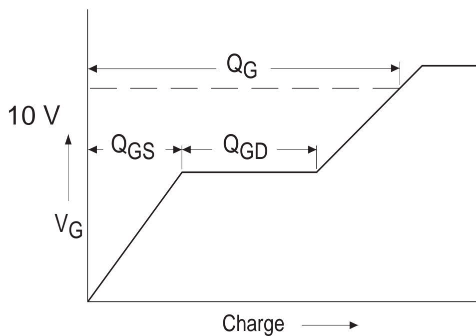

Fig 13a. Basic Gate Charge Waveform

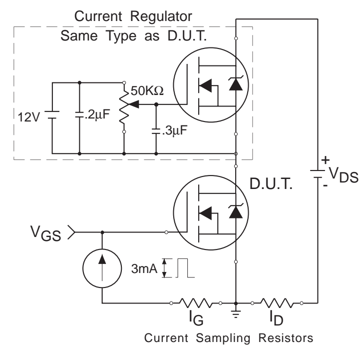

Fig 13b. Gate Charge Test Circuit

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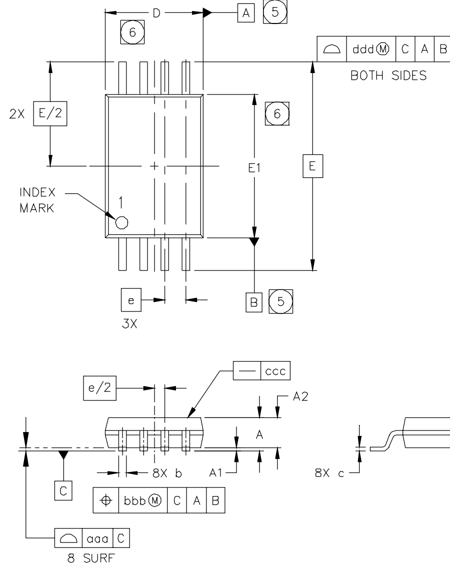
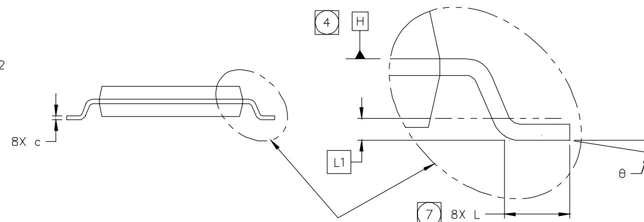
TSSOP-8 Package Outline



SYMBOL	MO-153AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	.0472
A1	0.05	---	0.15	.0020	---	.0059
A2	0.80	1.00	1.05	.032	.039	.041
b	0.19	---	0.30	.0075	---	.0118
c	0.09	---	0.20	.0036	---	.0078
D	2.90	3.00	3.10	.115	.118	.122
E	6.40 BSC			.251 BSC		
E1	4.30	4.40	4.50	.170	.173	.177
e	0.65 BSC			.0256		
L	0.45	0.60	0.75	.0178	.0236	.0290
L1	0.25 BSC			.010 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.0039		
bbb	0.10			.0039		
ccc	0.05			.0019		
ddd	0.20			.0078		



NOTES
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AS SHOWN.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE MO-153AA.

LEAD ASSIGNMENTS

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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