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## NTE5567, NTE5568, NTE5569, & NTE5571 Silicon Controlled Rectifier (SCR) 80 Amp, TO65

**Features:**

- High Current Rating
- Excellent Dynamic Characteristics
- Superior Surge Capabilities
- Standard Package

**Voltage Ratings and Electrical Characteristics:** ( $T_J = +125^{\circ}\text{C}$  unless otherwise specified)

Maximum Repetitive Peak Forward and Reverse Voltage (Note 1), $V_{DRM}$ , $V_{RRM}$	
NTE5567 .....	200V
NTE5568 .....	600V
NTE5569 .....	1200V
NTE5571 .....	1600V
Maximum Non-Repetitive Peak Voltage (Note 2), $V_{RSM}$	
NTE5567 .....	300V
NTE5568 .....	700V
NTE5569 .....	1300V
NTE5571 .....	1700V
Maximum Peak Reverse and Off-State Current, $I_{DRM}$ , $I_{RRM}$ .....	
15mA	
Maximum Average On-State Current (180° Sinusoidal Conduction), $I_{T(RMS)}$	
NTE5567, NTE5568, NTE5569 ( $T_C = +94^{\circ}\text{C}$ ) .....	50A
NTE5571 ( $T_C = +90^{\circ}\text{C}$ ) .....	50A
Maximum RMS On-State Current, $I_{T(RMS)}$ .....	
80A	
Maximum Peak One-Cycle Non-Repetitive Surge Current (t = 10ms, Sinusoidal Half Wave), $I_{TSM}$	
(No Voltage Reapplied)	
NTE5567, NTE5568, NTE5569 .....	1430A
NTE5571 .....	1200A
(100% $V_{RRM}$ Reapplied)	
NTE5567, NTE5568, NTE5569 .....	1200A
NTE5571 .....	1010A
Maximum $I^2t$ for Fusing (t = 10ms, Sinusoidal Half Wave), $I^2t$	
(No Voltage Reapplied)	
NTE5567, NTE5568, NTE5569 .....	10.18KA <sup>2</sup> s
NTE5571 .....	7.21KA <sup>2</sup> s
(100% $V_{RRM}$ Reapplied)	
NTE5567, NTE5568, NTE5569 .....	7.20KA <sup>2</sup> s
NTE5571 .....	5.10KA <sup>2</sup> s

**Voltage Ratings and Electrical Characteristics (Cont'd):** ( $T_J = +125^\circ\text{C}$  unless otherwise specified)

Maximum $I^2\sqrt{t}$ for Fusing ( $t = 0.1$ to $10\text{ms}$ , No Voltage Reapplied), $I^2\sqrt{t}$	
NTE5567, NTE5568, NTE5569	101.8KA <sup>2</sup> √s
NTE5571	72.1KA <sup>2</sup> √s
Low Level Value of Threshold Voltage ( $16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $V_{T(TO)1}$	
NTE5567, NTE5568, NTE5569	0.94V
NTE5571	1.02V
High Level Value of Threshold Voltage ( $\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)}$ ), $V_{T(TO)2}$	
NTE5567, NTE5568, NTE5569	1.08V
NTE5571	1.17V
Low Level Value of On–State Slope Resistance ( $16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $r_{t1}$	
NTE5567, NTE5568, NTE5569	4.08mΩ
NTE5571	4.78mΩ
High Level Value of On–State Slope Resistance ( $\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)}$ ), $V_{T(TO)2}$	
NTE5567, NTE5568, NTE5569	3.34mΩ
NTE5571	3.97mΩ
Maximum On–State Voltage ( $I_{pk} = 157\text{A}$ , $T_J = +25^\circ\text{C}$ ), $V_{TM}$	
NTE5567, NTE5568, NTE5569	1.60V
NTE5571	1.78V
Maximum Holding Current ( $T_J = +25^\circ\text{C}$ , Anode Supply 22V, Resistive Load, Initial $I_T = 2\text{A}$ ), $I_H$	200mA
Latching Current (Anode Supply 6V, Resistive Load), $I_L$	400mA
Maximum Rate of Rise of Turned–On Current, $di/dt$	
( $V_{DM} = \text{Rated } V_{DRM}$ , Gate Pulse = 20V, 15Ω, $t_p = 6\mu\text{s}$ , $t_r = 0.1\mu\text{s}$ ax., $I_{TM} = (2 \times \text{Rated } di/dt) \text{ A}$ )	
NTE5567, NTE5568	200A/μs
NTE5569, NTE5571	100A/μs
Typical Delay Time, $t_d$	0.9μs
( $T_C = +25^\circ\text{C}$ , $V_{DM} = \text{Rated } V_{DRM}$ , DC Resistive Circuit, Gate Pulse = 10V, 15Ω Source, $t_p = 20\mu\text{s}$ )	
Typical Turn–Off Time, $t_q$	110μs
( $T_C = +125^\circ\text{C}$ , $I_{TM} = 50\text{A}$ , Reapplied $dv/dt = 20\text{V}/\mu\text{s}$ , $dir/dt = -10\text{A}/\mu\text{s}$ , $V_R = 50\text{V}$ )	
Maximum Critical Rate of Rise of Off–State Voltage, $dv/dt$	
(Linear to 100% rated $V_{DRM}$ )	200V/μs
(Linear to 67% rated $V_{DRM}$ )	500V/μs
Maximum Peak Gate Power ( $t_p \leq 5\text{ms}$ ), $P_{G(AV)}$	10W
Maximum Average Gate Power, $P_{GM}$	2.5W
Maximum Peak Positive Gate Current, $I_{GM}$	2.5A
Maximum Peak Positive Gate Voltage, $+V_{GM}$	20V
Maximum Peak Negative Gate Voltage, $-V_{GM}$	10V
DC Gate Current Required to Trigger (6V Anode–to–Cathode Applied), $I_{GT}$	50mA
DC Gate Voltage Required to Trigger (6V Anode–to–Cathode Applied, $T_J = +25^\circ\text{C}$ ), $V_{GT}$	2.5V
DC Gate Current Not to Trigger (Rated $V_{DRM}$ Anode–to–Cathode Applied), $I_{GD}$	5.0mA
DC Gate Voltage Not to Trigger (Rated $V_{DRM}$ Anode–to–Cathode Applied), $V_{GD}$	0.2V
Operating Junction Temperature Range, $T_J$	$-40^\circ$ to $+125^\circ\text{C}$
Storage Temperature Range, $T_{stg}$	$-40^\circ$ to $+125^\circ\text{C}$
Thermal Resistance	
Junction–to–Case (DC Operation), $R_{thJC}$	0.35K/W
Case–to–Heatsink (Mounting Surface Smooth, Flat, and Greased), $R_{thCS}$	0.25K/W
Mounting Torque (Non–Lubricated Threads), $T$	25 – 30 (2.8 – 3.4) lbf–in (Nm)

Note 1. Units may be broken over non–repetitively in the off–state direction without damage, if  $di/dt$  does not exceed 20A/μs.

Note 2. For voltage pulses with  $t_p \leq 5\text{ms}$ .

