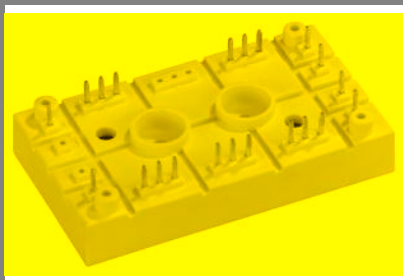


SKDT 115



SEMIPONT™ 5

Bridge Rectifier

SKDT 115

Target Data

Features

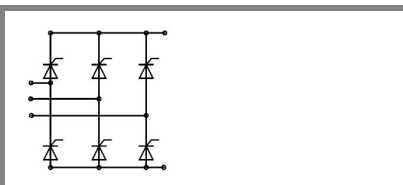
- Compact design
- Two screws mounting
- Heat transfer and isolation through direct copper board (low R_{th})
- Low resistance in steady-state and high reliability
- High surge currents
- Glass passivated thyristor chips
- Up to 1600 V reverse voltage
- UL -recognized, file no. E 63 532

Typical Applications*

- DC and AC drives
- Controlled field rectifier for DC motors
- Controlled battery charger

V_{RSM} V	V_{RRM}, V_{DRM} V	$I_D = 110$ A (full conduction) ($T_s = 80$ °C)
1300	1200	SKDT 115/12
1700	1600	SKDT 115/16

Symbol	Conditions	Values	Units
I_D	$T_s = 80$ °C	110	A
I_{TSM}, I_{FSM}	$T_{vj} = 25$ °C; 10 ms $T_{vj} = 125$ °C; 10 ms	1050 950	A
i^2t	$T_{vj} = 25$ °C; 8,3 ... 10 ms $T_{vj} = 125$ °C; 8,3 ... 10 ms	5500 4500	A ² s A ² s
V_T, V_F	$T_{vj} = 25$ °C; $I_T, I_F = 120$ A	max. 1,8	V
$V_{T(TO)}$	$T_{vj} = 125$ °C;	max. 1,1	V
r_T	$T_{vj} = 125$ °C	max. 6	mΩ
I_{DD}, I_{RD}	$T_{vj} = 125$ °C; $V_{DD} = V_{DRM}, V_{RD} = V_{RRM}$	max. 20	mA
t_{gd}	$T_{vj} = 25$ °C; $I_G = A; di_G/dt = A/\mu s$		μs
t_{gr}	$V_D = \cdot V_{DRM}$		μs
$(dv/dt)_{cr}$	$T_{vj} = 125$ °C	max. 500	V/μs
$(di/dt)_{cr}$	$T_{vj} = 125$ °C; $f = 50...60$ Hz	max. 50	A/μs
t_q	$T_{vj} = 125$ °C; typ.	150	μs
I_H	$T_{vj} = 25$ °C; typ. / max.	- / 200	mA
I_L	$T_{vj} = 25$ °C; $R_G = 33$ Ω	- / 400	mA
V_{GT}	$T_{vj} = 25$ °C; d.c.	min. 3	V
I_{GT}	$T_{vj} = 25$ °C; d.c.	min. 150	mA
V_{GD}	$T_{vj} = 125$ °C; d.c.	max. 0,25	V
I_{GD}	$T_{vj} = 125$ °C; d.c.	max. 5	mA
$R_{th(j-s)}$	per thyristor	0,84	K/W K/W K/W
T_{vj}		- 40 ... + 125	°C
T_{stg}		- 40 ... + 125	°C
T_{solder}	terminals	260	°C
V_{isol}	a. c. 50 Hz; r.m.s.; 1 s / 1 min.	3600 (3000)	V
M_s	to heatsink	2,5	Nm
M_t			Nm
m	approx.	75	g
Case		G 58	



SKDT

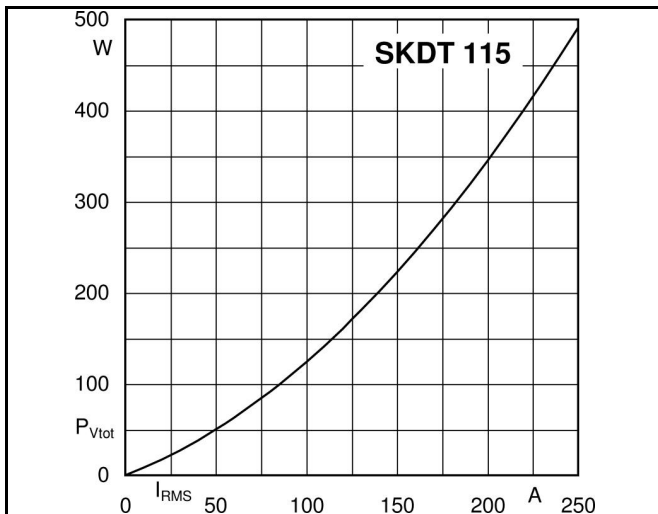


Fig. 1 Power dissipation vs. r.m.s. current

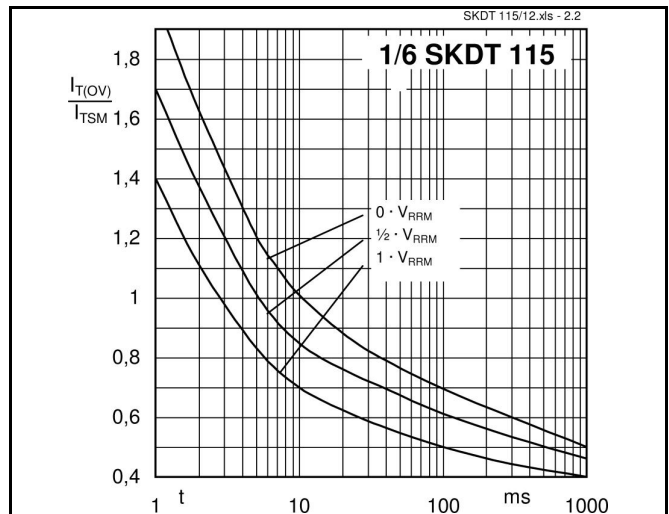


Fig. 2 Surge overload current vs. time

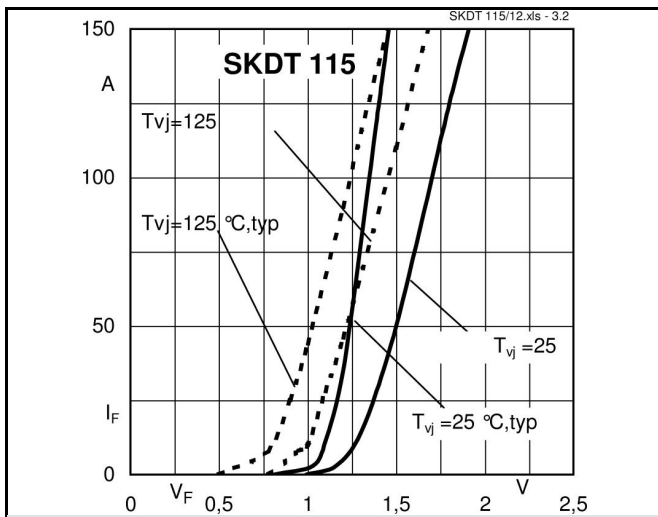


Fig. 3 Single thyristor on-state characteristic

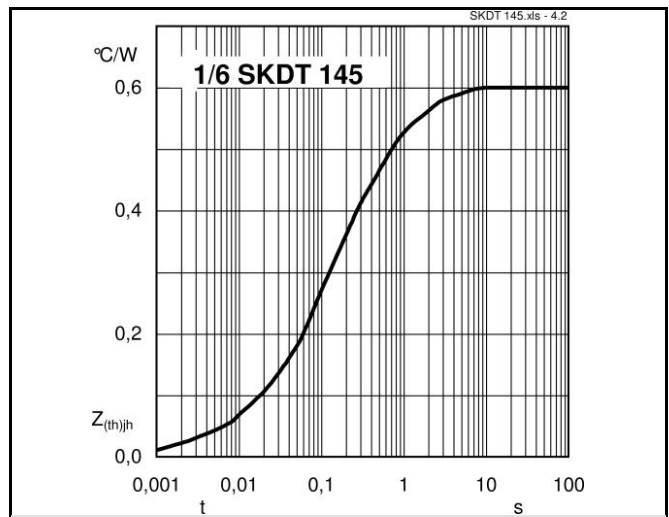


Fig. 4 Transient thermal impedance vs. time

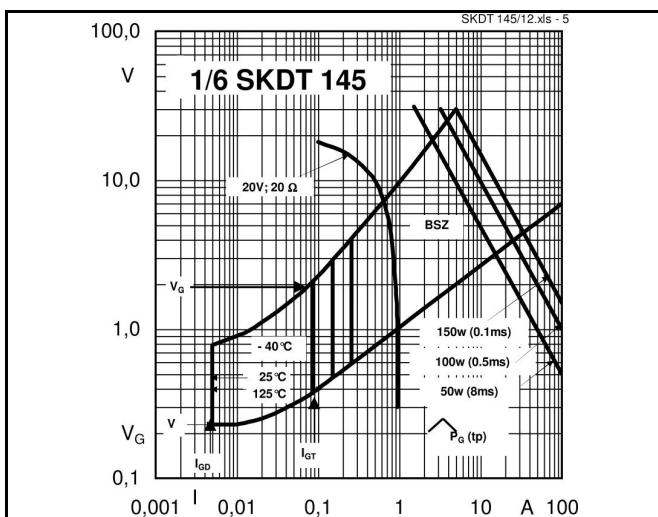


Fig. 5 Gate trigger characteristic

