DUAL SYNCHRONOUS PWM CONTROLLER WITH CURRENT SHARING CIRCUITRY AND LDO CONTROLLER

FEATURES

- Dual Synchronous Controller in 24-Pin Package with 180° out-of-phase operation
- LDO Controller with Independent Bias Supply
- Can be configured as 2-Independent or 2-Phase PWM Controller
- Programmable Current Sharing in 2-Phase Configuration
- Flexible, Same or Separate Supply Operation
- Operation from 4V to 25V Input
- Programmable Switching Frequency up to 400KHz
- Soft-Start controls all outputs
- Precision Reference Voltage Available
- 500mA Peak Output Drive Capability
- Short Circuit Protection for all outputs
- Power Good Output
- Synchronizable with External Clock
- RoHS Compliant

DESCRIPTION

The APU3046 IC combines a Dual synchronous Buck controller and a linear regulator controller, providing a cost-effective, high performance and flexible solution for multi-output applications. The Dual synchronous controller can be configured as 2-independent or 2-phase controller. In 2-phase configuration, the APU3046 provides a programmable current sharing which is ideal when the output power exceeds any single input power budget. APU3046 provides a separate adjustable output by driving a switch as a linear regulator. This device features programmable switching frequency up to 400KHz per phase, under-voltage lockout for all input supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

APPLICATIONS

- Dual-Phase Power Supply
- DDR Memory Source Sink Vtt Application
- Graphic Card
- Hard Disk Drive
- Power supplies requiring multiple outputs

TYPICAL APPLICATION

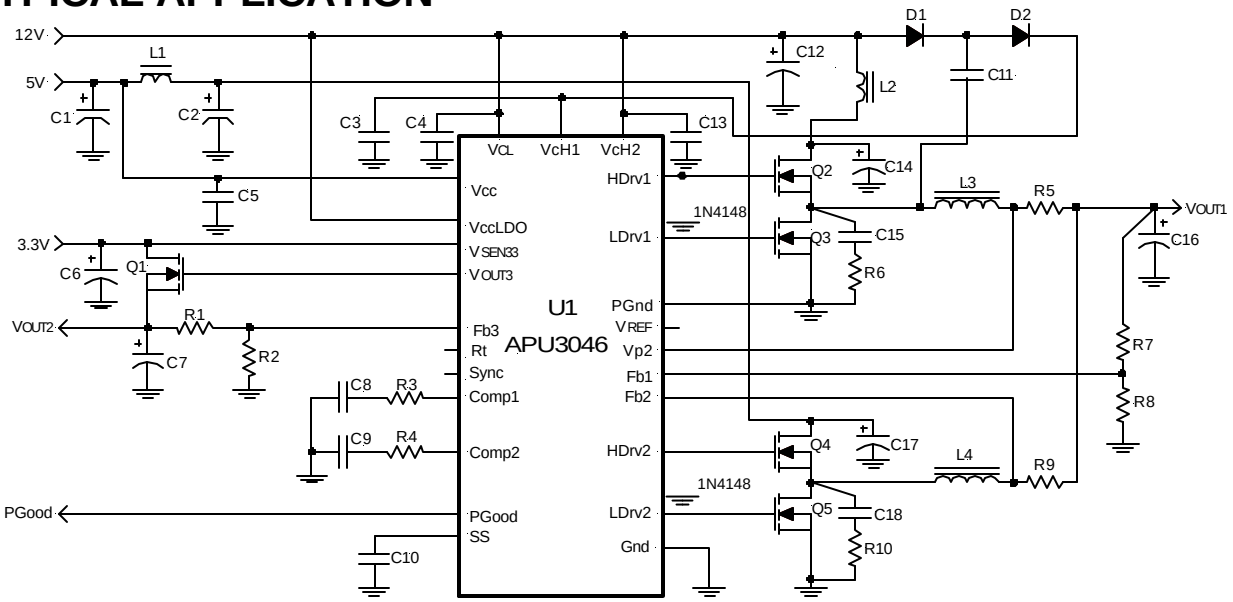


Figure 1 - Typical application of APU3046 configured as 2-phase converter with current sharing.

PACKAGE ORDER INFORMATION

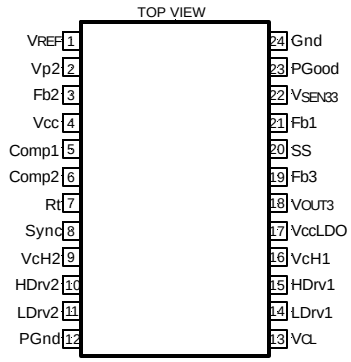
T_A (°C)	DEVICE	PACKAGE	FREQUENCY
0 To 70	APU3046O	24-Pin Plastic TSSOP (O)	200-400KHz

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
VccLDO, VcH1, VcH2 and V_{CL} Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

24-PIN PLASTIC TSSOP (O)



θ_{JA} = 84°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcH1=VcH2=V_{CL}=VccLDO=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage Section						
Fb Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2		%
UVLO Section						
UVLO Threshold - Vcc	$UVLO_{Vcc}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VccLDO	$UVLO_{VccLDO}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - VccLDO				0.25		V
UVLO Threshold - VcH1	$UVLO_{VcH1}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH1				0.2		V
UVLO Threshold - VcH2	$UVLO_{VcH2}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH2				0.2		V
UVLO Threshold - Fb	UVLOFb	Fb Ramping Down		0.6		V
UVLO Hysteresis - Fb				0.1		V
UVLO Threshold - V_{SEN33}	$UVLO_{VSEN33}$	Supply Ramping Up		2.5		V
UVLO Hysteresis - V_{SEN33}				0.2		V
Supply Current Section						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		5		mA
VcH1 Dynamic Supply Current	Dyn I_{cH1}	Freq=200KHz, C_L=1500pF		7		mA
VcH2 Dynamic Supply Current	Dyn I_{cH2}	Freq=200KHz, C_L=1500pF		7		mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		3.5		mA
VcH1 Static Supply Current	I_{cH1Q}	SS=0V		2		mA
VcH2 Static Supply Current	I_{cH2Q}	SS=0V		2		mA
VccLDO Static Supply Current	I_{cLDO}	SS=0V		1		mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	15	25	30	μA
Power Good Section						
Fb1 Lower Trip Point	PG_{FB1L}	Fb1 Ramping Down		$0.9V_{REF}$		V
Fb1 Upper Trip Point	PG_{FB1H}	Fb1 Ramping Up		$1.1V_{REF}$		V
Fb2 Lower Trip Point	PG_{FB2L}	Fb2 Ramping Down		$0.9V_{REF}$		V
Fb2 Upper Trip Point	PG_{FB2H}	Fb2 Ramping Up		$1.1V_{REF}$		V
Fb3 Lower Trip Point	PG_{FB3L}	Fb3 Ramping Down		$0.9V_{REF}$		V
Fb3 Upper Trip Point	PG_{FB3H}	Fb3 Ramping Up		$1.1V_{REF}$		V
Power Good Voltage OK	V_{PG}	5K resistor pulled up to 5V	4.5	4.8	5	V
Error Amp Section						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V		-0.1		μA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V		-64		μA
Transconductance 1	g_{m1}			400		μmho
Transconductance 2	g_{m2}			600		μmho
Input Offset Voltage for PWM2	$V_{OS(ERR)2}$	Fb2 to V_{P2}	-2	0	+2	mV
Oscillator Section						
Frequency	Freq	Rt=Open Rt=Gnd	180 300	200 350	220 450	KHz
Ramp Amplitude	V_{RAMP}			1.25		V
Output Drivers Section						
Rise Time	Tr	C_L=1500pF		35	100	ns
Fall Time	Tf	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90		%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%
LDO Controller Section						
Drive Current	I_{LDO}		30	45		mA
Fb Voltage	V_{FB}LDO		1.225	1.25	1.275	V
Input Bias Current	$I_{LDO(BIAS)}$			0.5	2	μA

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V_{REF}	Reference Voltage.
2	Vp2	Non-inverting input to the second error amplifier. In the current sharing mode, it is connected to the programming resistor. In independent 2-channel mode it is connected to V_{REF} pin when Fb2 is connected to the resistor divider to set the output voltage.
3 21	Fb2 Fb1	Inverting inputs to the error amplifiers. In current sharing mode, Fb1 is connected to a resistor divider to set the output voltage and Fb2 is connected to programming resistor to achieve current sharing. In independent 2-channel mode, these pins work as feedback inputs for each channel.
4	Vcc	Supply voltage for the internal blocks of the IC.
5,6	Comp1, Comp2	Compensation pins for the error amplifiers.
7	Rt	The switching frequency can be programmed between 200KHz and 400KHz by connecting a resistor between Rt and Gnd. By floating the pin, the switching frequency will be 200KHz and by grounding the pin, the switching frequency will be 400KHz.
8	Sync	The internal oscillator may be synchronized to an external clock via this pin.
9 16	VcH2 VcH1	Supply voltage for the high side output drivers. These are connected to voltages that must be at least 4V higher than their bus voltages (assuming 5V threshold MOSFET). A minimum of 1μF, high frequency capacitor must be connected from these pins to PGnd to provide peak drive current capability.

PIN#	PIN SYMBOL	PIN DESCRIPTION
10,15	HDrv2, HDrv1	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from these pins to ground for the application when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load.
11,14	LDrv2, LDrv1	Output driver for the synchronous power MOSFET.
12	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to the system's ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from Vcc, V_{CL}, VcH1 and VcH2 pins to this pin for noise free operation.
13	V_{CL}	Supply voltage for the low side output drivers.
17	VccLDO	Separate input supply for LDO controller.
18	V_{OUT3}	Driver signal for the LDO's external transistor.
19	Fb3	LDO's feedback pin, connected to a resistor divider to set the output voltage of LDO.
20	SS	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.
22	V_{SEN33}	Sense the LDO input voltage for UVLO.
23	PGood	Power good pin. This pin is a collector output that switches Low when any of the outputs are outside of the specified under voltage trip point.
24	Gnd	Analog ground for internal reference and control circuitry. Connect to PGnd with a short trace.

BLOCK DIAGRAM

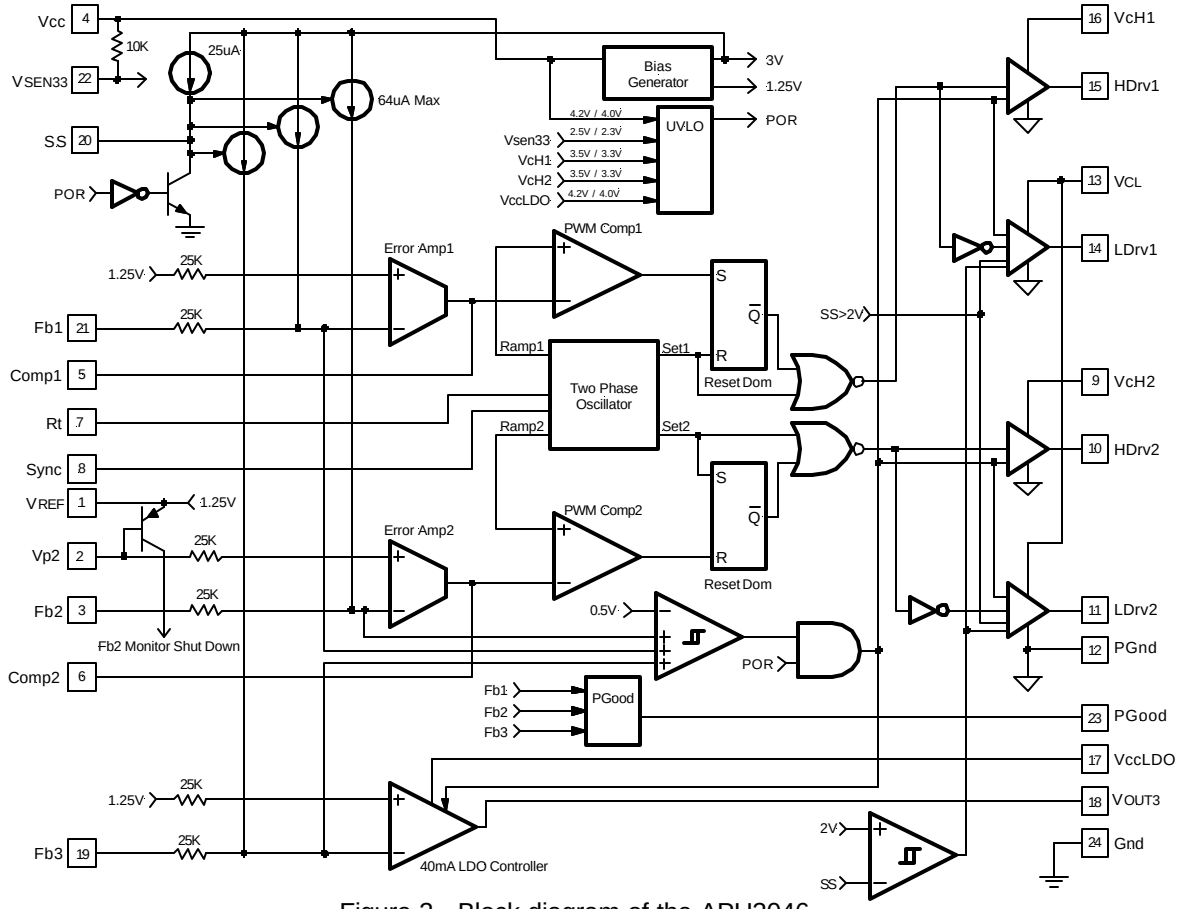


Figure 2 - Block diagram of the APU3046.

THEORY OF OPERATION

Introduction

The APU3046 is designed for multi-outputs applications. It includes two synchronous buck controllers and a linear regulator controller. The two synchronous controller operates with fixed frequency voltage mode and can be configured as two independent controller or 2-phase controller with current sharing. The timing of the IC is provided through an internal oscillator circuit. These are two out of phase oscillators and can be programmed by using an external resistor from 200KHz to 400KHz per phase. Figure 11 shows switching frequency versus external resistor.

Independent Mode

In this mode the APU3046 provides two independent outputs with either common or different input voltages. The output voltage of the individual channel is set and controlled by the output of the error amplifier, this is the amplified error signal from the sensed output voltage and the reference voltage. This voltage is compared to the ramp signal and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

Current Sharing Mode

In the current sharing mode, the two converter's outputs tied together and provide one single output (see Figure 1). In this mode, one control loop acts as a master and sets the output voltage as a regular Voltage Mode buck controller and the other control loop acts as a slave and monitors the current information for current sharing. The current sharing is programmable and sets by using two external resistors in output currents' path. The slave's error amplifier, error amplifier 2 (see Block Diagram) measures the voltage drops across the current sense resistors, the differential of these signals is amplified and compared with the ramp signal and generate the fixed frequency pulses of variable duty cycle to match the output currents.

Out of Phase Operation

The APU3046 drives its two output stages 180^{o} out of phase. In 2-phase configuration, the two inductor ripple currents cancel each other and result to a reduction of the output current ripple and contribute to a smaller output capacitor for the same ripple voltage requirement.

In application with single input voltage, the 2-phase configuration reduces the input ripple current. This results in much smaller RMS current in the input capacitor and reduction of input capacitor.

Soft-Start

The APU3046 has a programmable soft start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1, VcH2, VccLDO and $V_{SEN}33$ rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.5V. This can be easily done by using an external small signal transistor. During shutdown the MOSFET drivers and the LDO controller turn off.

Power Good

The APU3046 provides a power good signal. This is an open collector output and it is pulled low if the output voltages are not within the specified threshold. This pin can be left floating if not used.

Short-Circuit Protection

The outputs are protected against the short circuit. The APU3046 protects the circuit for shorted output by sensing the output voltages. The APU3046 shuts down the PWM signals and LDO controller, when the output voltages drops below the set values.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs and LDO controller remain in the off state whenever the supply voltages drop below set parameters. Normal operation resumes once the supply voltages rise above the set values.

Frequency Synchronization

The APU3046 can be synchronized with an external clock signal. The synchronizing pulses must have a minimum pulse width of 100ns. If the sync function is not used, the Sync pin can be either connected to ground or be floating.

APPLICATION INFORMATION

Design Example:

The following example is a typical application for APU3046 in current sharing mode. The schematic is Figure 13 on page 15.

For Switcher:	For Linear Regulator:
$V_{IN1(MASTER)}$ = 5V	V_{IN3} = 3.3V
$V_{IN2(SLAVE)}$ = 12V	V_{OUT2} = 2.5V
V_{OUT1} = 1.5V	I_{OUT2} = 2A
I_{OUT} = 16A	
ΔV_{OUT} = 75mV	
f_S = 200KHz	

PWM Section

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb1 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT1} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 3.

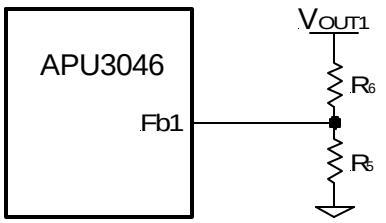


Figure 3 - Typical application of the APU3046 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

This will result to:

V_{OUT1} = 1.5V, V_{REF} = 1.25V, R_5 = 1K, R_6 = 200Ω

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:

C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Boost Supply

To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 1. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

Sense Resistor Selection

These resistors will determine the current sharing between two channels. The relationship between the Master and Slave output currents is expressed by:

$$R_{SEN1} \times I_{MASTER} = R_{SEN2} \times I_{SLAVE} \qquad ---(3)$$

For an equal current sharing, R_{SEN1}=R_{SEN1}

Choose R_{SEN1}=R_{SEN2}=5mΩ

Input Capacitor selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1\text{-}D)} \qquad ---(4)$$

Where:

D is the Duty Cycle, simply D=V_{OUT}/V_{IN}.

I_{RMS} is the RMS value of the input capacitor current.

I_{OUT} is the output current for each channel.

For V_{IN1}=5V, I_{OUT1}=8A and D1=0.3

Results to: I_{RMS1}=3.6A

And for V_{IN2}=12V, I_{OUT2}=8A and D2=0.125

Results to: I_{RMS2}=2.6A

For higher efficiency, a low ESR capacitor is recommended.

For V_{IN1}=5V, choose two Poscap from Sanyo 6TPB330M (6.3V, 330μF, 40mΩ, 3A)

For V_{IN2}=12V, choose two 16TPB47M (16V, 47μF, 70mΩ, 1.4A).

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \qquad ---(5)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=75mV and ΔI_O=10A, result to ESR=7.5mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting six of these capacitors in parallel, results to an ESR of ≅ 7mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

The resulting output ripple current is smaller then each channel ripple current due to the 180° phase shift. These currents cancel each other. The cancellation is not the maximum because of the different duty cycle for each channel.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi); the optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(6)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

For Δi_1=30% of I_1, we get: L_1=2.18μH
For Δi_2=30% of I_2, we get: L_2=2.7μH

The Coilcraft DO5022HC series provides a range of inductors in different values and low profile for large currents.
For L_1 choose: DO5022P-222HC (2.2μH,12A)
For L_2 choose: DO5022P-332HC (3.3μH,10A)

Power MOSFET Selection

The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The total conduction loss is defined as:

$$P_{CON(TOTAL)} = P_{CON}\text{(Upper Switch)}\vartheta + P_{CON}\text{(Lower Switch)}\vartheta$$

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7460 for control MOSFET and IRF7457 for synchronous MOSFET. These devices provide low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7460	IRF7457
V_{DSS} = 20V	V_{DSS} = 20V
I_D = 10A @ 75°C	I_D = 12A @ 70°C
$R_{DS(ON)}$ = 10mΩ @ V_{GS}=10V	$R_{DS(ON)}$ = 7.5mΩ @ V_{GS}=10V
ϑ = 1.8 for 150°C (Junction Temperature)	ϑ = 1.5 for 150°C (Junction Temperature)

The total conduction losses for the master channel is:

$P_{CON(MASTER)}$ = 0.85W

The total conduction losses for the slave channel is:

$P_{CON(SLAVE)}$ = 0.77W

The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero-voltage condition, therefore the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(7)$$

Where:

$V_{DS(OFF)}$ = Drain to Source Voltage at off time

t_r = Rise Time

t_f = Fall Time

T = Switching Period

I_{LOAD} = Load Current

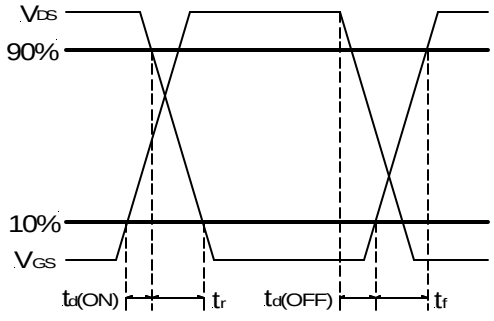


Figure 4 - Switching time waveforms.

From IRF7460 data sheet we obtain:

IRF7460

t_r = 6.9ns

t_f = 4.3ns

These values are taken under a certain condition test. For more detail please refer to the IRF7460 and IRF7457 data sheets.

By using equation (7), we can calculate the switching losses.

$P_{SW(MASTER)}$ = 44.8mW

$P_{SW(SLAVE)}$ = 107.5mW

Feedback Compensation

The control scheme for master and slave channels is based on voltage mode control, but the compensation of these two feedback loops is slightly different.

The Master channel sets the output voltage and its feedback loop should take care of double pole introduced by the output filter as a regular voltage mode control loop. The goal is to provide a close loop transfer function with the highest 0dB crossing frequency and adequate phase margin. The slave feedback loop acts slightly different and its goal is using the current information for current sharing.

The master feedback loop sees the output filter. The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The resonant frequency of the LC filter expressed as follows:

$$F_{LC(MASTER)} = \frac{1}{2\pi\sqrt{Lo \times Co}} \qquad ---(8)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

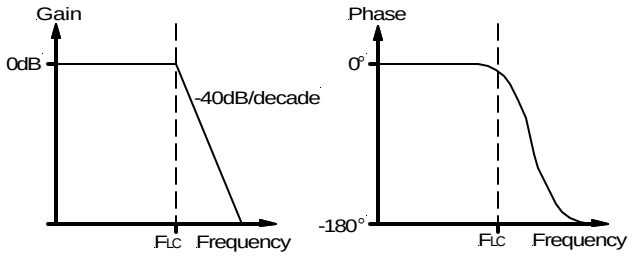


Figure 5 - Gain and phase of LC filter.

The master error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp1 pin to ground as shown in Figure 6.

The ESR zero of the LC filter expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(9)$$

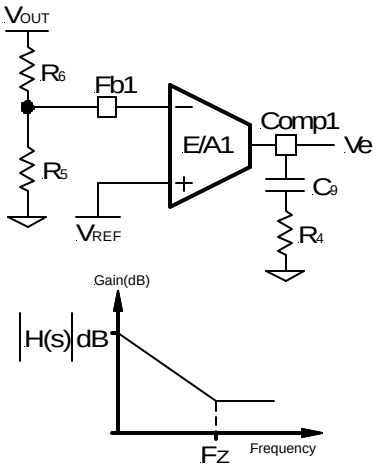


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5} \right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(10)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(11)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(12)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$F_{O1} > F_{ESR}$ and $F_{O1} \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN(MASTER)}} \times \frac{F_{O1} \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{gm} \qquad ---(13)$$

Where:
$V_{IN(MASTER)}$ = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
F_{O1} = Crossover Frequency for the master E/A
F_{ESR} = Zero Frequency of the Output Capacitor
$F_{LC(MASTER)}$ = Resonant Frequency of Output Filter
gm = Error Amplifier Transconductor
R_5 and R_6 = Resistor Dividers for Output Voltage Programming

For:
$V_{IN(MASTER)}$ = 5V
V_{OSC} = 1.25V
F_{O1} = 30KHz
F_{ESR} = 25.26KHz
$F_{LC(MASTER)}$ = 3.57KHz
R_5 = 1K
R_6 = 200Ω
gm = 600μmho

This results to: R_4=29.7KΩ. Choose: R_4=29.4KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC(MASTER)}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi \sqrt{L_O \times C_O}} \qquad ---(14)$$

For:
Lo = 2.2μH
Co = 900μF
Fz = 2.67KHz
R_4 = 24.9KΩ

Using equations (12) and (14) to calculate C_9, we get:

C_9 = 2003pF
Choose: C_9 = 2200pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

For $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

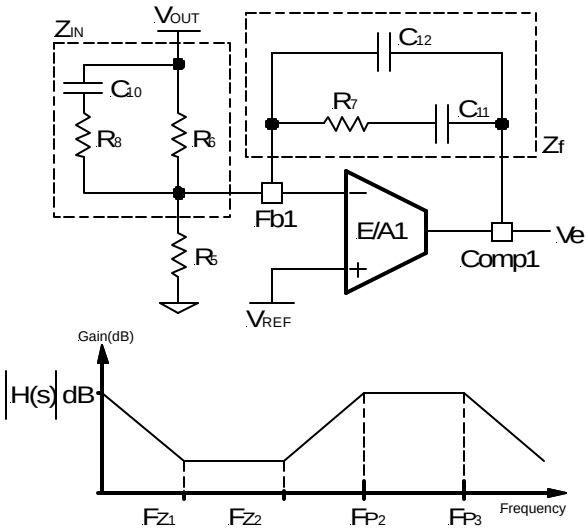


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(15)}$$

By replacing Z_{IN} and Z_f according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_{O1} = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(16)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (15) regarding transconductance error amplifier.

1) Select the crossover frequency:

   $F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.

   $F_{Z1} \cong 75\% F_{LC}$

   $$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

C_{12} > 50pF
If not, change R_7 selection.

5) Place R_7 in (16) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times F_O \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C10 \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C10 \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

The slave error amplifier is a differential-input transconductance amplifier as well, the main goal for the slave feed back loop is to control the inductor current to match the masters inductor current as well provides highest bandwidth and adequate phase margin for overall stability.

The transfer function of power stage is expressed by:

$$G(s) = \frac{I_{L2}(s)}{Ve(s)} = \frac{V_{IN} - V_{OUT}}{sL_2 \times V_{OSC}} \quad ---(17)$$

Where:
V_{IN} = Input Voltage
V_{OUT} = Output Voltage
L_2 = Output Inductor
V_{OSC} = Oscillator Peak Voltage

As shown the transfer function is a function of inductor current.

The transfer function for the compensation network is given by equation (18), when using a series RC circuit as shown in Figure 8:

$$D(s) = \frac{Ve(s)}{R_{S2} \times I_{L2}(s)} = \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1 + sC_2R_2}{sC_2}\right) \quad ---(18)$$

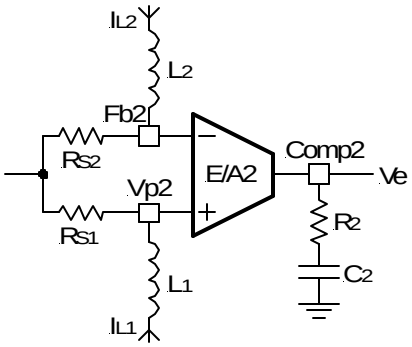


Figure 8 - The PI compensation network for slave channel.

The loop gain function is:

$H(s)=[G(s) \times D(s) \times R_{S2}]$

$$H(s)=R_{S2} \times \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1+sR_2C_2}{sC_2}\right) \times \left(\frac{V_{IN}-V_{OUT}}{sL_2 \times V_{OSC}}\right)$$

Select a zero crossover frequency (F_{O2}) one-tenth of the switching frequency:

$$F_{O2} = \frac{f_S}{10}$$

F_{O2} = 20KHz

$$H(Fo) = g_m \times R_{S1} \times R_2 \times \frac{V_{IN} - V_{OUT}}{2\pi \times Fo \times L_2 \times V_{OSC}} = 1 \quad ---(19)$$

From (18), R_2 can be express as:

$$R_2 = \frac{1}{g_m \times R_{S1}} \times \frac{2\pi \times F_{O2} \times L_2 \times V_{OSC}}{V_{IN(SLAVE)} - V_{OUT}} \quad ---(20)$$

Set the zero of compensator to be half of $F_{LC(SLAVE)}$, the compensator capacitor, C_2, can be calculated as:

$$F_{LC(SLAVE)} = \frac{1}{2\pi \sqrt{L_2 \times C_{OUT}}}$$

$$Fz = \frac{F_{LC(SLAVE)}}{2}$$

$$C_2 = \frac{1}{2\pi \times R_2 \times Fz} \quad ---(21)$$

Using equations (20) and (21) we get the following values for R_2 and C_2.

R_2=16.45K; Choose: R_2=16.5K

C_2=6606pF; Choose: C_2=6800pF

LDO Section

Output Voltage Programming

Output voltage for LDO is programmed by reference voltage and external voltage divider. The Fb3 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb3 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT2} = V_{REF} \times \left(1 + \frac{R_7}{R_{10}}\right)$$

For:
V_{OUT2} = 2.5V
V_{REF} = 1.25V
R_{10} = 1KΩ

Results to R_7=1KΩ

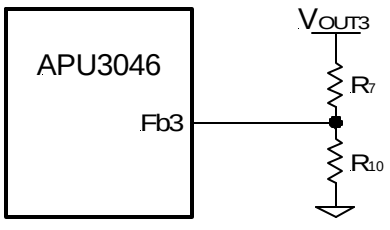


Figure 9 - Programming the output voltage for LDO.

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulator is to select the maximum $R_{DS(ON)}$ based on the input to the dropout voltage and the maximum load current.

$$R_{DS(ON)} = \frac{V_{IN3} - V_{OUT2}}{I_{OUT2}}$$

For:
V_{IN3} = 3.3V
V_{OUT2} = 2.5V
I_{OUT2} = 2A

Results to: $R_{DS(ON)(MAX)}$ = 0.4Ω

Note that since the MOSFET $R_{DS(ON)}$ increases with temperature, this number must be divided by ~1.5 in order to find the $R_{DS(ON)(MAX)}$ at room temperature. The IRLR2703 has a maximum of 0.065Ω $R_{DS(ON)}$ at room temperature, which meets our requirements.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

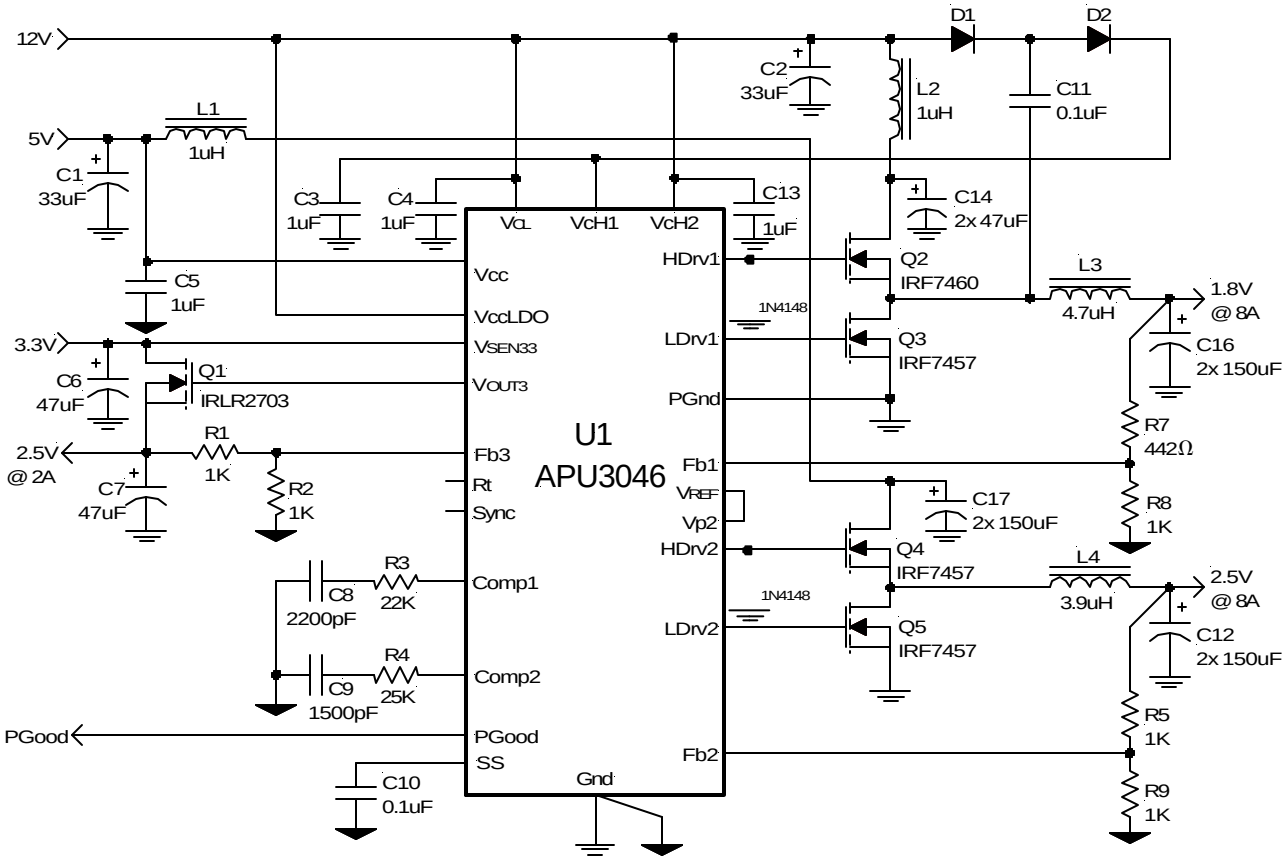


Figure 10 - Typical application for APU3046 configured as two independent controllers.

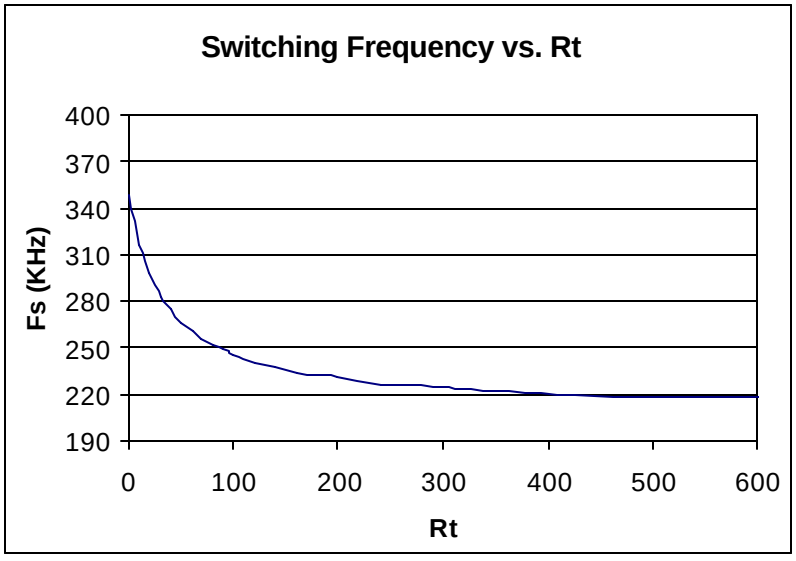


Figure 11 - Switching frequency per phase vs. Rt

TYPICAL APPLICATION

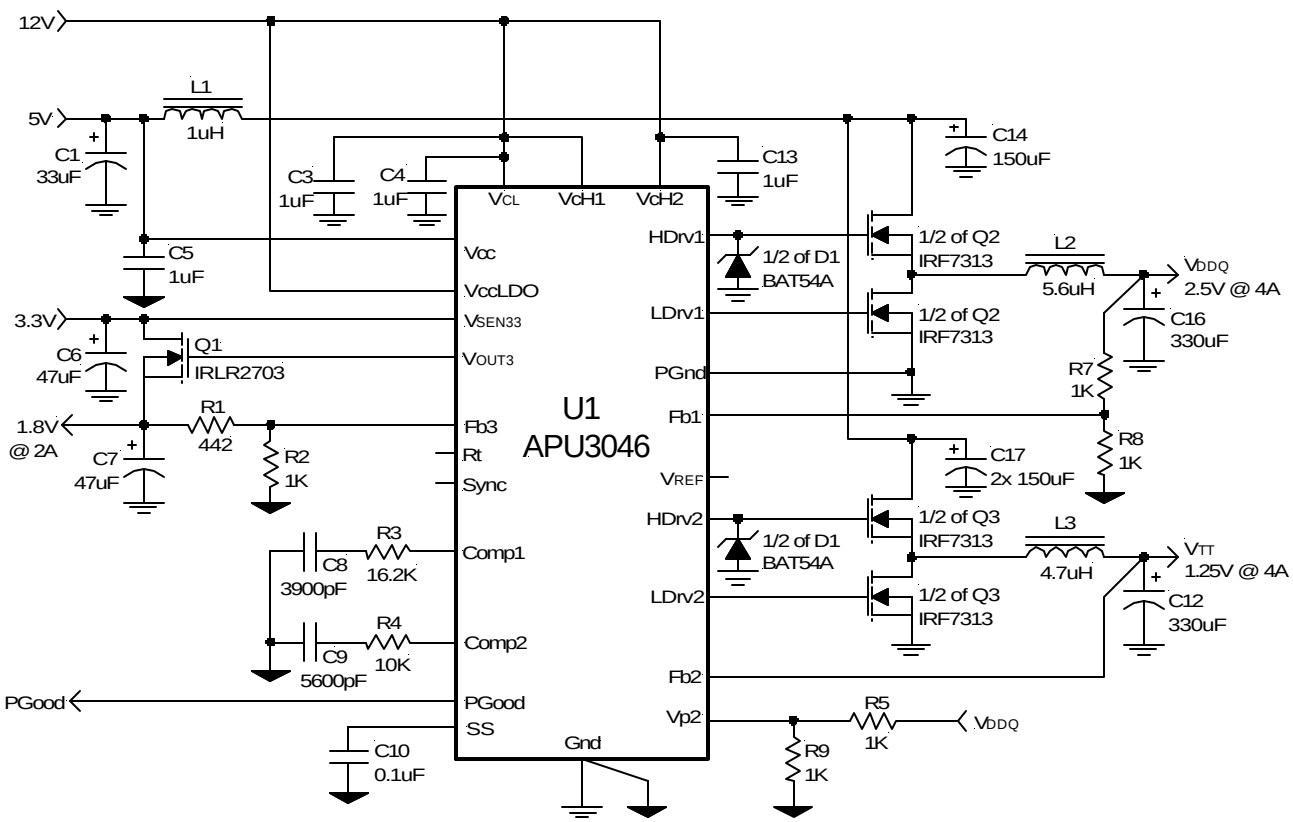


Figure 12 - Typical application for APU3046 configured for DDR memory application.

DEMO-BOARD APPLICATION

Dual Input: 5V and 12V to 1.5V @ 16A

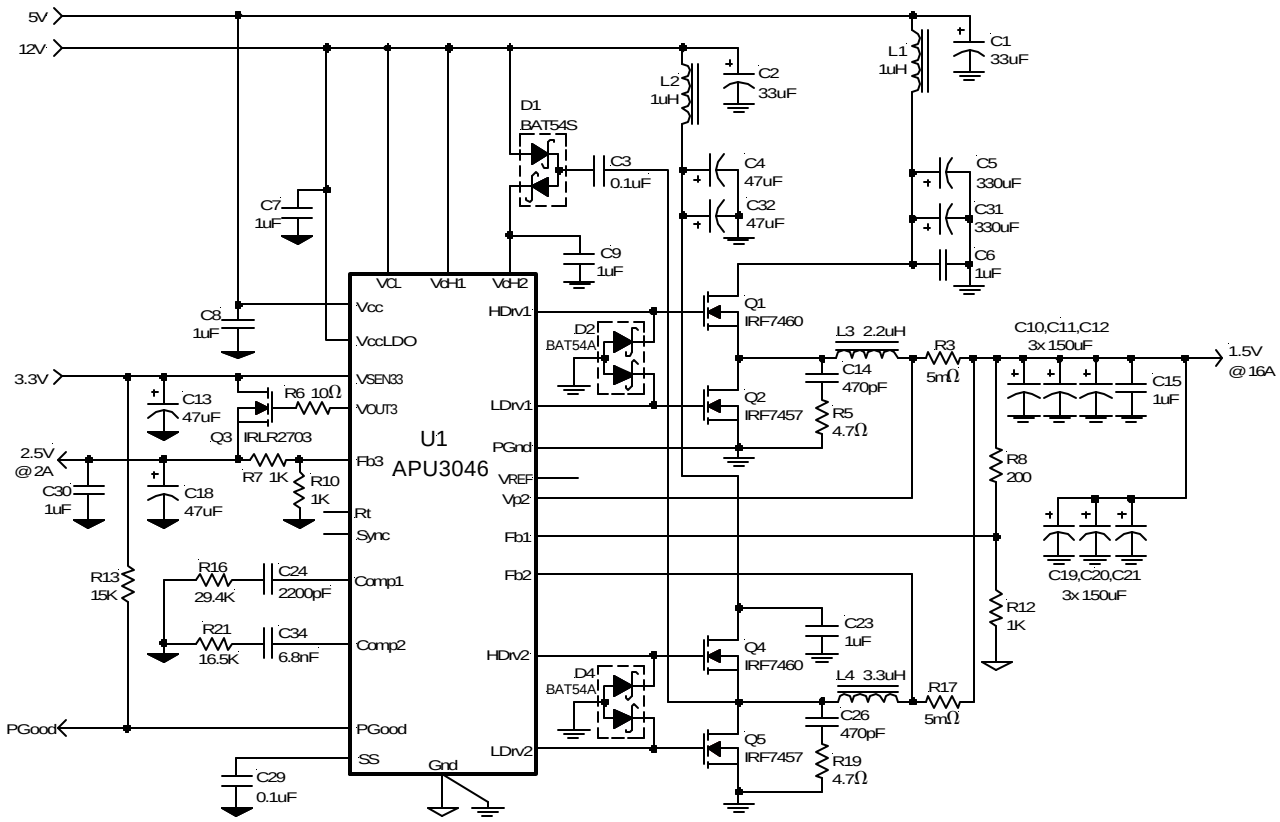


Figure 13 - Demo-board application of APU3046.

DEMO-BOARD APPLICATION

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q4	MOSFET	20V, 10mΩ, 12A	2	IRF7460	IR	irf.com
Q2,Q5	MOSFET	20V, 7mΩ, 15A	2	IRF7457	IR	
Q3	MOSFET	30V, 0.045Ω, 23A	1	IRLR2703	IR	
U1	Controller	Synchronous PWM	1	APU3046	APEC	
D1	Diode	Fast Switching	1	BAT54S	IR	
D2,D4	Diode	Fast Switching	2	BAT54A or 1N4148	IR Any	
L1,L2	Inductor	1μH, 6.8A	2	D03316P-102	Coilcraft	coilcraft.com
L3	Inductor	2.2μH, 12A	1	D05022P-222HC	Coilcraft	
L4	Inductor	3.3μH, 10A	1	D05022P-332HC	Coilcraft	
C1,C2	Cap, Tantalum	33μF, 16V	2	ECS-T1CD336R	Panasonic	maco.panasonic.co.jp
C4,C32	Cap, Poscap	47μF, 16V	2	16TPB47M	Sanyo	sanyo.com/industrial
C5,C31	Cap, Poscap	330μF, 6.3V	2	6TPB330M	Sanyo	
C10,11,12, 19,20,21	Cap, Poscap	150μF, 6.3V, 40mΩ	6	6TPC150M	Sanyo	
C3,C29	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	maco.panasonic.co.jp
C9	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C24	Cap, Ceramic	2200pF, X7R, 50V	1	ECJ-2VB1H222K	Panasonic	
C34	Cap, Ceramic	6800pF, X7R, 50V	1	ECJ-2VB1H682K	Panasonic	
C14,C26	Cap, Ceramic	470pF, X7R, 50V	2	ECJ-2VC1H471J	Panasonic	
C6,7,8, 15,23,30	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-2VF1C105Z	Panasonic	
C13,C18	Cap, Tantalum	47μF, 10V	2	ECS-T1AD476R	Panasonic	
R2,4,15,18	Resistor	2.15Ω	4			
R16	Resistor	29.4K	1			
R21	Resistor	16.5K	1			
R5,R19	Resistor	4.7Ω	2			
R8	Resistor	200, 1%	1			
R7,10,12	Resistor	1K, 1%	3			
R3,R17	Resistor	5mΩ, 1W, 1%	2	ERJ-M1WSF5MOU	Panasonic	
R13	Resistor	15K	1			
R6	Resistor	10Ω	1			

WAVEFORMS

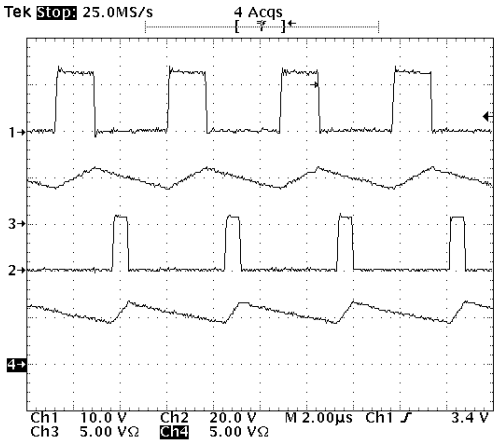


Figure 14 - Gate signals vs. inductor currents.

Ch1: Gate signal for control FET(master) (10V/div).
Ch2: Gate signal for control FET(slave) (20V/div).
Ch3: Inductor current for master channel (5A/div).
Ch4: Inductor current for slave channel (5A/div).
V_{MASTER}=5V, V_{SLAVE}=12V, I_{OUT}=10A

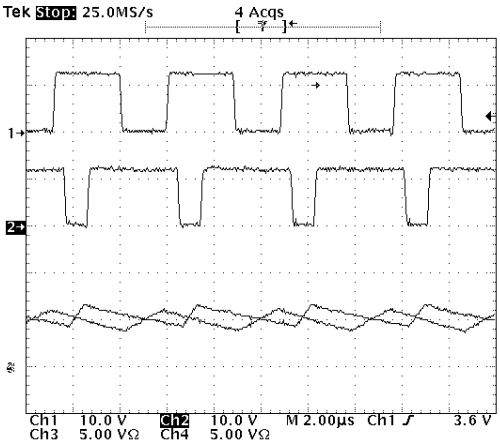


Figure 15 - Inductors current matching.

Ch1: Gate signal for sync FET(master) (10V/div).
Ch2: Gate signal for sync FET(slave) (10V/div).
Ch3: Inductor current for master channel (5A/div).
Ch4: Inductor current for slave channel (5A/div).
V_{MASTER}=5V, V_{SLAVE}=12V, I_{OUT}=10A

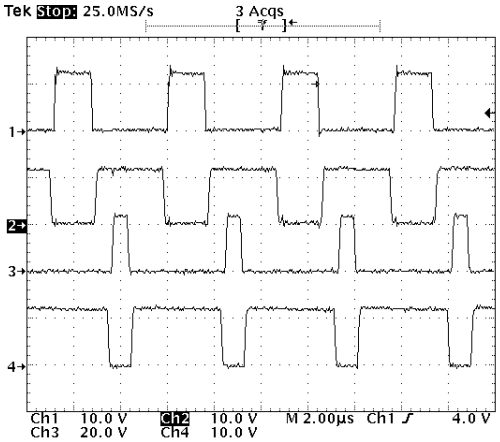


Figure 16 - Gate signals.

Ch1: Gate signal for control FET(master) (10V/div).
Ch2: Gate signal for sync FET(master) (10V/div).
Ch3: Gate signal for control FET(slave) (20V/div).
Ch4: Gate signal for sync FET(slave) (10V/div).

WAVEFORMS

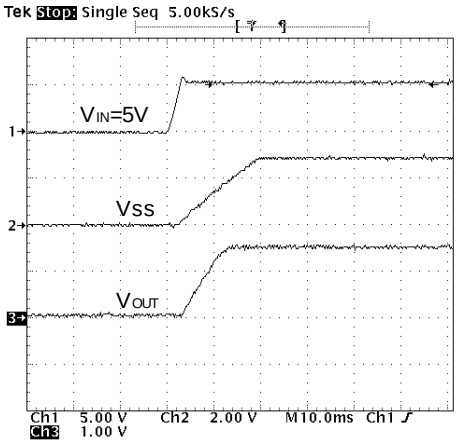


Figure 17 - Start-up @ I_{OUT} = 10A.

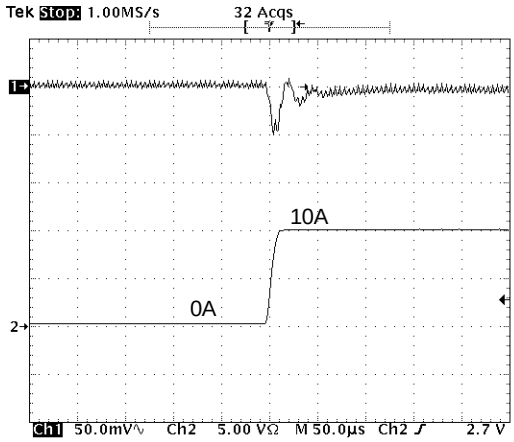


Figure 18 - Transient response @ I_{OUT} = 0 to 10A.

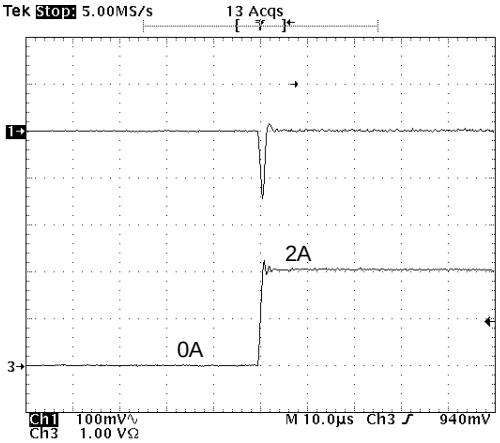
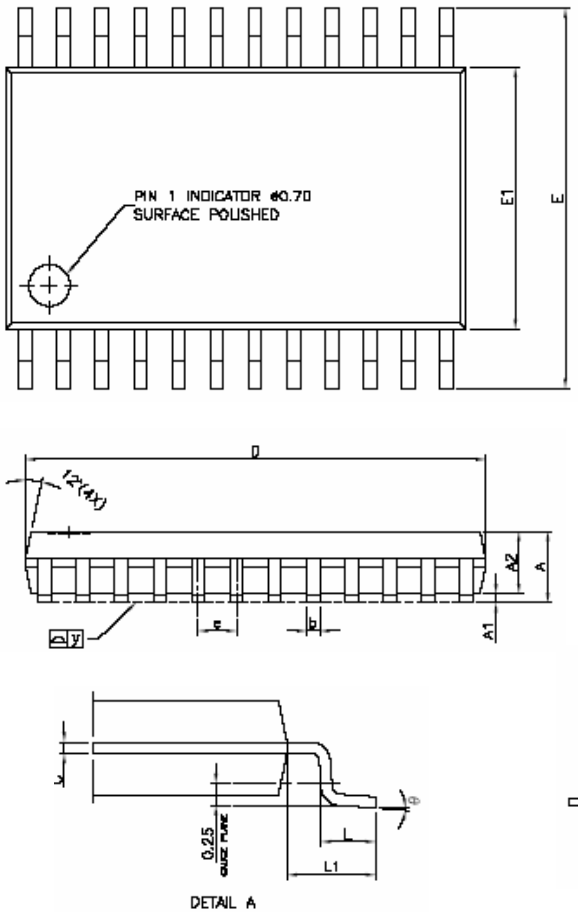


Figure 19 - Transient response for LDO @ I_{OUT} = 0 to 2A.

ADVANCED POWER ELECTRONICS CORP.

Package Outline : TSSOP-24



	Millimeters		
SYMBOLS	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.08	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	7.70	7.80	7.90
E	—	6.40	—
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.45	0.60	0.75
L1	—	1.00	—
y	—	—	0.08
θ	0.00	—	8.00

Part Marking Information & Packing : TSSOP-24