Single Synchronous Step-down Controller

FEATURES

- High Efficiency and Low Power Consumption
- 4700ppm/°C R_{DS-ON} Current Sense Compensation
- Selectable Auto-Skip / PWM-Only Mode
- Low-Side R_{DS-ON} Current Sense
- Positive and Negative Current Limit
- Integrate OV/UV and Thermal Shutdown Protections
- Integrated Boost Diode
- Wide Input Range: 3V to 28V
- Output Range: 0.7V to 5.5V
- 4 Selectable Frequencies (290 / 340 / 380 / 430 kHz)
- 0.5% Output Voltage Accuracy
- Power Good (PGOOD) Signal
- 1ms Soft Start and Output Discharge Function (Soft-stop)
- 100ns Load Step Transient Response
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Notebook and Sub-Notebook Computers
- I/O Supplies
- System Power Supplies

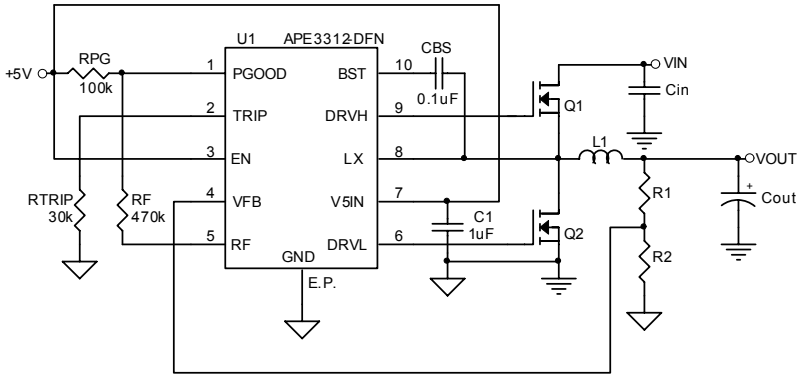
DESCRIPTION

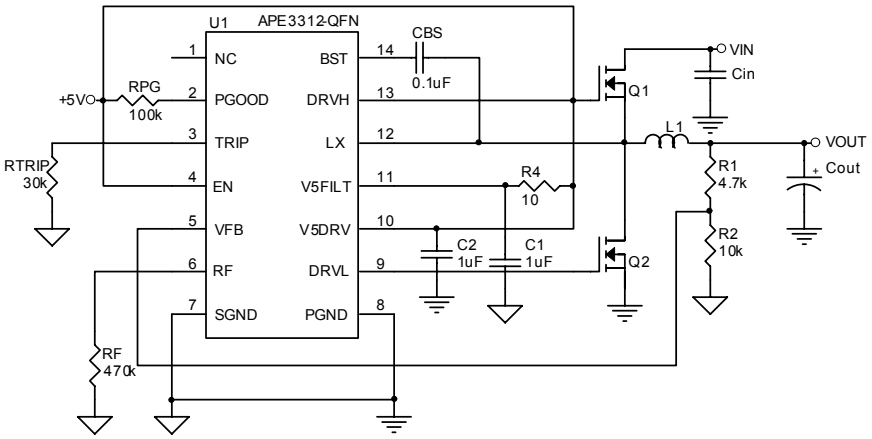
The APE3312 is a high efficiency synchronous buck controller for POL voltage regulator in notebook PC application. A small size and minimize pin cont scants PCB space. The quasi-fixed frequency mode with four frequencies selectable provides ease of use, fast transient response, and low external component count. APE3312 supports two operating modes. Auto-skip mode is for high efficiency in light loading. PWM-only mode is for low noise operation.

The APE3312 has several protect function, includes over voltage protection, positive and negative over current protection, and over temperature protection to prevent system or IC damage. Besides, the internal soft-start function prevents inrush-current and overshoot voltage issues in the start up. The device receives a 5V supply form another regulator. The conversion input ranging is from 3V to 28V, and output ranging is from 0.7V to 5.5V.

The APE3312 is available in a 10-pin DFN and 14-pin QFN packages.

TYPICAL APPLICATION



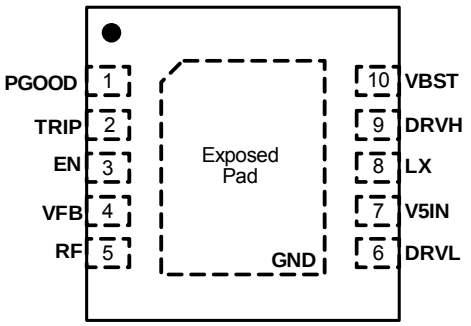


ORDERING / PACKAGE INFORMATION

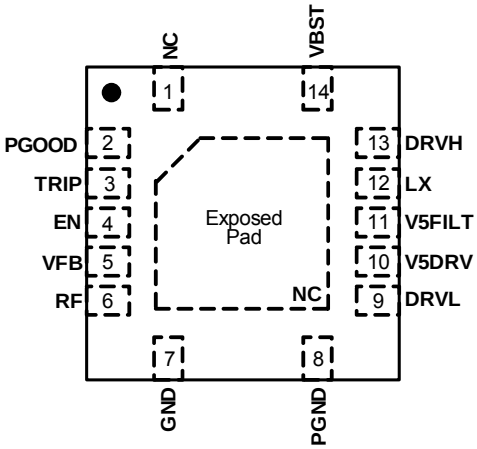
APE3312X

Package Type
GN3: DFN 3x3-10L
VN35: QFN 3.5x3.5-14L

Top View
DFN 3x3-10L



Top View
QFN 3.5x3.5-14L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VBST	-0.3V to 36V
VBST to LX	-0.3V to 6V
EN, TRIP, V5IN, V5DRV, V5FILT	-0.3V to 6V
RF	-0.3V to 6V
DRVH	-1V to 36V
DRVH to LX	-0.3V to 6V
LX	-1V to 30V
PGOOD, DRVL	-0.3V to 6V
PGND, GND	-0.3V to 0.3V
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	125°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Case ($R\theta_{JC}$)	
DFN-10 (3mmx3mm)	43°C/W
QFN-14 (3.5mmx3.5mm)	60°C/W

RECOMMENDED OPERATING CONDITIONS

VBST	4.5V to 34V
VBST to LX	4.5V to 5.5V
EN, TRIP, V5IN, V5DRV, V5FILT	-0.1V to 5.5V
DRVH	-0.8V to 34V
DRVH to LX	-0.1V to 5.5V
LX	-0.8V to 28V
PGOOD, DRVL	-0.1V to 5.5V
PGND, GND	-0.1V to 0.1V
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(VIN=2.95 to 6V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Input						
Input Voltage Range	V_{IN}		3		28	V
	V5IN		4.5		5.5	V
V5IN Supply Current	I_{V5IN}	V5IN current, EN=5V, VFB=0.735V, LX = -0.1V, no loading		320	500	uA
V5IN Shutdown Current	$I_{V5IN-SD}$	V5IN current, EN =0V		0	1	uA
Output						
Output Voltage Range	V_{OUT}	Adjustable output range	0.7		5.5	V
FB Voltage Regulation Range	V_{FB}	PWM mode		700		mV
		Auto-Skip mode	700.5	704	707.5	mV
FB Input Current	I_{FB}	V_{FB}, absolute value		0.1		uA
Output Discharge Current form LX	I_{DIS}	EN=0V, V_{LX}=0.5V	5	13		mA
Soft Start and On-time Timer						
Minimum On Time	$T_{ON(MIN)}$	V_{OUT}=0.7V, V_{LX}=28V, R_{RF}=39kΩ		79		ns
Minimum Off Time	$T_{OFF(MIN)}$			400		ns
Soft Start Time	T_{SS}	From EN=H to V_{OUT}=95%		1		ms
Output Drivers						
DRVH Resistance	R_{DRVH}	Source, $V_{VBST-DRVH}$=0.5V		1.5	3	Ω
		Sink, $V_{DRVH-LX}$=0.5V		0.7	1.8	Ω
DRVL Resistance	R_{DRVL}	Source, $V_{V5IN-DRVL}$=0.5V		1	2.2	Ω
		Sink, $V_{DRVL-GND}$=0.5V		0.5	1.2	Ω
Dead Time	T_D	DRVH-low(DRVH=1V) to DRVL-high(DRVL=4V), V_{LX}=-0.05V	7	17	30	ns
		DRVL-low(DRVL=1V) to DRVH-high(DRVH=4V), V_{LX}=-0.05V	10	22	35	ns
Boot Strap Switch						
Forward Voltage	V_{FBST}	$V_{V5IN-VBST}$, I_F=10mA		0.2	0.3	V

ELECTRICAL SPECIFICATIONS (Continued)

(T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
UVLO and LOGIC Threshold						
V_{5IN} UVLO Threshold	V_{UVLO}	Raising	4.2	4.38	4.5	V
		Falling	3.7	3.93	4.1	V
Switch Frequency	f_{SW}	R_{RF}= 470kΩ	266	290	314	kHz
		R_{RF}= 200kΩ	312	340	368	kHz
EN Voltage Threshold	V_{EN}	Enable	1.8			V
		Disable			0.5	V
EN Input Current	I_{EN}	EN=5V			1	uA
Mode Setting Voltage	V_{RF}	PWM mode	1.8			V
		Auto-skip mode			0.5	V
Current Sense						
TRIP Source	I_{TRIP}	V_{TRIP} < 0.3V	9	10	11	uA
I_{TRIP} Temperature Coefficient	V_{FB}			4700		ppm/°C
Current Limit Threshold Range Setting Range	V_{TRIP}	V_{TRIP} to GND	0.2		3	V
Overcurrent Limit Threshold	V_{OCL}	V_{TRIP}=3.0V	355	375	395	mV
		V_{TRIP}=1.6V	185	200	215	mV
		V_{TRIP}=0.2V	17	25	33	mV
Negative Overcurrent Limit Comparator Offset	V_{NOCL}	V_{TRIP}=3.0V	-395	-375	-355	mV
		V_{TRIP}=1.6V	-215	-200	-185	mV
		V_{TRIP}=0.2V	-33	-25	-17	mV
Power Good Function						
PGOOD Threshold	V_{THPG}	PG lower threshold (PGOOD goes high)	92.5	95	97.5	%
		PG low hysteresis (PGOOD goes low)	-2.5	-5	-7.5	%
		PG higher threshold (PGOOD goes low)	121	125	129	%
PGOOD Sink Current	I_{PGMAX}	PGOOD=0.5V	3	6		mA
PGOOD Delay	T_{PGDEL}	Delay for PGOOD in	0.8	1	1.2	ms

ELECTRICAL SPECIFICATIONS (Continued)

(T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Under-Voltage and Over-Voltage Protection						
V_{FB} OVP Trip Threshold	V_{OVP}	OVP detect	121	125	129	%
V_{FB} OVP Propagation delay (Note1)	T_{OVPDEL}			1		us
V_{FB} UVP Trip Threshold	V_{UVP}	UVP detect	65	70	75	%
V_{FB} UVP Delay	T_{UVPDEL}		0.8	1	1.2	ms
UVP Enable Delay	T_{UVPEN}	From Enable to UVP wrok	1	1.2	1.4	ms
Thermal Shutdown						
Thermal Shutdown Threshold (Note1)	T_{SD}			155		°C
		Hysteresis		10		°C

Note1: Guaranteed by design, not production tested.

PIN DESCRIPTIONS

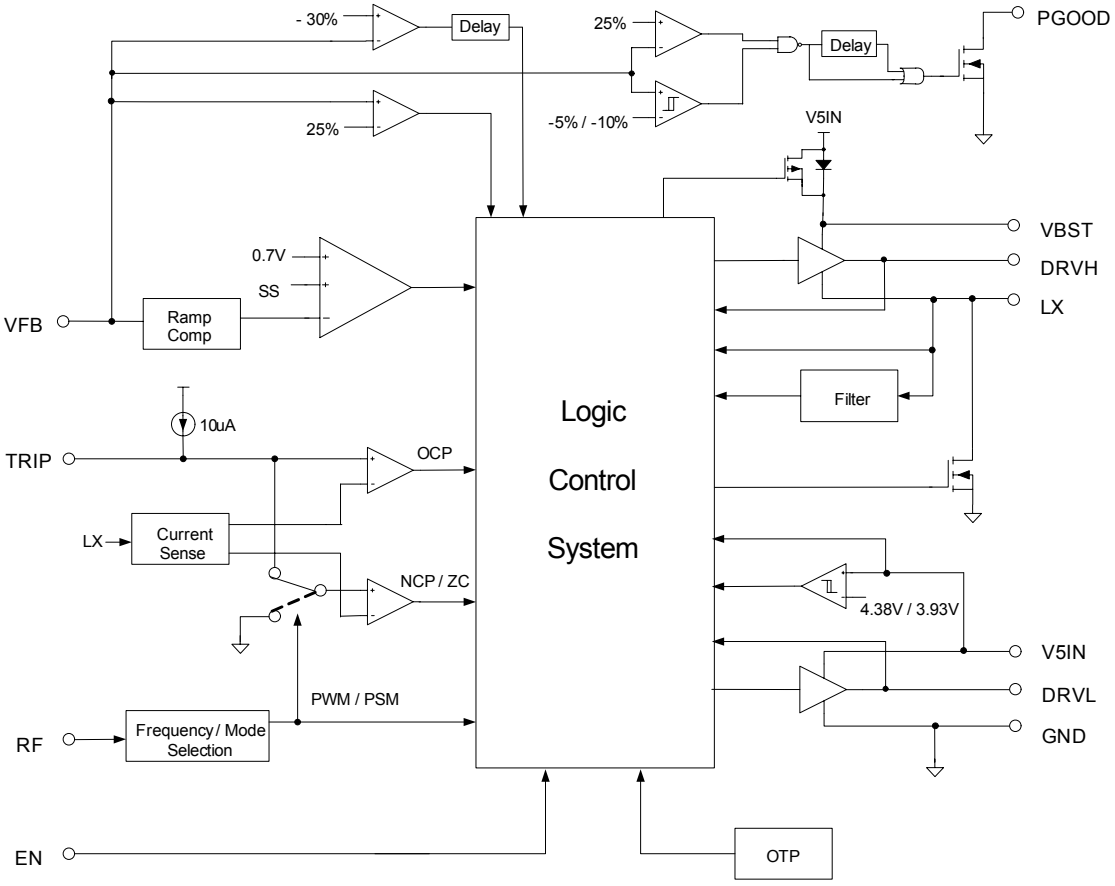
DFN-10L Package

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1	PGOOD	Power good output pin. PGOOD is an open-drain output. Connect a pull up resister to 5V. Current capability is 6mA.
2	TRIP	SMPS current limit threshold setting pin. Connect resistor form this pin to ground to set threshold for both overcurrent limit and negative overcurrent limit. Set the OCL trip voltage is $V_{OCL}=V_{TRIP}/8$
3	EN	SMPS Enable pin.
4	VFB	SMPS voltage feedback input
5	RF	Switch frequency / Mode selection pin. Connect a resistance to selection switching frequency. Besides, as the resistance connects to GND is auto-skip mode, or connecting to PGOOD pin select PWM mode.
6	DRVL	Low side N-MOS gate driver output. Drive voltage is V5IN voltage.
7	V5IN	Power supply input.
8	LX	High side N-MOS gate driver return. Also used for on time generation and output discharge.
9	DRVH	High side N-MOS gate driver output. Drive voltage corresponds to VBST to LX voltage.
10	VBST	Supply input for high side N-MOS gate driver (Boost terminal). Connect capacitor from this pin to LX. An internal MOSFET is connected between V5IN to this pin. Designer can add external Schottky diode if forward drop is critical to drive the power N-MOS.
Exposed Pad	GND	Ground.

QFN-14L Package

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1	NC	No connect
2	PGOOD	Power good output pin. PGOOD is an open-drain output. Connect a pull up resister to 5V. Current capability is 6mA.
3	TRIP	SMPS current limit threshold setting pin. Connect resistor form this pin to ground to set threshold for both overcurrent limit and negative overcurrent limit. Set the OCL trip voltage is $V_{OCL}=V_{TRIP}/8$
4	EN	SMPS Enable pin.
5	VFB	SMPS voltage feedback input
6	RF	Switch frequency / Mode selection pin. Connect a resistance to selection switching frequency (refer to Table1). Besides, as the resistance connects to GND is auto-skip mode, or connecting to PGOOD pin select PWM mode.
7	GND	Signal ground.
8	PGND	Power ground.
9	DRVL	Low side N-MOS gate driver output. Drive voltage is V5IN voltage.
10	V5DRV	5V power supply input for MOS gate drivers. Internally connected to VBST by a MOSFET. Connect 1uF or more to PGND to support instantaneous current for gate drivers.
11	V5FILT	5V power supply input for all the control circuitry except gate drivers. Apply RC filter consists of 10Ω + 1uF at the pin input.
12	LX	High side N-MOS gate driver return. Also used for on time generation and output discharge.
13	DRVH	High side N-MOS gate driver output. Drive voltage corresponds to VBST to LX voltage.
14	VBST	Supply input for high side N-MOS gate driver (Boost terminal). Connect capacitor from this pin to LX. An internal MOSFET is connected between V5DRV to this pin. Designer can add external Schottky diode if forward drop is critical to drive the power N-MOS.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

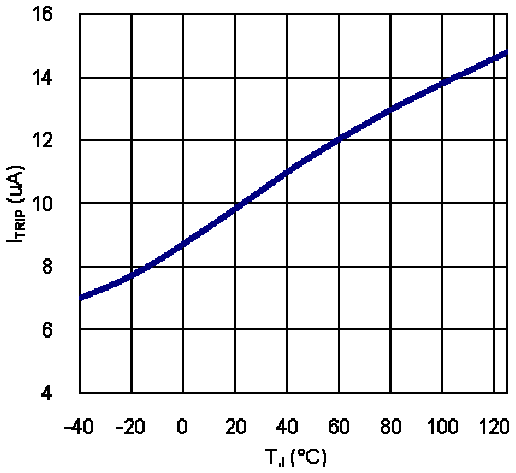


Fig.1 I_{TRIP} vs. Temperature

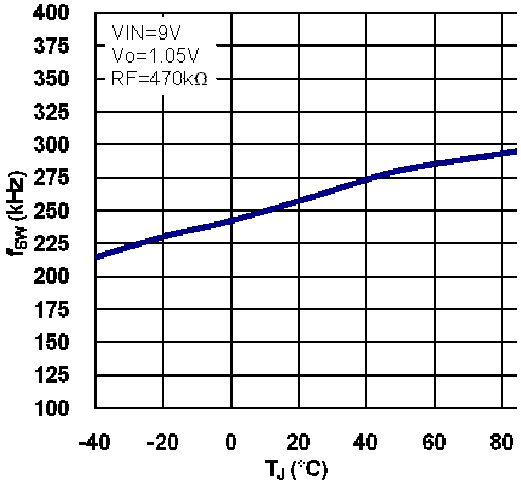


Fig.2 Switching Frequency vs. Temperature

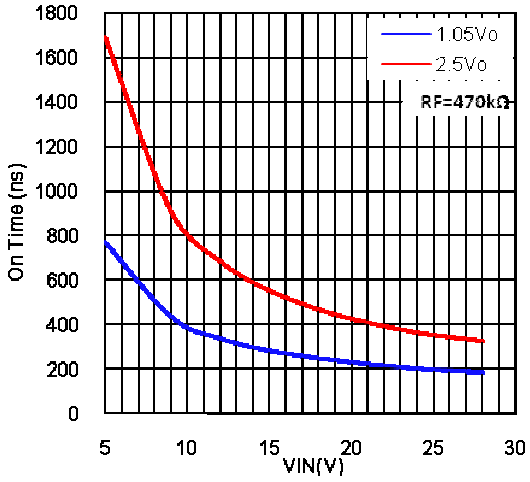


Fig.3 On Time vs. VIN

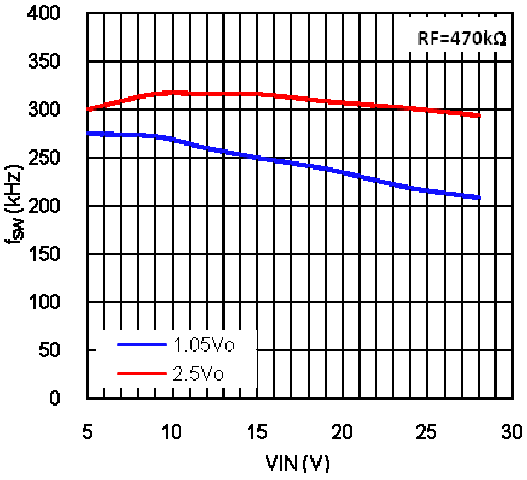


Fig.4 Switching Frequency vs. VIN

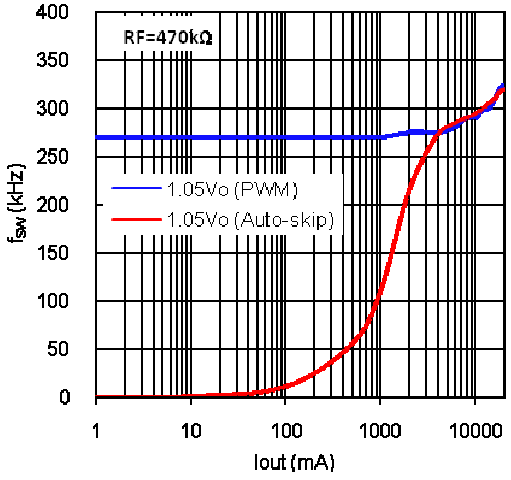


Fig.5 Switching frequency vs. Output Current

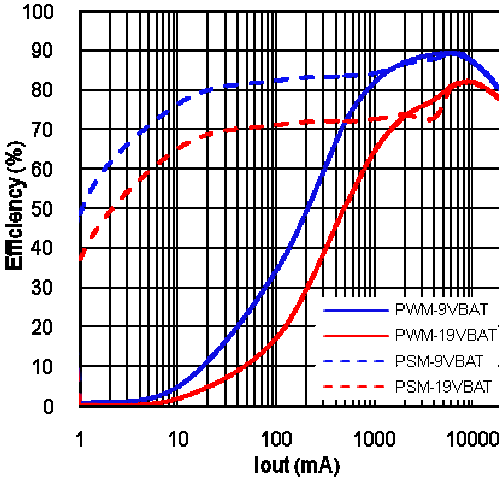


Fig.6 Efficiency for Vo=1.05V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

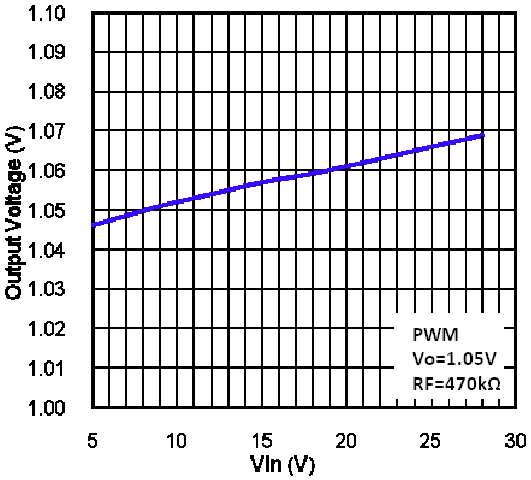


Fig.7 Line Regulation for Vo=1.05V

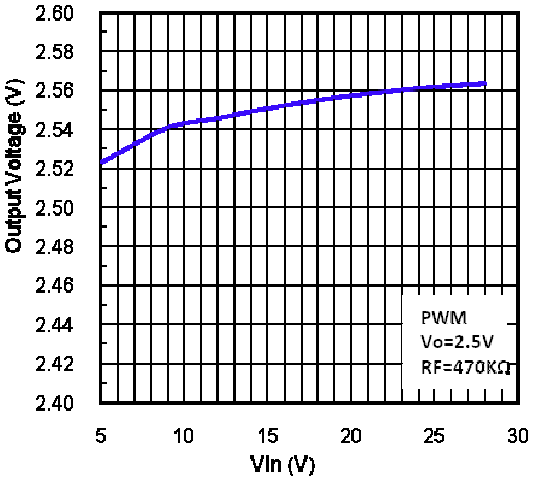


Fig.8 Line Regulation for Vo=2.5V

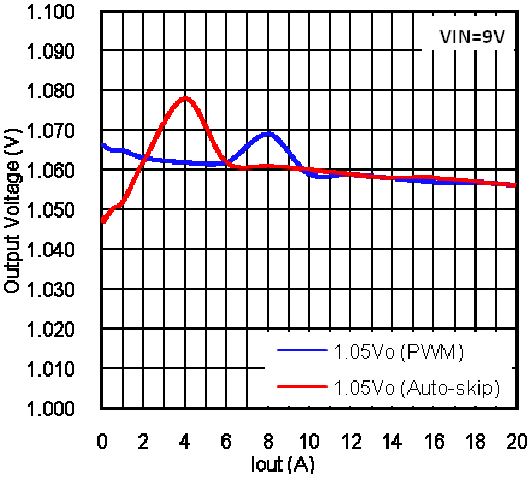


Fig.9 Load Regulation for Vo=1.05V

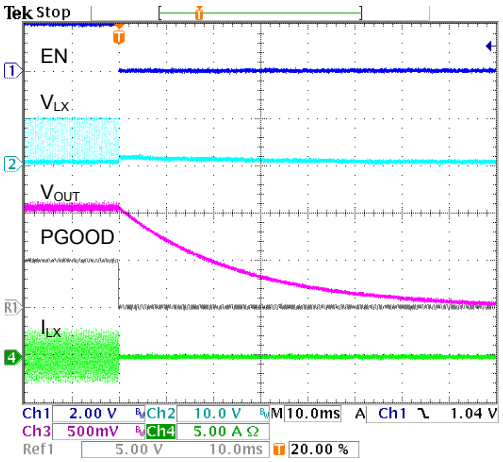


Fig.10 Shutdown Waveforms

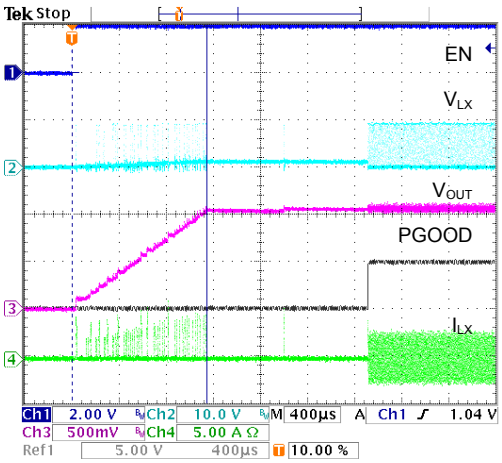


Fig.11 Start-up Waveforms, PWM mode
VIN=9V, Vo=1.05V, Io=0A

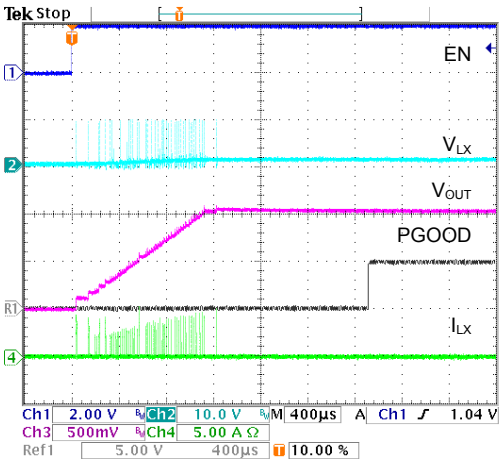


Fig.12 Start-up Waveforms, Auto-skip mode
VIN=9V, Vo=1.05V, Io=0A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

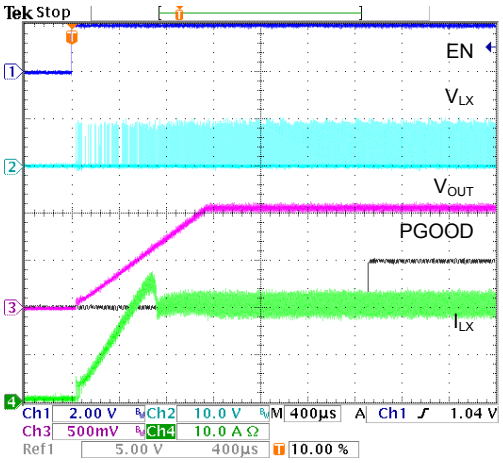


Fig.13 Start-up Waveforms, PWM mode
VIN=9V, Vo=1.05V, Io=20A

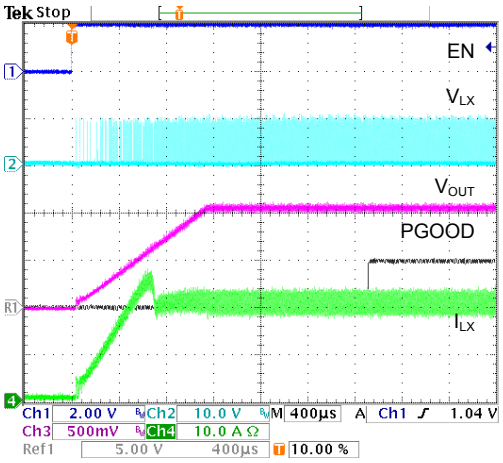


Fig.14 Start-up Waveforms, Auto-skip mode
VIN=9V, Vo=1.05V, Io=20A

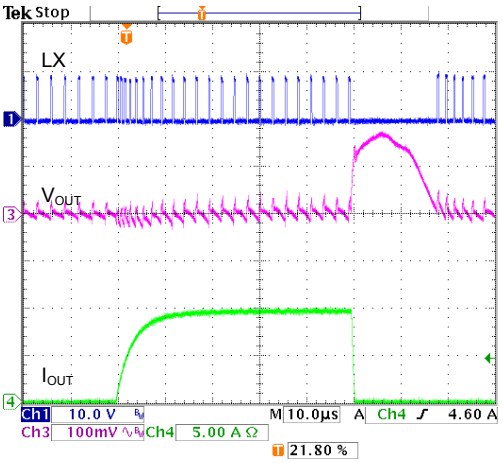


Fig.15 VIN=9V, Vo=1.05V, PWM mode
f_{SW}=340kHz, L=1uH, Cout=330uF/9mΩ *1

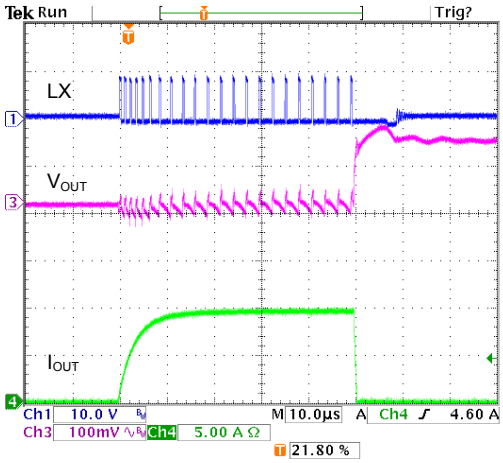


Fig.16 VIN=9V, Vo=1.05V, Auto-skip mode
f_{SW}=340kHz, L=1uH, Cout=330uF/9mΩ *1

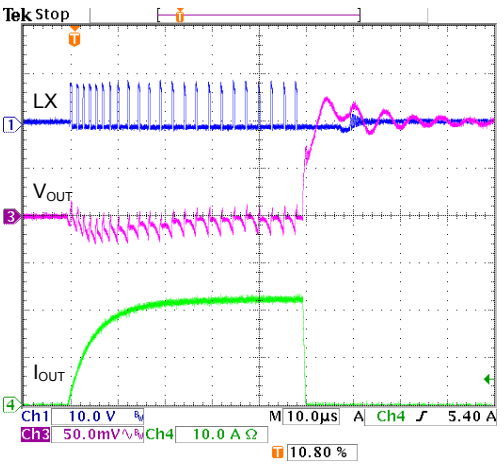


Fig.17 VIN=9V, Vo=1.05V, PWM mode
f_{SW}=340kHz, L=0.47uH, Cout=330uF/9mΩ *3

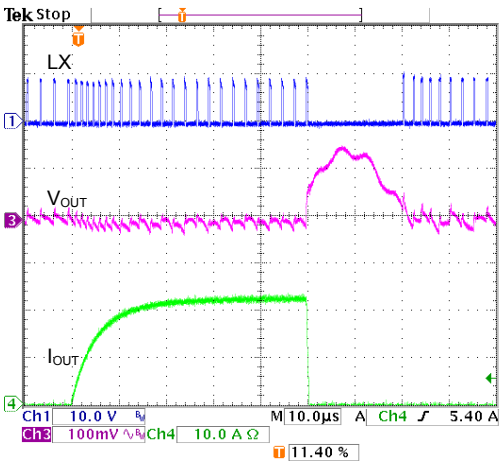


Fig.18 VIN=9V, Vo=1.05V, Auto-skip mode
f_{SW}=340kHz, L=0.47uH, Cout=330uF/9mΩ *3

DETAIL DESCRIPTION

The APE3312 synchronous buck controller is designed for low-voltage power supplies for notebook PC applications. The APE3312 control scheme is a constant-on-time, pseudo-fixed frequency, current-mode PWM controller and specifically designed for leading fast load transient while maintaining a relative constant switching frequency and operating over a wide range of input voltage. This architecture depends on the ESR of output capacitor; the output ripple voltage across the ESR provides the PWM ramp signal, eliminating the need for a current sense resistor. The high-side switch on-time is determined by an internal one-shot which pulse width is inversely proportional to input voltage and proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ.). The on-time one-shot is triggered if the error comparator is low.

+5V Bias Input

The APE3312 requires an external +5V bias supply in addition to the battery voltage. The external bias supply is needed to supply the PWM control circuitry and gate drivers. The +5V input can be generated by an external linear regulator, if stand-alone capability is needed. The 5V bias supply must be power up after to the battery supply (VIN) is present to ensure startup well.

On-Time One-Shot (T_{ON})

The core of pseudo fixed frequency PWM is the one-shot that sets the on-time of high-side switch for the controller. This low jitter, adjustable one-shot includes circuitry that varies the on-time in response to VIN and output voltage. The on-time is disproportional to the input voltage, and proportional to the output voltage, so that the duty ratio is kept as VOUT/VIN theoretically.

Switch frequency / Mode selection

The switching frequency is selectable from four preset values by a resistor connected to RF as shown in Table 1. Leave the RF pin open to set the lowest switching frequency, 290 kHz.

The APE3312 operates with PWM-only or auto-skip mode by connecting R_{RF} high or low to provide multi-function. Pull RF pin low via R_{RF} to set the APE3312 operates in auto-skip mode. Pull RF pin high via R_{RF} to force PWM-only mode.

Resistance (kΩ)	Switching Frequency (kHz)
470	290
200	340
100	380
39	430

Table1. R_{RF} vs. f_{SW}

DETAIL DESCRIPTION (Continued)

Auto-Skip Mode

In auto-skip mode, the internal Zero-Cross comparator looks for inductor current. When the zero current is detected, the controller enters auto-skip mode and turns low-side MOSFET off on each cycle. If the inductor current does not cross zero, the controller immediately exits auto-skip mode. At light load condition, the APE3312 operates in power save mode and reduces the switching frequency automatically to maintain high efficiency. This decreased frequency is performed smoothly and without increasing output ripple. The boundary between continuous and discontinuous inductor-current conduction mode, $I_{OUT(LB)}$, can be calculated by:

$$I_{OUT(LB)} = \frac{1}{2 \times L \times f_{sw}} \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Forced PWM-Only Mode

The low-noise, forced PWM-Only mode disables the zero-crossing comparator, which controls the low-side switch on-time. The constant switching frequency has two benefits: first, the frequency can be selected to avoid noise-sensitive regions; second, the inductor ripple-current remains relatively constant which resulting in easy to design and predictable output voltage ripple.

Output Voltage Setting

The output can be adjusted to a voltage range from 0.7V to 5.5V. The output voltage can be calculated as:

$$V_{OUT} = 0.7V \times (\frac{R1}{R2} + 1)$$

Current Limit

The current-limit circuit of APE3312 senses the R_{DS-ON} of low-side MOSFET, monitors valley inductor current. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. The current limit threshold is adjusted with an external resistor at TRIP pin. V_{TRIP} is set the current limit valley level, which is the following equation:

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times I_{TRIP} = R_{TRIP}(k\Omega) \times 10uA$$

Note that V_{TRIP} is internally limited ranging is from 0.2V to 3V.

The valley current limit threshold can be given as:

$$I_{OC(Valley)} = \frac{R_{TRIP}(k\Omega) \times I_{TRIP}(uA)}{8 \times R_{DS-ON}(m\Omega)} = \frac{V_{TRIP}(mV)}{8 \times R_{DS-ON}(m\Omega)}$$

Therefore, the load current at over-current threshold, Iocp, can be calculated as follows:

$$I_{OCP} = I_{OC(Valley)} + \frac{\Delta I_L}{2} = \frac{V_{TRIP}}{8 \times R_{DS-ON}} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}$$

The output voltage tends to fall down cause of an over current condition. Finally, it crosses the UVP threshold and shuts down the controller. The APE3312 also supports temperature compensated for R_{DS-ON} sensing. I_{TRIP} has 4700ppm/°C temperature coefficient to compensate the temperature dependency of the R_{DS-ON} to keep almost identical current limit threshold in operation temperature range.

DETAIL DESCRIPTION (Continued)

There is also a negative current limit in the forced continuous conduction mode that prevents excessive reverse inductor currents when VOUT is sinking current. The negative current limit detect threshold is approximate to the negative polarity of positive current limit threshold.

Soft Start

The APE3312 has an internal, 1ms, soft start with overcurrent limit. When the EN pin voltage rises above the enable threshold, the controller enters its start-up sequence. Soft-start allows a gradual increase of the internal current-limit level during startup to reduce the input surge currents.

Soft Stop

The APE3312 discharges output by an internal MOSFET connected between LX and PGND while EN is low or any fault shutdown condition. The discharge time is depended of the output capacitance and the discharge resistance.

Under-Voltage Lockout Protection (UVLO)

The APE3312 has V5IN (V5FILT) under-voltage lockout protection (UVLO). This is a non-latched protection. When the V5IN (V5FILT) voltage is lower than 3.93V, the APE3312 is off.

Power Good Output

The APE3312 provides a power good (PGOOD) output, which is an open-drain output requiring a pull-up resistor. Typically connect to +5V bias supply through a 100kΩ resistor. The PGOOD comparator continuously monitors the output for both over-voltage and under-voltage conditions. In shutdown and soft-start period, PGOOD is actively low. After soft-start, PGOOD is released after 1ms delay time when the output is within 95% of the threshold. If the output voltage is without 90% or 125% of the target threshold, the PGOOD becomes low immediately. Note that the PGOOD window detector is independent of the output over-voltage and under-voltage protection thresholds, but held low after an UVP or OVP.

Under Voltage Protection (UVP)

If VFB falls lower than 70% of nominal value, the DRVH and DRVL are pulled low to turn off the MOSFETs after 1ms. The APE3312 latches off until its EN input is toggled or the +5V bias supply is re-start. The UVP function is disabled during start-up period.

Over Voltage Protection (OVP)

If VFB exceeds 125% of nominal value, over-voltage protection is triggered. The DRVL latches high and the low side MOSFET is turned on and high side MOSFET is turned off. This action discharges the output capacitor rapidly. DRVL stays high and the output latches off until the EN input is toggled or the +5V bias supply is re-started.

APPLICATION INFORMATION

Inductor Selection

The inductor value determines the ripple current and the ripple voltage of the converter. This inductor choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The inductor selection is based on the ripple current which is typically set between 1/4 to 1/2 of the maximum load current. The switching frequency and ripple current determine the inductor which can be calculated as follows:

$$L = \frac{V_{OUT}(V_{IN}-V_{OUT})}{f_{SW} \times \Delta I_L \times V_{IN}}$$

The ripple current can be given by:

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}}$$

Output Capacitor Selection

The output capacitor must have high enough ESR to satisfy the ripple requirements for loop stability. The important parameters of capacitor are the ESR, the capacitance value, the RMS ripple current rating, and the voltage rating. For the output capacitor of APE3312, ESR is the most important parameter. Determine ESR to meet the required ripple voltage as follow:

$$ESR(m\Omega) = \frac{\Delta V_{OUT}}{\Delta I_L}$$

A minimum ESR is required to generate the required ripple voltage for regulation. Due to the pseudo fixed frequency PWM mode not contain an error amplifier in the loop; a sufficient feedback signal needs to be provided from output ripple. The VFB required 15mV ripple signal at least. That will generate output ripple

ΔV_{OUT} = (VOUT/0.7) × 15 mV

The capacitor is usually selected by ESR and voltage rating rather than by capacitance value. The conductive polymer capacitors are recommended to proper high capacitance and low ESR.

MOSFET Selection

Choose a high side MOSFET that has conduction loss equal to the switching loss at the optimum input voltage for maximum efficiency. Choose a low-side MOSFET that has the lowest R_{DS-ON}. Ensure that the APE3312 DL gate driver can drive low-side MOSFET. The current ability of the N-channel MOSFET must be more than the peak switching current. The voltage rating V_{DS} of the N-channel MOSFET should be at least 1.25 times the maximum input voltage. Low R_{DS-ON} MOSFET is for reducing the conduction loss. Low C_{ISS} MOSFET is for reducing the switching loss. But most of time, this two factors are trade-off. Consider the system requirement and define the MOSFETs rating.

APPLICATION INFORMATION (Continued)

Stability Consideration

The constant on-time, pseudo fixed frequency PWM scheme has natural frequency jitter. An mV order of noise on the feedback signal affects the frequency jitter from a few to ten percent of switching frequency. Double pulse and feedback loop unstable results in unstable operation. Double pulse occurs because the insufficient ripple at the VFB, or the VFB and VOUT ripple waveforms are very noisy and trigger the VFB comparator. If the ripple voltage of VFB is too small, the VFB waveform will be interfered with switching noise. The noise causes the VFB comparator to trigger too quickly after the 400ns minimum off -time. Double pulse will result in higher output ripple voltage but in most cases is harmless.

Design Procedure

First of all, specify the external component, input voltage range, output voltage tolerance, load current, and the desired switching frequency. There are two values of load current to consider: continuous and peak load current. Continuous load current is concerned with thermal stresses of MOSFETs. Peak load current determines the components stresses and design of threshold of the current limit. The following guidelines will help calculate the external components of the APE3312 as Typical Application Circuit.

1. Select inductor. Before determine the inductance, the ripple current, ΔI_L, must be defined first, typically set between 1/4 to 1/2 of the maximum load current. The ripple current can be defined as:

$$\Delta I_L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{L\times f_{SW}\times V_{IN}}$$

The inductor value can be calculated as follows:

$$L = \frac{V_{OUT}\times (V_{IN(max)}-V_{OUT})}{\Delta I_L\times f_{SW}\times V_{IN(max)}}$$

The inductor current must be rated for maximum peak current.

$$I_{L(PEAK)} = I_{OC(Valley)} + \Delta I_L = \frac{V_{TRIP}}{R_{DS-ON}} + \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{L\times f_{SW}\times V_{IN}}$$

2. Select R1 and R2. The recommended value for R2 is between 10kΩ and 20kΩ. $R1 = R2\times(\frac{V_{OUT}-0.7}{0.7})$

3. Choose output capacitor. The output capacitance is based on transient ability.

$$C_{OUT(min)} = \frac{L\times (I_{out(max)} + 0.5\Delta I_L)^2}{\Delta V_{OUT}{}^2}$$

Determine ESR to meet the required ripple voltage, above 15mV. $ESR(m\Omega) = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{15mV\times V_{OUT}}{\Delta I_L\times 0.7V}$

4. Decide current limit threshold. Determine the current limit threshold when VIN is minimum and load current is maximum conditions. The R_{TRIP} determines by

$$R_{TRIP}(\Omega) = \frac{R_{DS-ON}}{10uA}\times (I_{OCP} - \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times L\times f_{SW}\times V_{IN}})$$

APPLICATION INFORMATION (Continued)

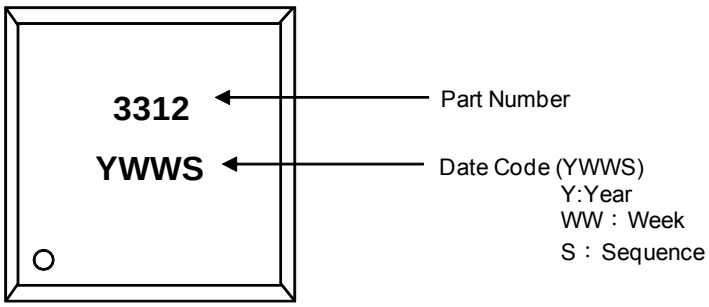
Layout Considerations

The switching power stages require more attention in PCB layout. Keep the high current paths short. Separate the ground terminals. Four-layer board is recommended. Use two middle layers as ground planes, with interconnections between top and bottom layers as needed. Below lists help start layout work.

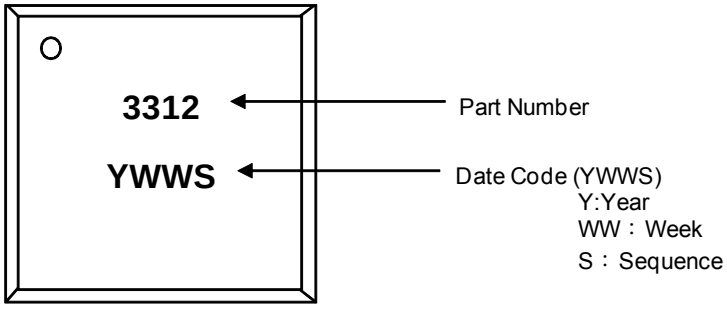
1. Minimize the resistance by keeping the power component group together with short and wide trace (60mil at least).
2. Minimize the high-side path with short and wide trace. This path starts at VIN, goes through the high-side MOSFET, through the inductor, through the output capacitor, through the input capacitor, and back to the input.
3. Minimize the low-side high current path. The high current path starts at the ground of the low-side MOSFET, goes through the low-side MOSFET, through the inductor, through the output capacitor, and back to the ground of the low-side MOSFET.
4. Power components should be grouped together near the gate drivers. Connect the drivers of DRVH and DRVL close to the gate of high-side and low-side MOSFET with short trace as possible to reduce stray inductance.
5. Place feedback resistors R1 and R2 near VFB and GND pin with short wire and should be far away to the noise source, such as switching loop. Use ground plane to shield feedback trace from power components.
6. Keep sensitive analog node (VFB, TRIP, and RF) away from high-speed switching loop to avoid noise coupling.
7. The current limit setting resistor, R_{TRIP}, should connect to TRIP and GND pin directly, next to the IC.
8. The frequency setting resistor, R_{RF}, should next to the IC.
9. Group the analog ground connection of the V5IN (V5FILT) bypass capacitors, VFB, RF, and TRIP. Connect the analog ground plane directly to GND pin of the IC.
10. Group the power ground connection of the VIN capacitor, VOUT capacitor, and the source of the low-side MOSFETs as close as possible. Connect this power ground plane directly to PGND pin of the IC.
11. PGND is used as the positive current sensing node so PGND should be connected to the source terminal of the bottom MOSFET.
12. Use plane connection between GND (analog ground) and PGND (power ground) near the IC.

MARKING INFORMATION

DFN 3x3-10L

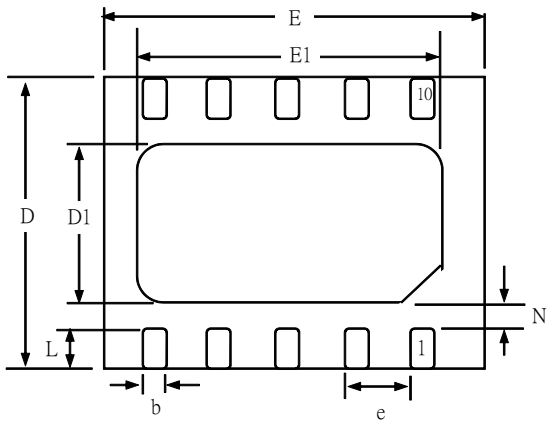


QFN 3.5x3.5-14L

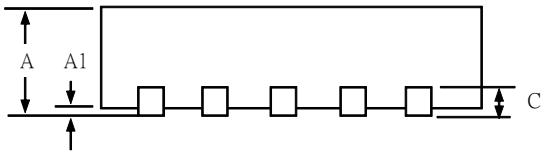


PACKAGE OUTLINE

DFN 3x3-10L



BOTTOM VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.70	0.85	1.00
A1	0.00	0.03	0.05
b	0.18	0.24	0.30
C	0.195	0.203	0.211
D	2.90	3.00	3.10
D1	1.55	1.62	1.69
E	2.90	3.00	3.10
E1	2.25	2.45	2.65
e	0.5 (ref.)		
L	0.35	0.43	0.50

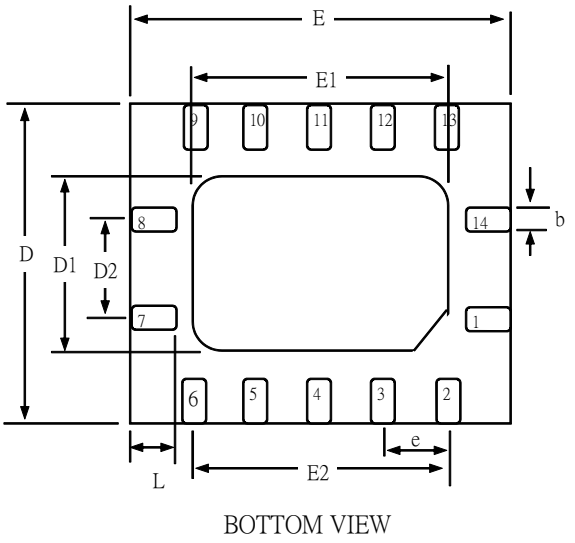
1.All Dimension Are In Millimeters.

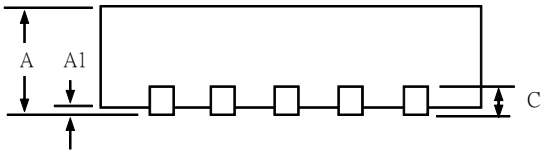
2.Dimension Does Not Include Mold Protrusions.

Draw No. I1-N310L-G-v00

PACKAGE OUTLINE (Continued)

QFN 3.5x3.5-14L





SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.03	0.05
b	0.19	0.24	0.29
C	0.195	0.203	0.211
D	3.45	3.50	3.55
D1	2.00	2.05	2.10
D2	1.50 ref.		
E	3.45	3.50	3.55
E1	2.00	2.05	2.10
E2	2.00 ref.		
e	0.5 (ref.)		
L	0.35	0.40	0.45

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Draw No. I1-VN35-14L-G-v00