

AP2761R-A

Pb Free Plating Product

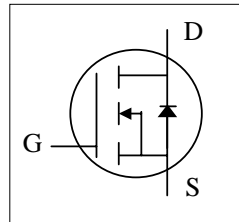


**Advanced Power
Electronics Corp.**

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

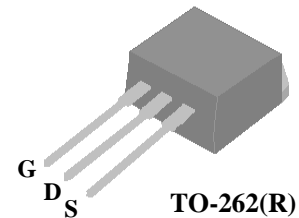
- ▼ Lower On-resistance
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant



BV_{DSS}	650V
$R_{DS(ON)}$	1 Ω
I_D	10A

Description

AP2761 series are specially designed as main switching devices for universal 90~265VAC off-line AC/DC converter applications. Both and TO-262 type provide high blocking voltage to overcome voltage surge and sag in the toughest power system with the best combination of fast switching, ruggedized design and cost-effectiveness.



The TO-262 package is universally preferred for all commercial-industrial applications. The device is suited for DC-DC, AC-DC converters for power applications.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.4	A
I_{DM}	Pulsed Drain Current ¹	18	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation	104	W
	Linear Derating Factor	0.8	W/ $^\circ C$
I_{AR}	Avalanche Current ²	10	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 1.2	$^\circ C/W$
Rthj-a	Thermal Resistance Junction-ambient	Max. 62	$^\circ C/W$

Data & specifications subject to change without notice

200503061-1/4


Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=1mA$	-	0.6	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=3.5A$	-	-	1	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=3.5A$	-	4.5	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=600V, V_{GS}=0V$	-	-	10	μA
	Drain-Source Leakage Current ($T_j=150^\circ\text{C}$)	$V_{DS}=480V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 30V$	-	-	± 100	nA
Q_g	Total Gate Charge ³	$I_D=10A$	-	53	85	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=520V$	-	10	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	15	-	nC
$t_{d(on)}$	Turn-on Delay Time ³	$V_{DD}=320V$	-	16	-	ns
t_r	Rise Time	$I_D=10A$	-	20	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=10\Omega, V_{GS}=10V$	-	82	-	ns
t_f	Fall Time	$R_D=32\Omega$	-	36	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	2770	4430	pF
C_{oss}	Output Capacitance	$V_{DS}=15V$	-	320	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	-	8	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ³	$I_S=10A, V_{GS}=0V$	-	-	1.5	V
t_{rr}	Reverse Recovery Time ³	$I_S=10A, V_{GS}=0V,$	-	610	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	8.64	-	μC

Notes:

1. Pulse width limited by safe operating area.
2. Starting $T_j=25^\circ\text{C}$, $V_{DD}=50V$, $L=1.2mH$, $R_G=25\Omega$, $I_{AS}=10A$.
3. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

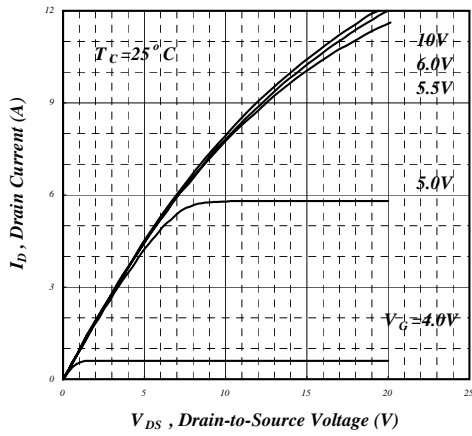


Fig 1. Typical Output Characteristics

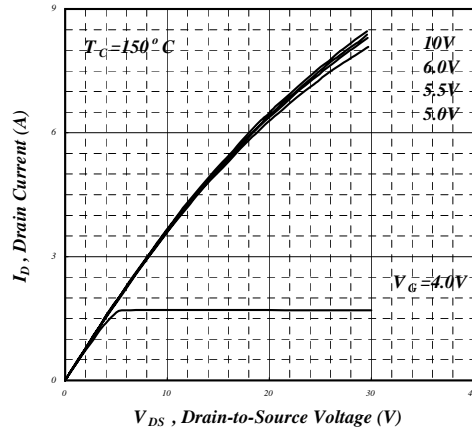


Fig 2. Typical Output Characteristics

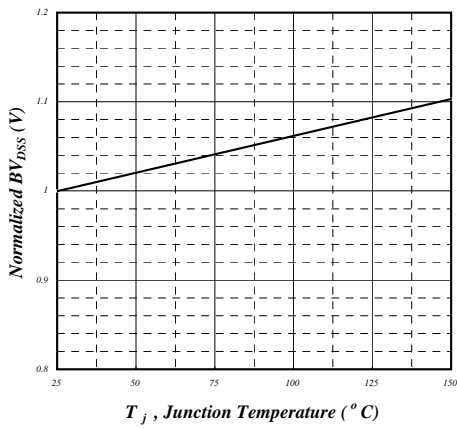


Fig 3. On-Resistance v.s. Gate Voltage

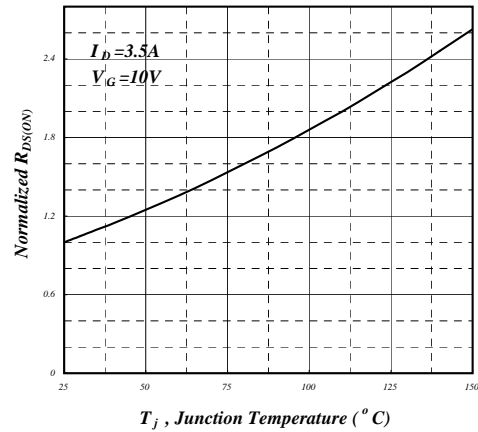


Fig 4. Normalized On-Resistance v.s. Junction Temperature

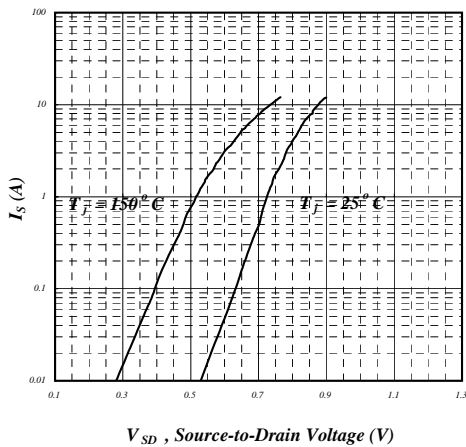


Fig 5. Forward Characteristic of Reverse Diode

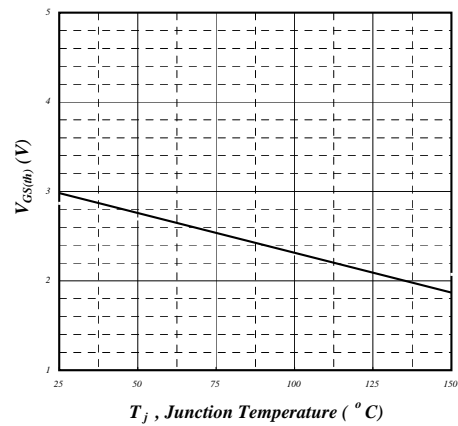


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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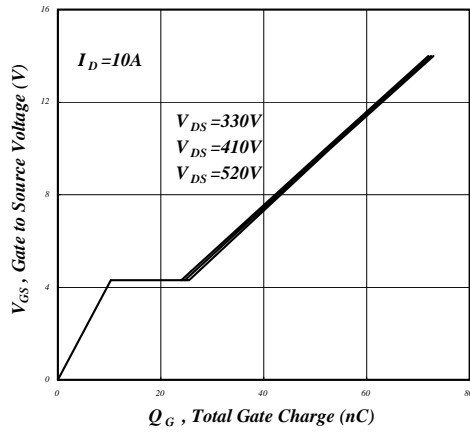


Fig 7. Gate Charge Characteristics

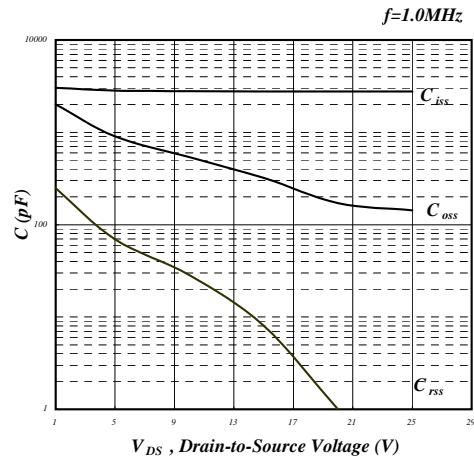


Fig 8. Typical Capacitance Characteristics

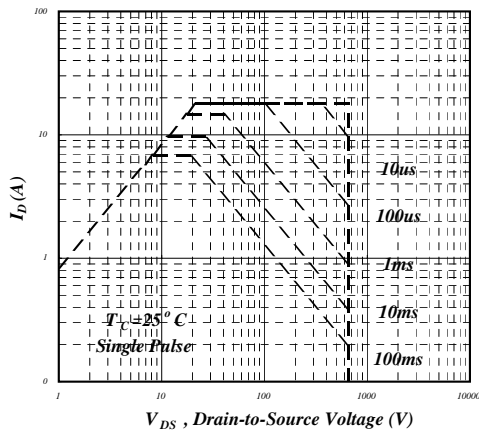


Fig 9. Maximum Safe Operating Area

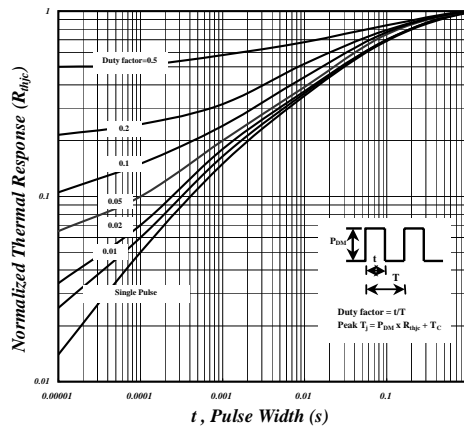


Fig 10. Effective Transient Thermal Impedance

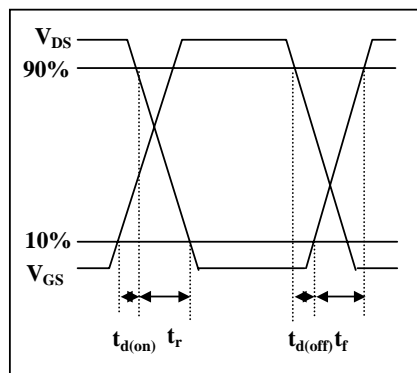


Fig 11. Switching Time Waveform

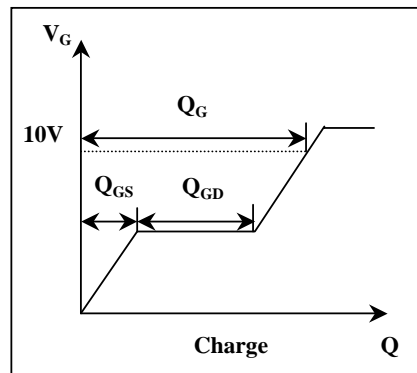


Fig 12. Gate Charge Waveform