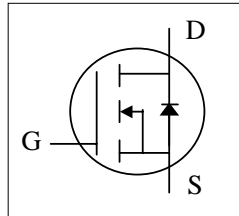




- ▼ Low Gate Charge
- ▼ Single Drive Requirement
- ▼ Fast Switching Performance
- ▼ RoHS Compliant & Halogen-Free

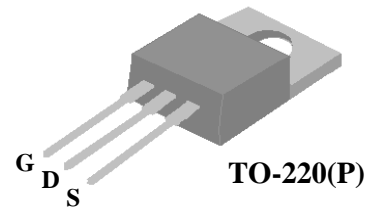


BV_{DSS}	60V
$R_{DS(ON)}$	16m Ω
I_D	60A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is widely preferred for commercial-industrial applications and suited for low voltage applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	+25	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	60	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	38	A
I_{DM}	Pulsed Drain Current ¹	240	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	89	W
	Linear Derating Factor	0.7	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.4	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$



Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.06	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	-	-	16	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =40A	-	44	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =60V, V _{GS} =0V	-	-	10	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =48V, V _{GS} =0V	-	-	250	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =40A	-	49	80	nC
Q _{gs}	Gate-Source Charge	V _{DS} =48V	-	13	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	20	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =30V	-	14	-	ns
t _r	Rise Time	I _D =40A	-	80	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	27	-	ns
t _f	Fall Time	R _D =0.75Ω	-	57	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2410	3860	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	290	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	240	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2	3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =40A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ²	I _S =30A, V _{GS} =0V,	-	48	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	75	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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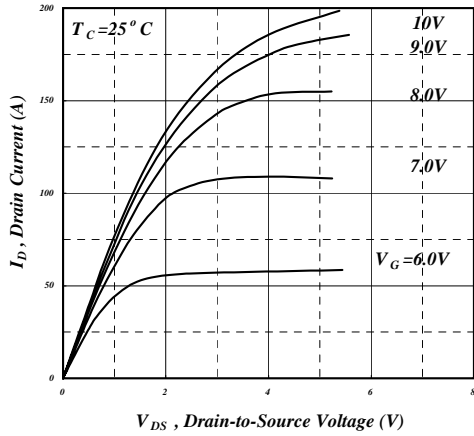


Fig 1. Typical Output Characteristics

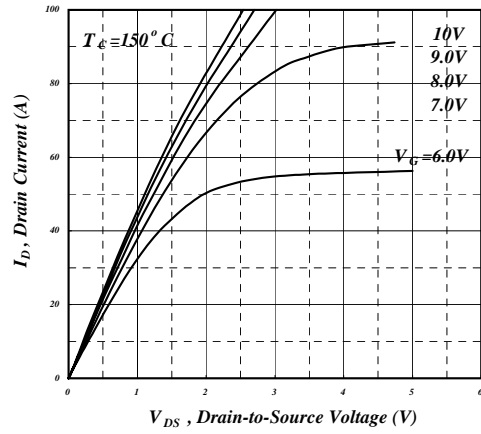


Fig 2. Typical Output Characteristics

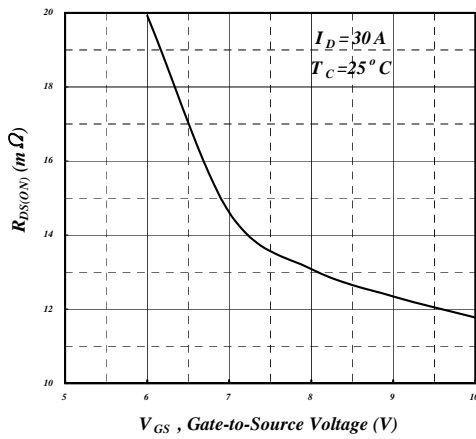


Fig 3. On-Resistance v.s. Gate Voltage

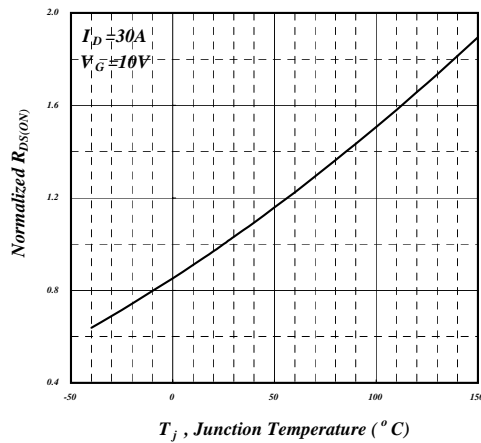


Fig 4. Normalized On-Resistance v.s. Junction Temperature

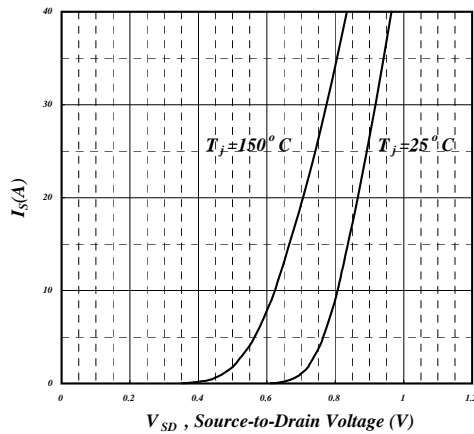


Fig 5. Forward Characteristic of Reverse Diode

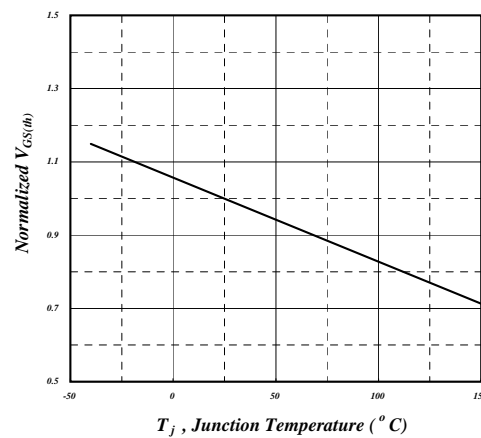


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

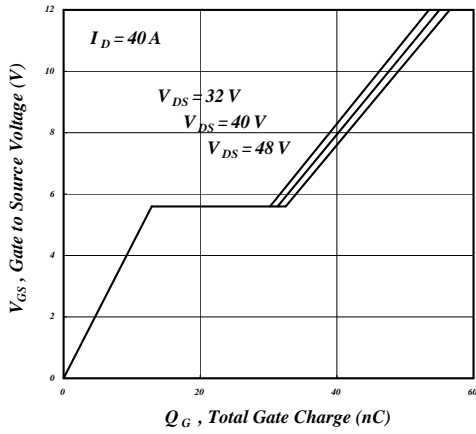


Fig 7. Gate Charge Characteristics

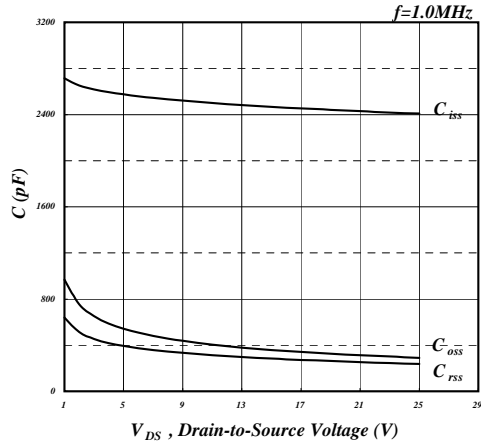


Fig 8. Typical Capacitance Characteristics

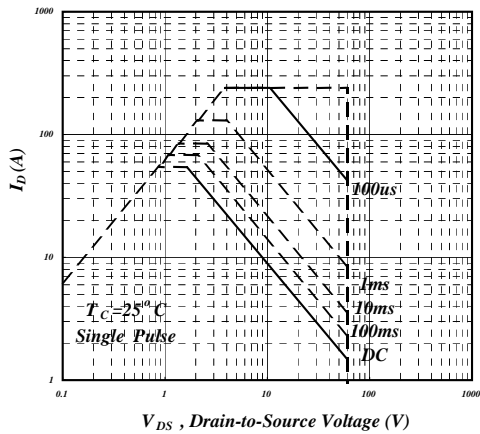


Fig 9. Maximum Safe Operating Area

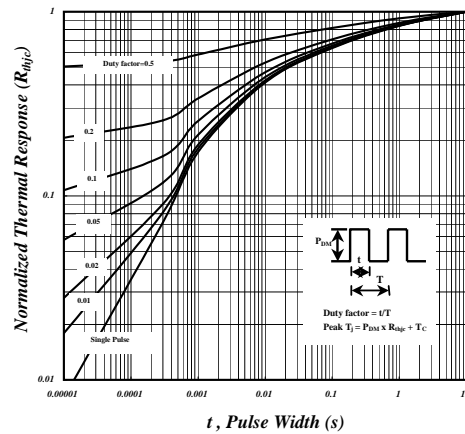


Fig 10. Effective Transient Thermal Impedance

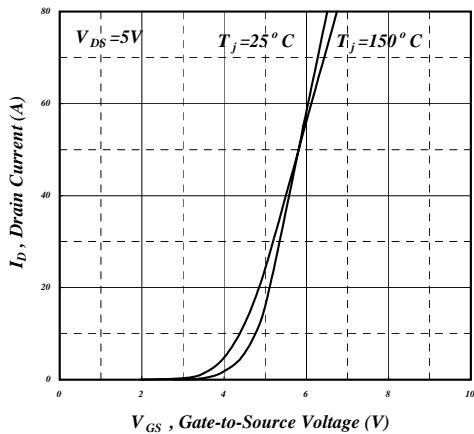


Fig 11. Transfer Characteristics

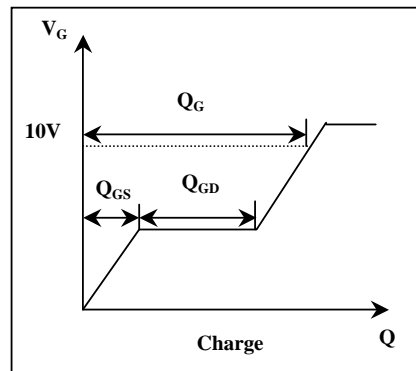


Fig 12. Gate Charge Waveform