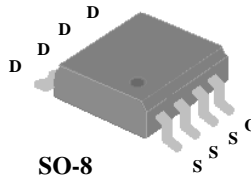
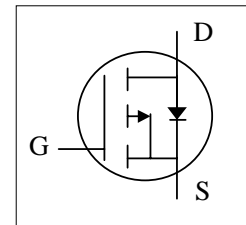




- ▼ Lower Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	-60V
$R_{DS(ON)}$	64m $\Omega$
$I_D$	-4.6A



## Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-60	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup> , $V_{GS}$ @ 10V	-4.6	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current <sup>3</sup> , $V_{GS}$ @ 10V	-3.6	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	-20	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	50	$^\circ\text{C}/\text{W}$



## Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-4A$	-	-	64	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=-10V, I_D=-4A$	-	10	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V$	-	-	-25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=-4A$	-	12.5	20	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-30V$	-	3.5	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	8	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=-30V$	-	11	-	ns
$t_r$	Rise Time	$I_D=-1A$	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	41	-	ns
$t_f$	Fall Time	$V_{GS}=-10V$	-	28	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	970	1550	pF
$C_{oss}$	Output Capacitance	$V_{DS}=-15V$	-	210	-	pF
$C_{riss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	150	-	pF

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=-1.9A, V_{GS}=0V$	-	-	-1.3	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=-4A, V_{GS}=0V,$	-	35	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	50	-	nC

### Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board ; 125 °C/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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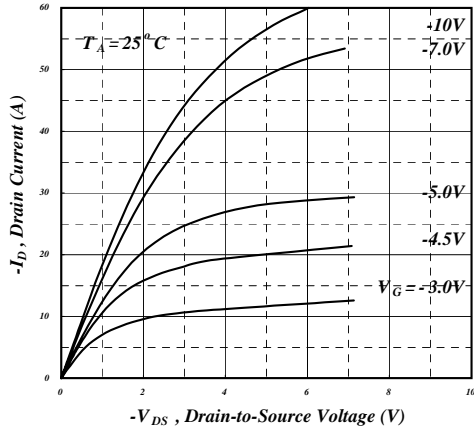


Fig 1. Typical Output Characteristics

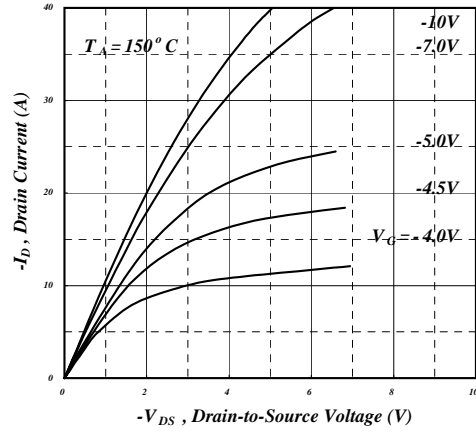


Fig 2. Typical Output Characteristics

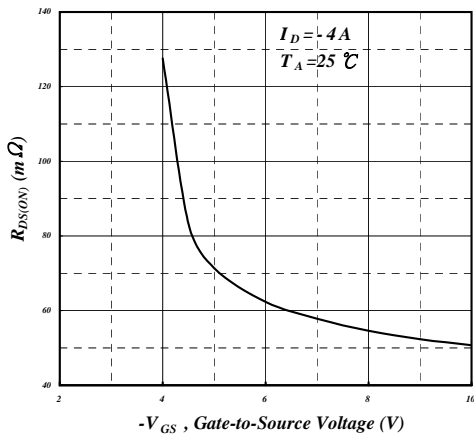


Fig 3. On-Resistance v.s. Gate Voltage

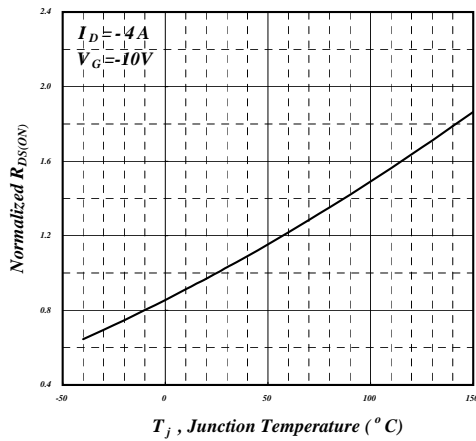


Fig 4. Normalized On-Resistance v.s. Junction Temperature

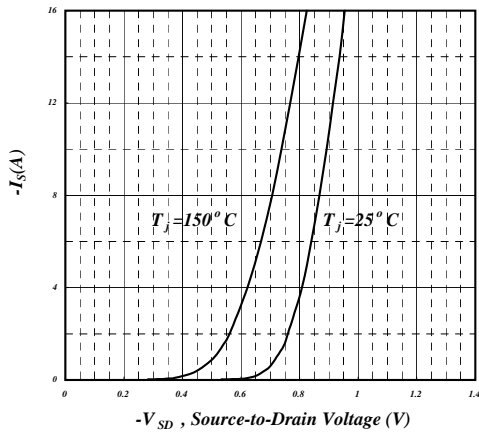


Fig 5. Forward Characteristic of Reverse Diode

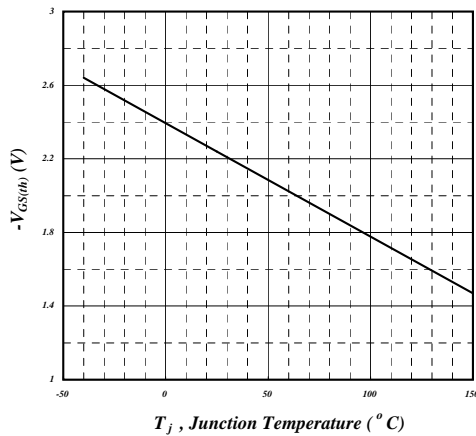


Fig 6. Gate Thresh. Voltage v.s. Junction Temperature

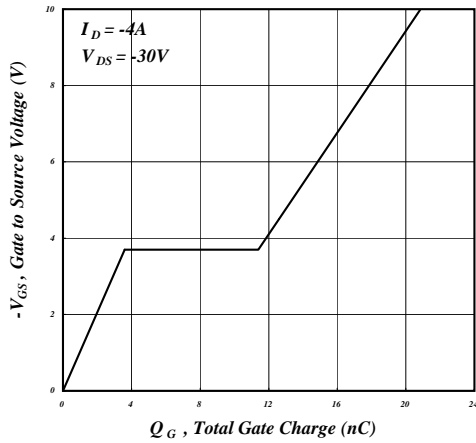


Fig 7. Gate Charge Characteristics

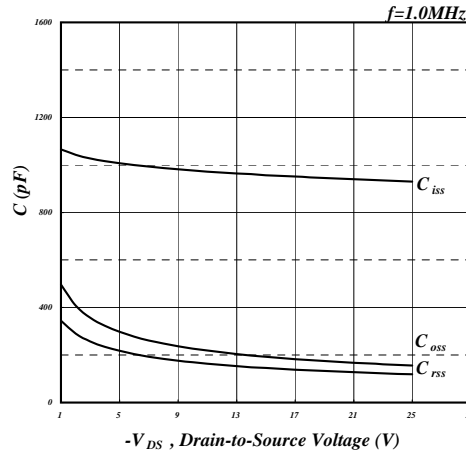


Fig 8. Typical Capacitance Characteristics

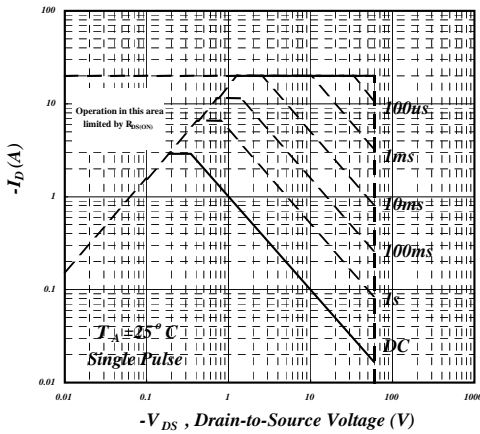


Fig 9. Maximum Safe Operating Area

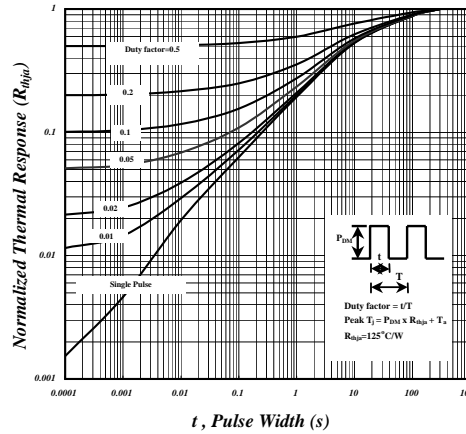


Fig 10. Effective Transient Thermal Impedance

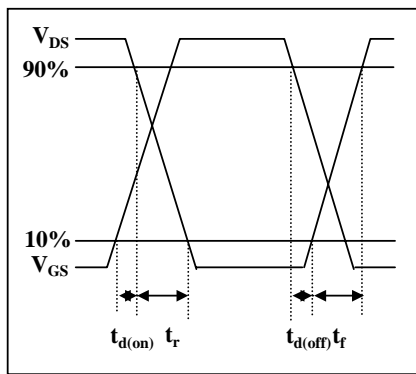


Fig 11. Switching Time Waveform

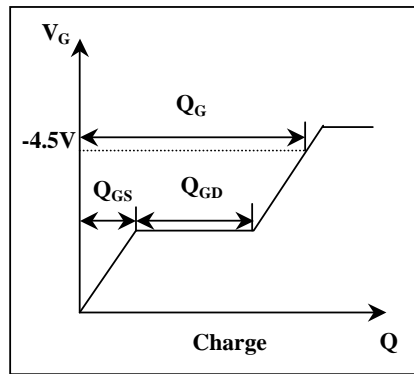


Fig 12. Gate Charge Waveform