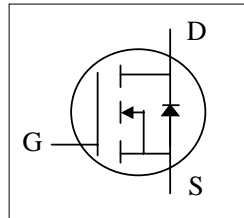




- ▼ **Low On-resistance**
- ▼ **Single Drive Requirement**
- ▼ **Surface Mount Package**

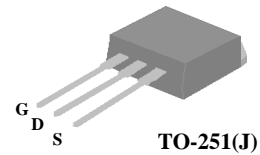
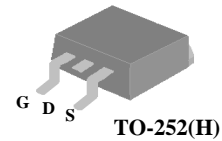


BV_{DSS}	60V
$R_{DS(ON)}$	36m Ω
I_D	25A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters. The through-hole version (AP9971GJ) are available for low-profile applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	25	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	16	A
I_{DM}	Pulsed Drain Current ¹	80	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	39	W
	Linear Derating Factor	0.31	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	3.2	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	62.5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	110	$^\circ\text{C}/\text{W}$



Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=1\text{mA}$	-	0.05	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=18A$	-	-	36	m Ω
		$V_{GS}=4.5V, I_D=12A$	-	-	50	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=18A$	-	17	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=125^\circ\text{C}$)	$V_{DS}=48V, V_{GS}=0V$	-	-	250	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=18A$	-	18	30	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=48V$	-	6	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	11	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=30V$	-	9	-	ns
t_r	Rise Time	$I_D=18A$	-	24	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	26	-	ns
t_f	Fall Time	$R_D=1.67\Omega$	-	7	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1700	2700	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	160	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	110	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=25A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=18A, V_{GS}=0V,$	-	37	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	38	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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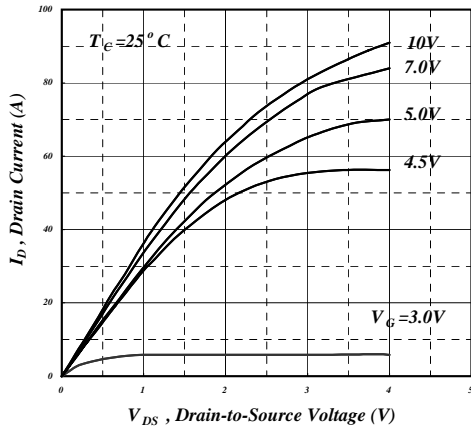


Fig 1. Typical Output Characteristics

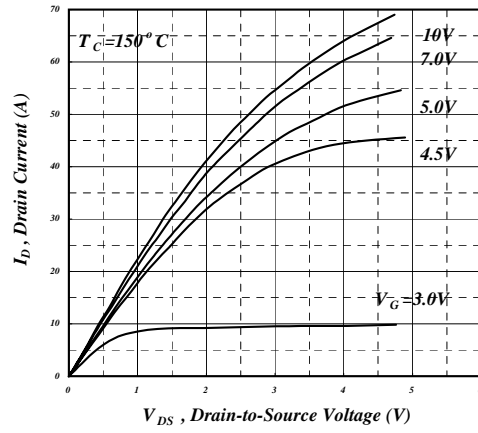


Fig 2. Typical Output Characteristics

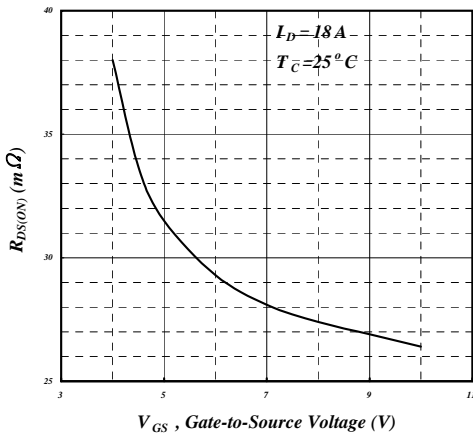


Fig 3. On-Resistance v.s. Gate Voltage

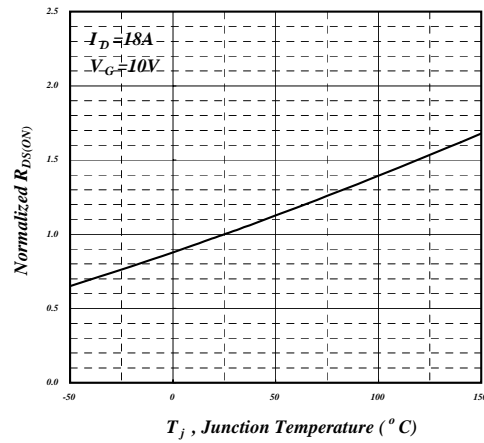


Fig 4. Normalized On-Resistance v.s. Junction Temperature

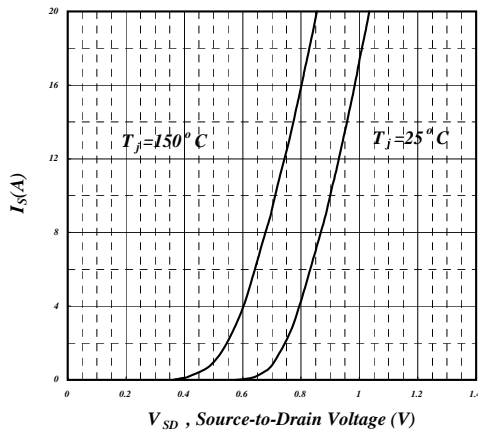


Fig 5. Forward Characteristic of Reverse Diode

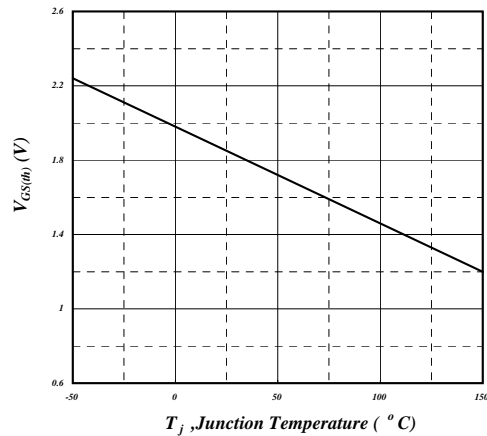


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

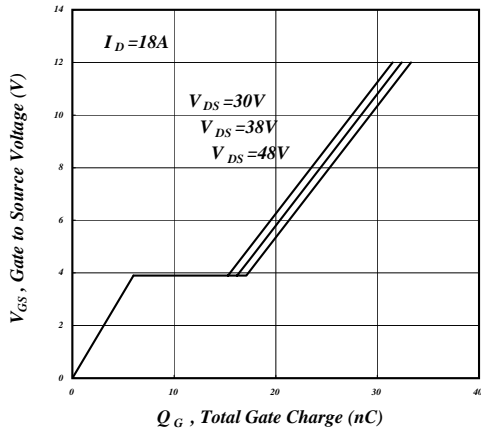


Fig 7. Gate Charge Characteristics

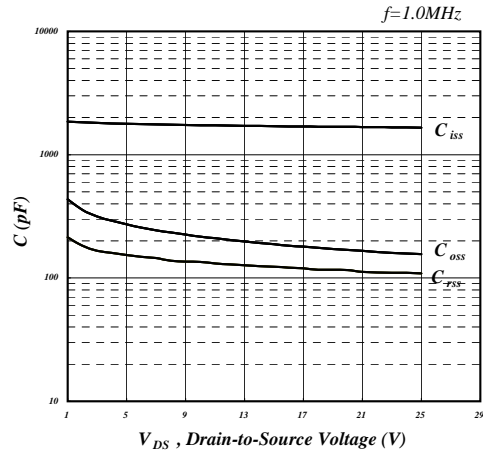


Fig 8. Typical Capacitance Characteristics

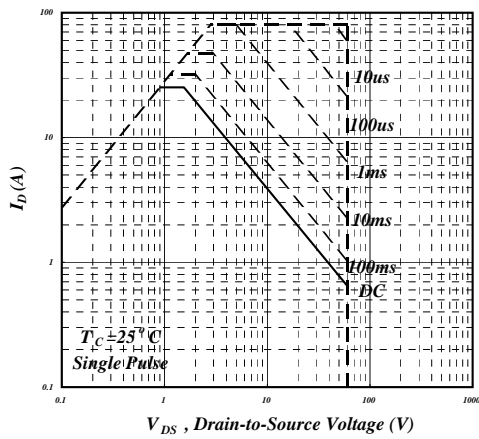


Fig 9. Maximum Safe Operating Area

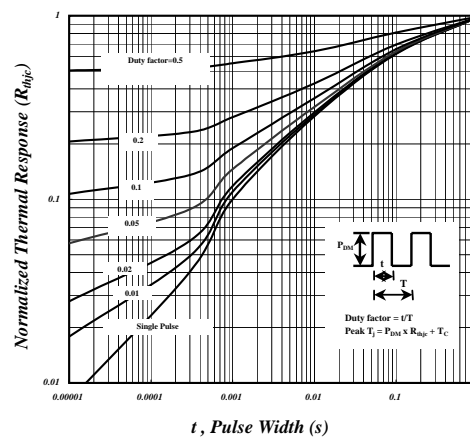


Fig 10. Effective Transient Thermal Impedance

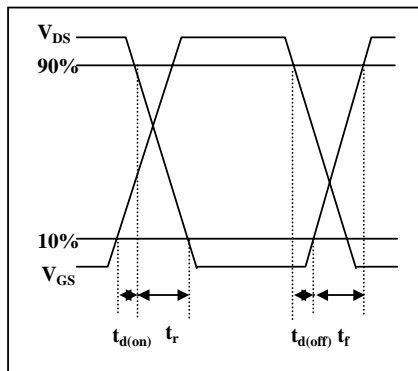


Fig 11. Switching Time Waveform

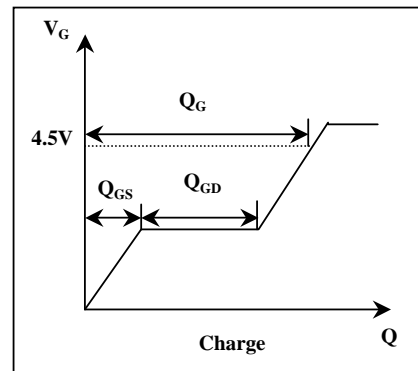


Fig 12. Gate Charge Waveform