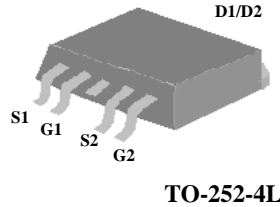


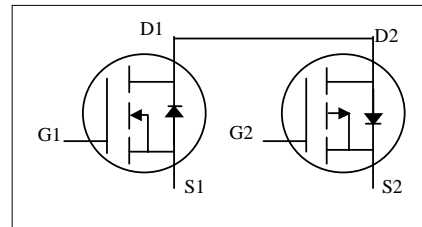
- ▼ Simple Drive Requirement
- ▼ Good Thermal Performance
- ▼ Fast Switching Performance



N-CH	BV_{DSS}	40V
	$R_{DS(ON)}$	30mΩ
	I_D	8A
P-CH	BV_{DSS}	-40V
	$R_{DS(ON)}$	36mΩ
	I_D	-7.3A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	+20	+20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current	30	-27	A
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	8.0	-7.3	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	6.3	-5.9	A
I_{DM}	Pulsed Drain Current ¹	40	-40	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	3.13		W
	Linear Derating Factor	0.025		W/°C
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c (N-CH)	Maximum Thermal Resistance, Junction-case ³	3.2	°C/W
Rthj-c (P-CH)	Maximum Thermal Resistance, Junction-case ³	3	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	40	°C/W



N-CH Electrical Characteristics @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.04	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =8A	-	-	30	mΩ
		V _{GS} =4.5V, I _D =5A	-	-	40	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =8A	-	18	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =40V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =32V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =+20V, V _{DS} =0V	-	-	+100	nA
Q _g	Total Gate Charge ²	I _D =8A	-	13	20.8	nC
Q _{gs}	Gate-Source Charge	V _{DS} =32V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	8	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =20V	-	8	-	ns
t _r	Rise Time	I _D =1A	-	5.5	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	23	-	ns
t _f	Fall Time	R _D =20Ω	-	6	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	960	1760	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	105	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	90	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.5	2.7	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =2.4A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ²	I _S =8A, V _{GS} =0V	-	20	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	14	-	nC

**P-CH Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=-1\text{mA}$	-	-0.03	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-7A$	-	-	36	$\text{m}\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	-	-	48	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-7A$	-	19	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=-32V, V_{GS}=0V$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-7A$	-	18	30	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-32V$	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	10	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-20V$	-	10	-	ns
t_r	Rise Time	$I_D=-1A$	-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-10V$	-	46	-	ns
t_f	Fall Time	$R_D=20\Omega$	-	30	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1360	2500	pF
C_{oss}	Output Capacitance	$V_{DS}=-25V$	-	155	-	pF
C_{riss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	140	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	7	13	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-2.4A, V_{GS}=0V$	-	-	-1.3	V
t_{rr}	Reverse Recovery Time ²	$I_S=-7A, V_{GS}=0V$	-	23	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	16	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. N-CH, P-CH are same.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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AP4563GH

N-Channel

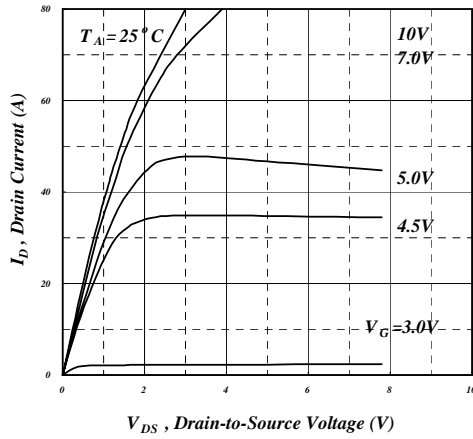


Fig 1. Typical Output Characteristics

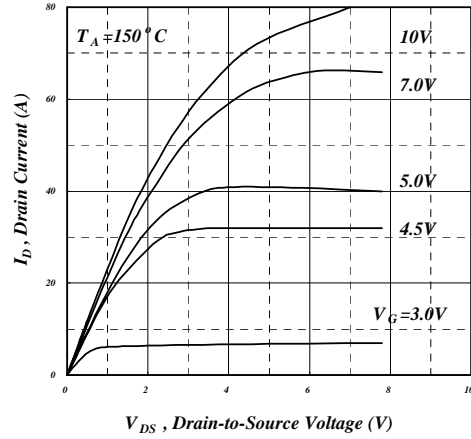


Fig 2. Typical Output Characteristics

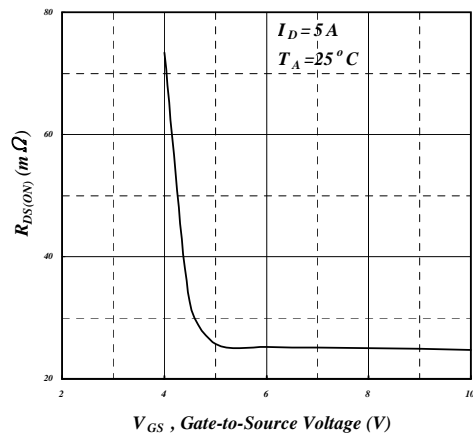


Fig 3. On-Resistance v.s. Gate Voltage

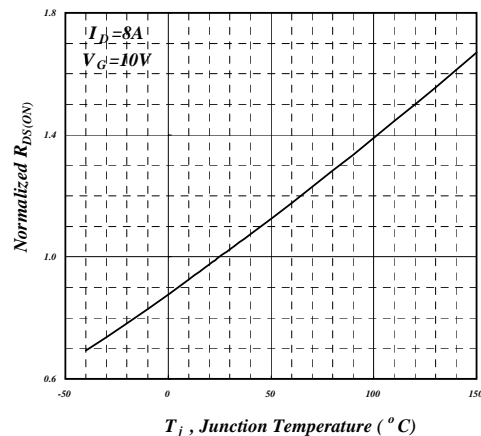


Fig 4. Normalized On-Resistance v.s. Junction Temperature

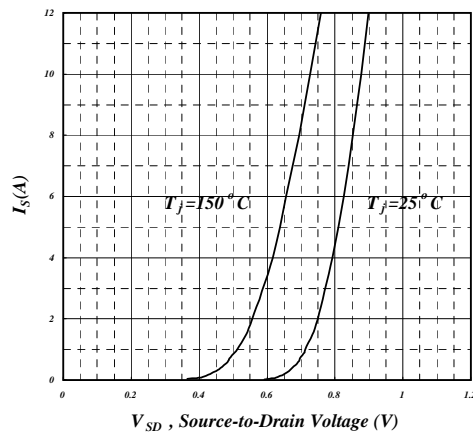


Fig 5. Forward Characteristic of Reverse Diode

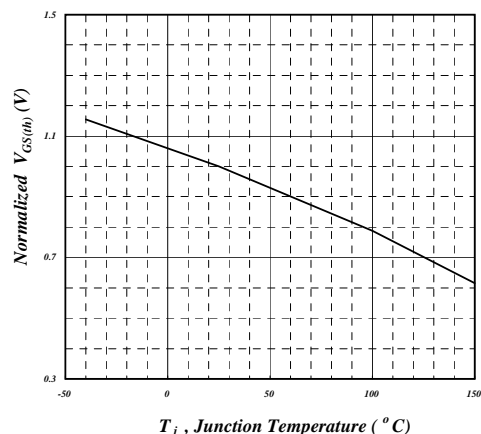


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

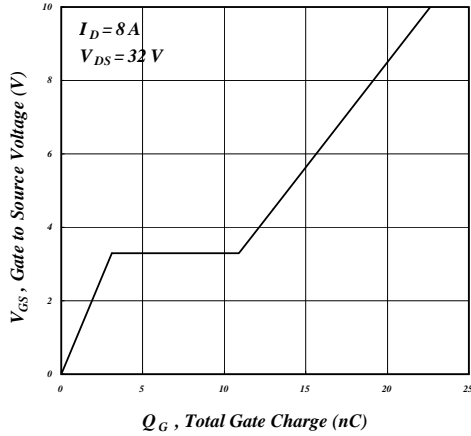


Fig 7. Gate Charge Characteristics

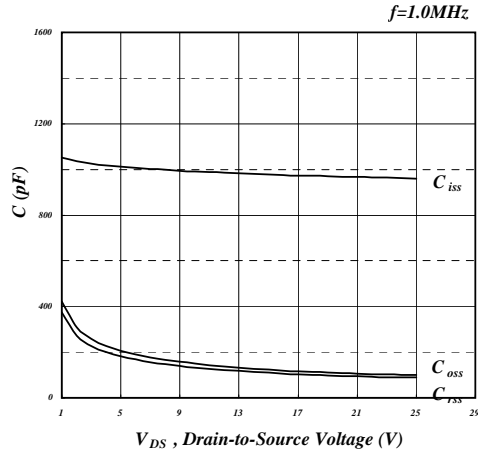


Fig 8. Typical Capacitance Characteristics

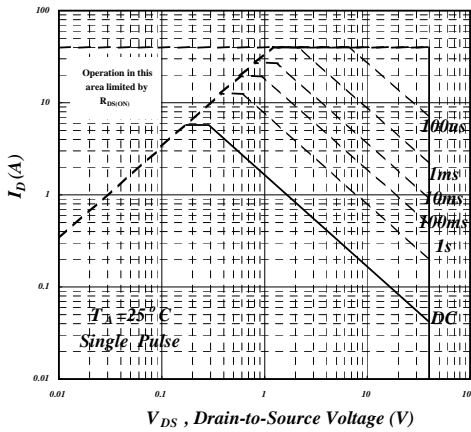


Fig 9. Maximum Safe Operating Area

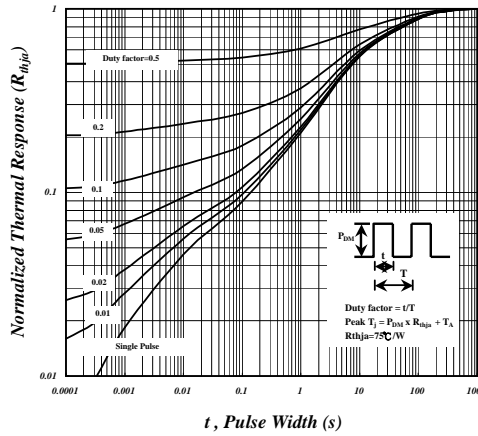


Fig 10. Effective Transient Thermal Impedance

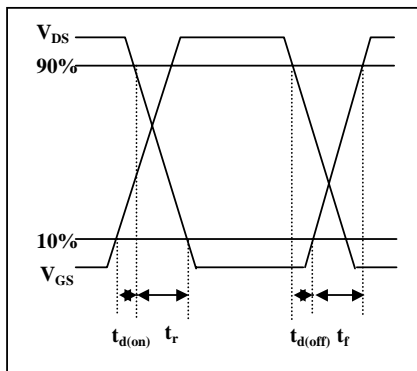


Fig 11. Switching Time Waveform

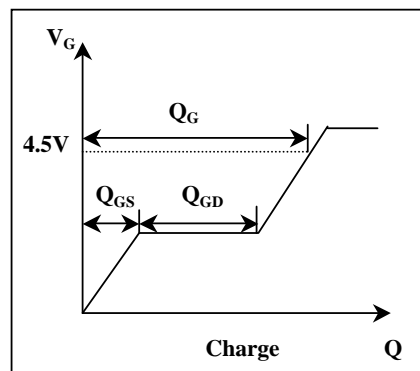


Fig 12. Gate Charge Waveform



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P-Channel

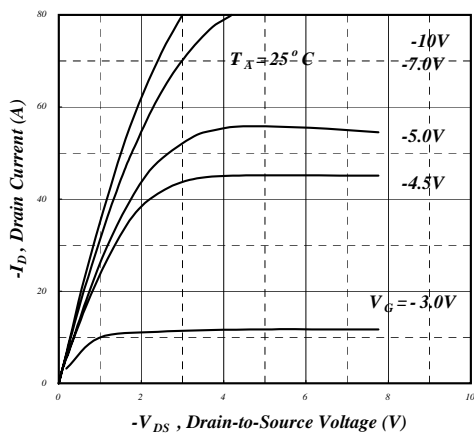


Fig 1. Typical Output Characteristics

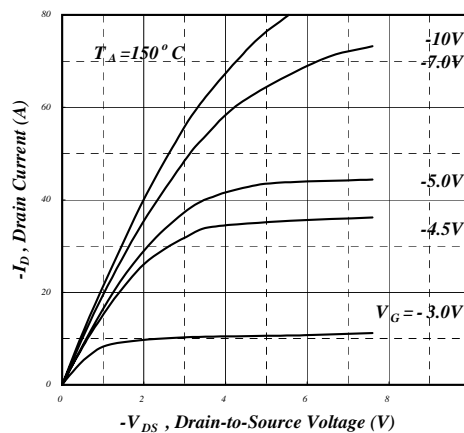


Fig 2. Typical Output Characteristics

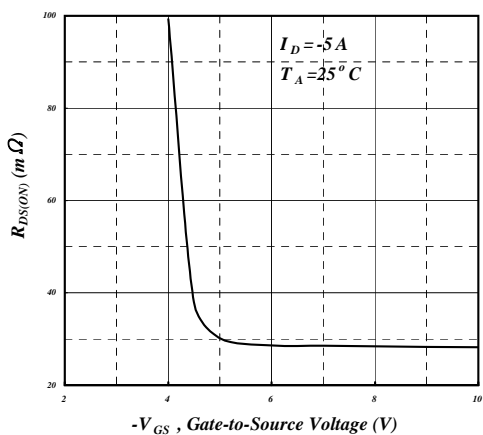


Fig 3. On-Resistance v.s. Gate Voltage

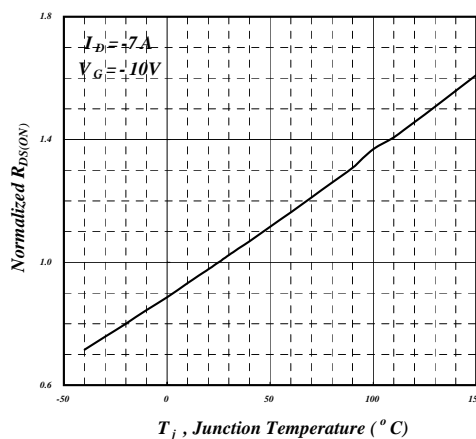


Fig 4. Normalized On-Resistance v.s. Junction Temperature

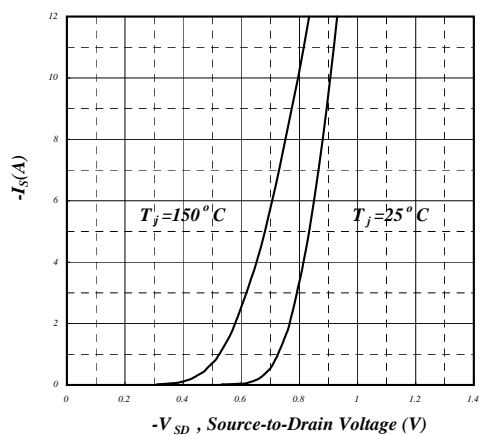


Fig 5. Forward Characteristic of Reverse Diode

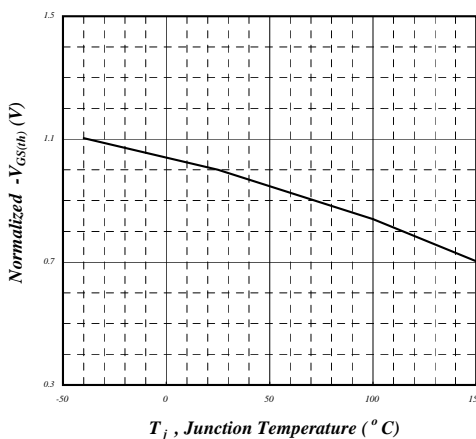


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

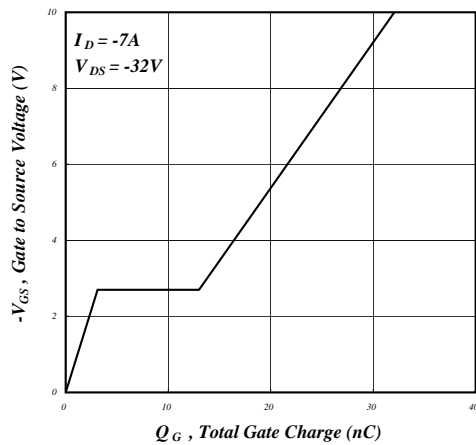


Fig 7. Gate Charge Characteristics

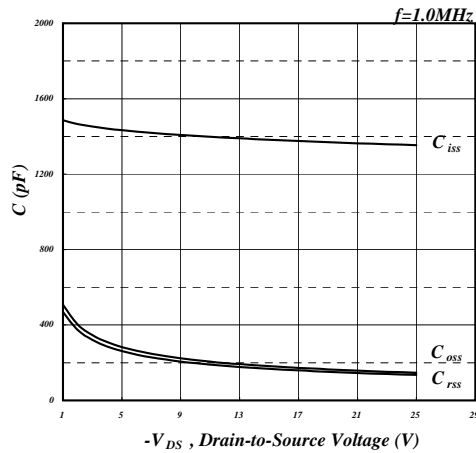


Fig 8. Typical Capacitance Characteristics

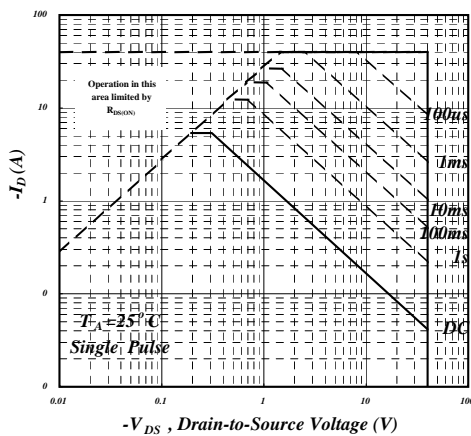


Fig 9. Maximum Safe Operating Area

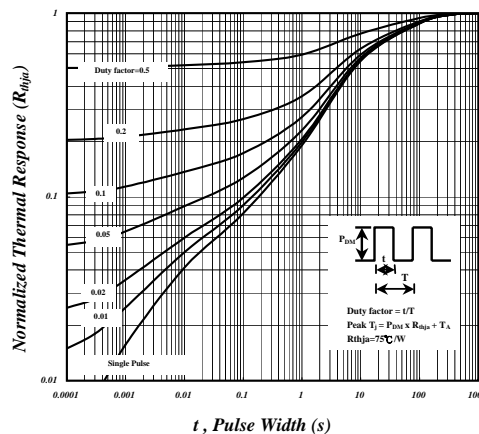


Fig 10. Effective Transient Thermal Impedance

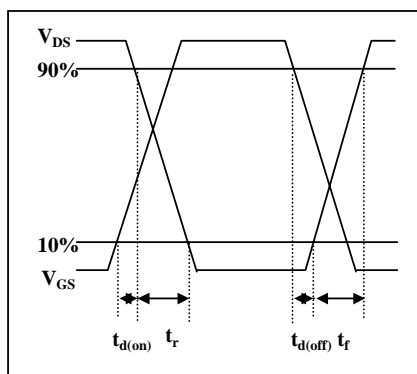


Fig 11. Switching Time Waveform

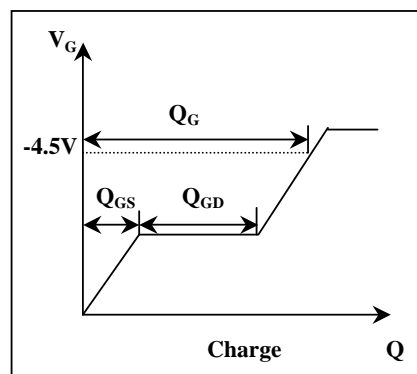


Fig 12. Gate Charge Waveform