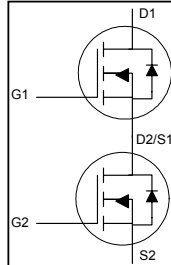




- ▼ Simple Drive Requirement
- ▼ Easy for Synchronous Buck Converter Application
- ▼ RoHS Compliant & Halogen-Free

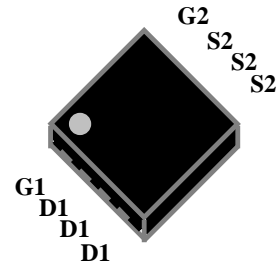
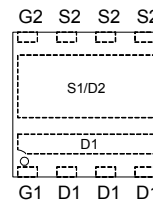


CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	18m Ω
	I_D	21A
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	10.5m Ω
	I_D	39A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.



PMPAK[®] 3 x 3

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current (Chip Limited)	21	39	A
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	8.3	11.8	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	6.6	9.5	A
I_{DM}	Pulsed Drain Current ¹	40	40	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ³	1.9	2.2	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	10	5	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	65	55	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ⁴	115	105	$^\circ C/W$



CH-1 Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =8A	-	14	18	mΩ
		V _{GS} =4.5V, I _D =5A	-	23.2	30	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.4	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =8A	-	14	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =8A	-	4.2	6.7	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	1.8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	1.9	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	6.5	-	ns
t _r	Rise Time	I _D =1A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	15	-	ns
t _f	Fall Time	V _{GS} =10V	-	3	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	450	720	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	70	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	50	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =8A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =8A, V _{GS} =0V,	-	13	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	6	-	nC

**CH-2 Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=11A$	-	8	10.5	m Ω
		$V_{GS}=4.5V, I_D=7A$	-	13.3	16.5	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.4	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=11A$	-	20	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V$	-	-	10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=11A$	-	7.5	12	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=15V$	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=15V$	-	9	-	ns
t_r	Rise Time	$I_D=1A$	-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	20	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	4	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	970	1550	pF
C_{oss}	Output Capacitance	$V_{DS}=15V$	-	120	-	pF
C_{riss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	80	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=11A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_S=11A, V_{GS}=0V,$	-	16	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	10	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$.
4. Surface mounted on min. copper pad of FR4 board, on steady-state

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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Channel-1

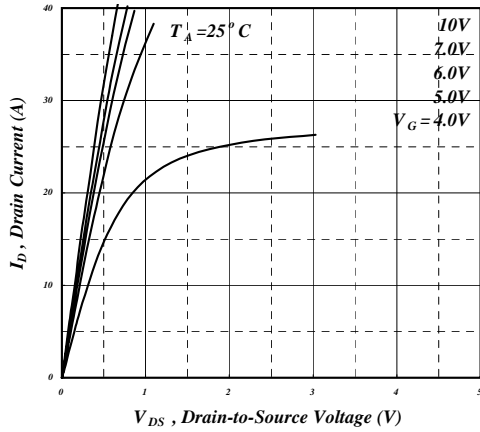


Fig 1. Typical Output Characteristics

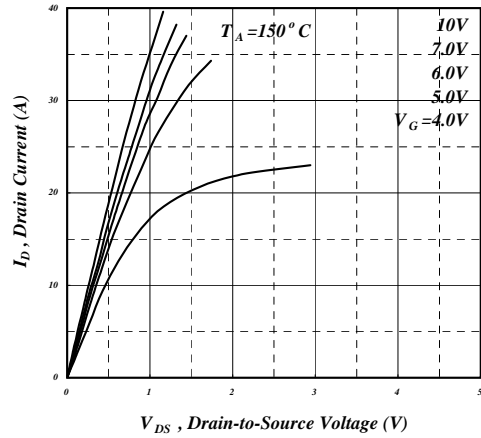


Fig 2. Typical Output Characteristics

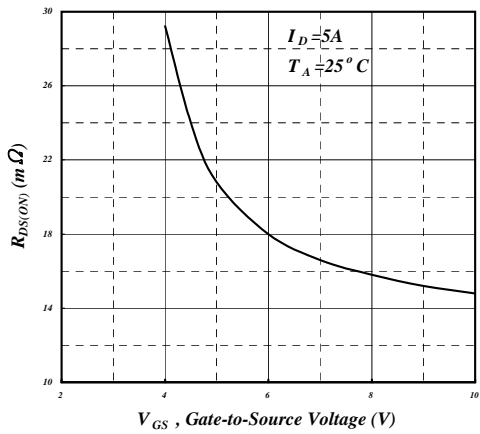


Fig 3. On-Resistance v.s. Gate Voltage

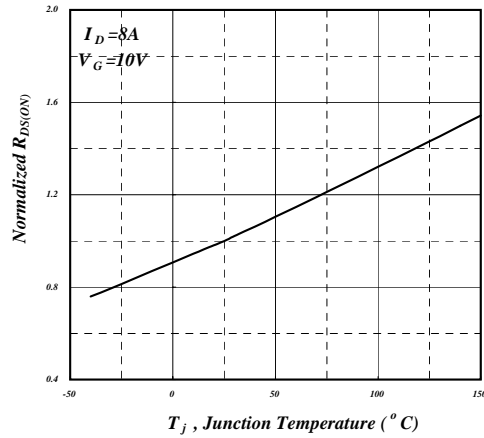


Fig 4. Normalized On-Resistance v.s. Junction Temperature

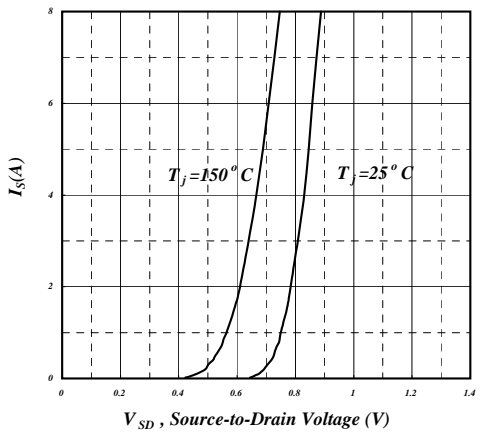


Fig 5. Forward Characteristic of Reverse Diode

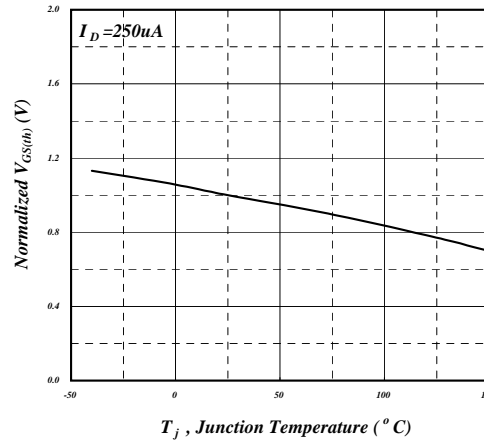


Fig 6. Gate Thresh. Voltage v.s. Junction Temperature

AP6950GYT-HF



Channel-1

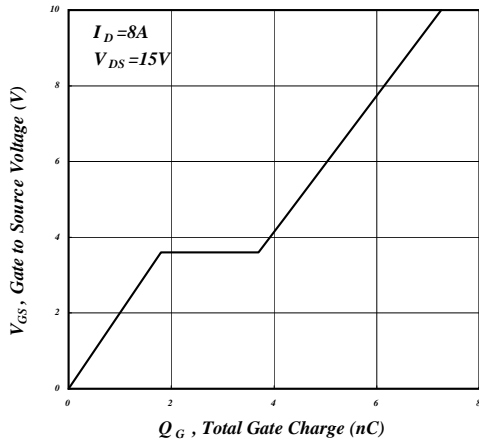


Fig 7. Gate Charge Characteristics

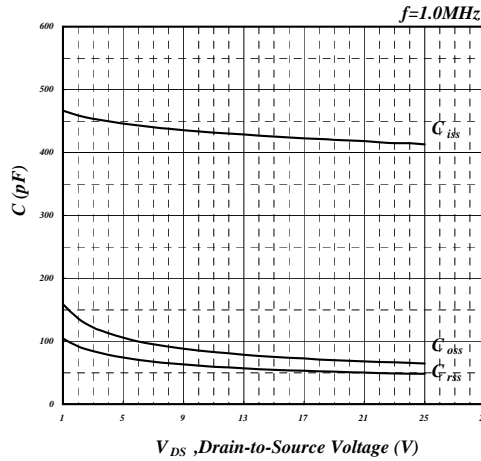


Fig 8. Typical Capacitance Characteristics

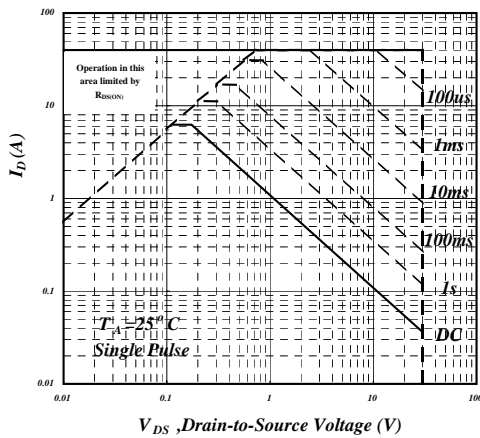


Fig 9. Maximum Safe Operating Area

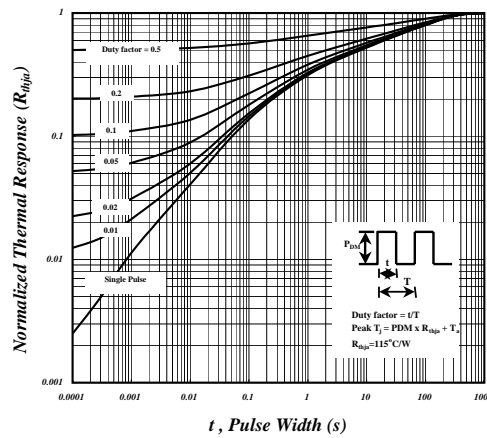


Fig 10. Effective Transient Thermal Impedance

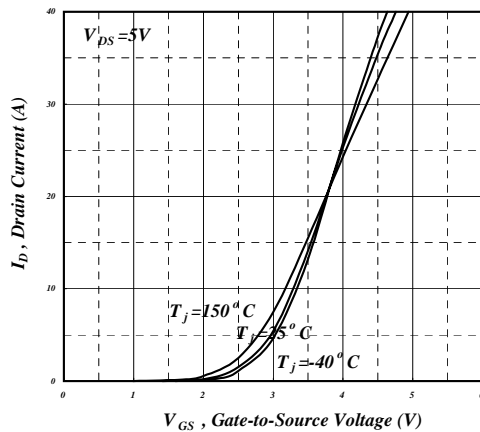


Fig 11. Transfer Characteristics

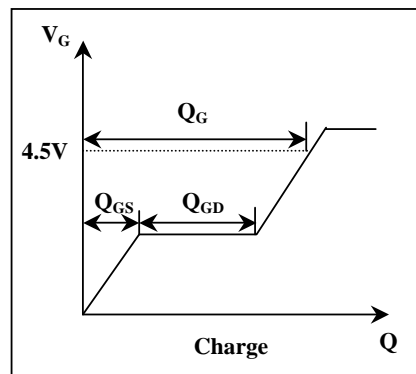


Fig 12. Gate Charge Waveform



Channel-2

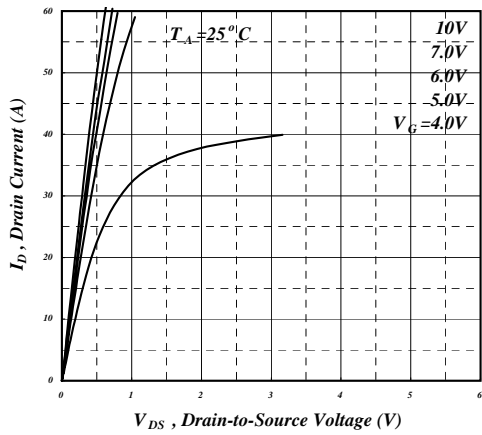


Fig 1. Typical Output Characteristics

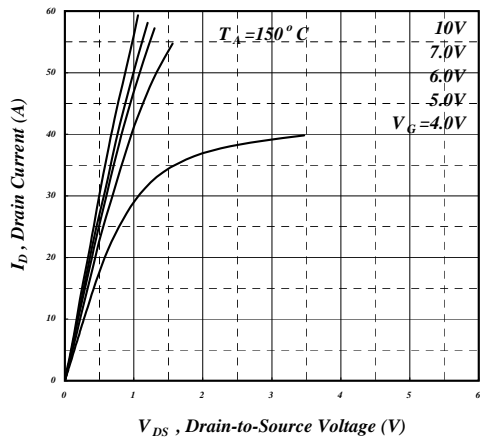


Fig 2. Typical Output Characteristics

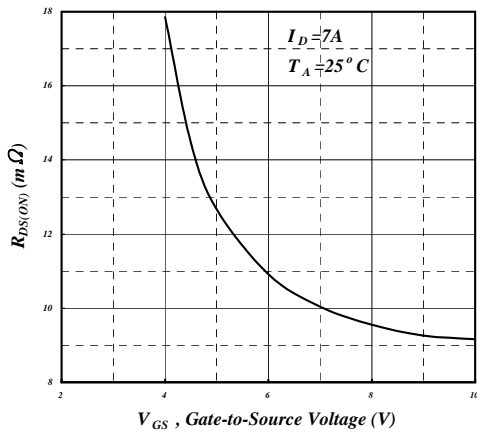


Fig 3. On-Resistance v.s. Gate Voltage

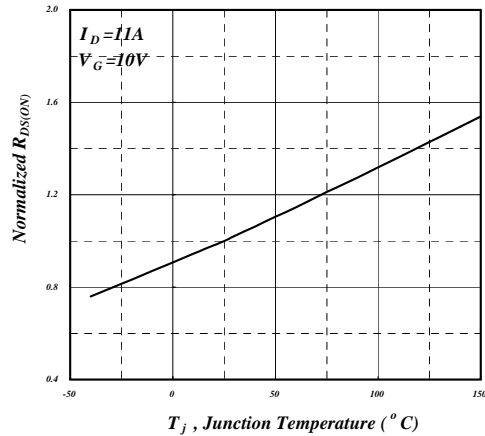


Fig 4. Normalized On-Resistance v.s. Junction Temperature

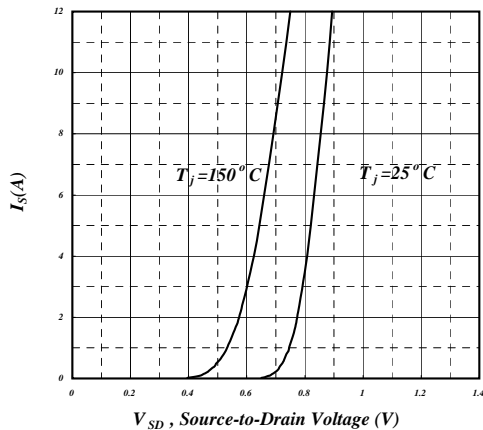


Fig 5. Forward Characteristic of Reverse Diode

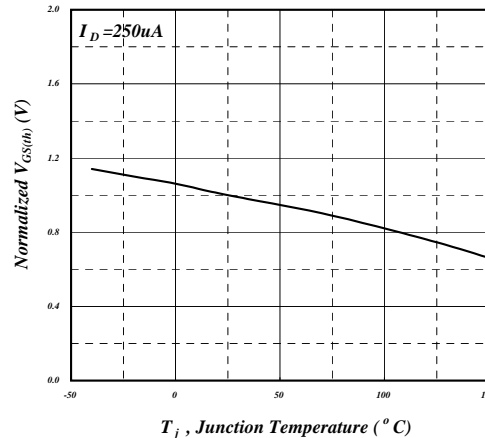


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



AP6950GYT-HF

Channel-2

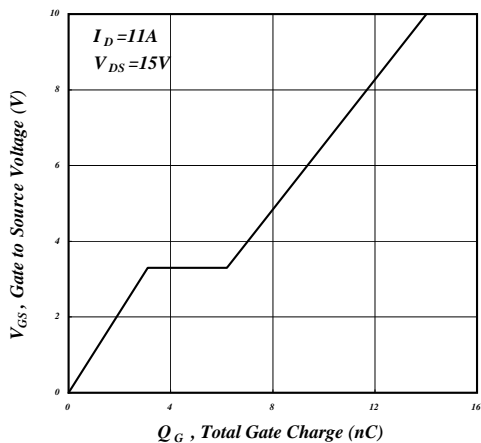


Fig 7. Gate Charge Characteristics

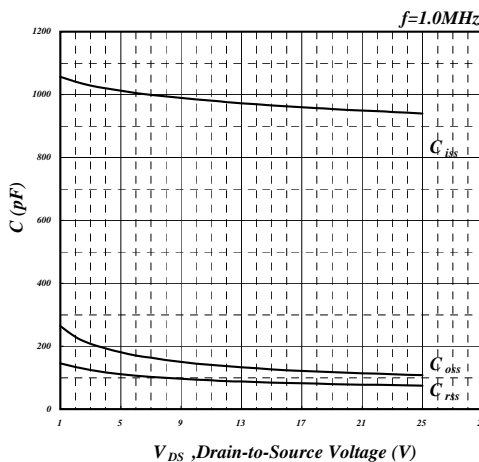


Fig 8. Typical Capacitance Characteristics

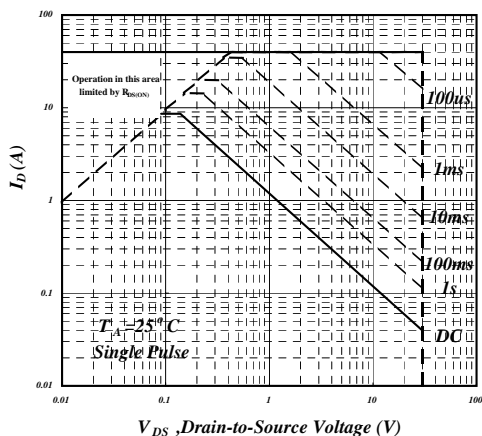


Fig 9. Maximum Safe Operating Area

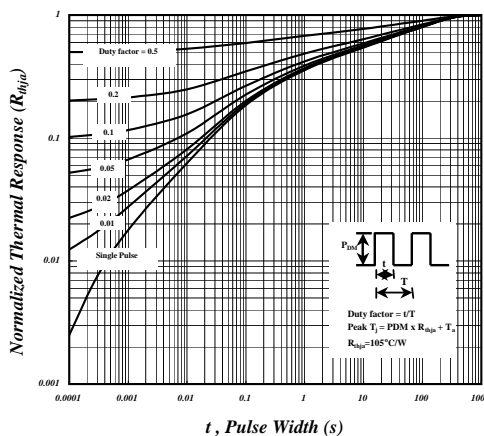


Fig 10. Effective Transient Thermal Impedance

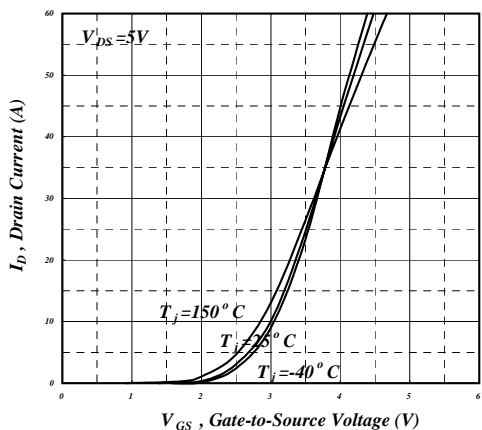


Fig 11. Transfer Characteristics

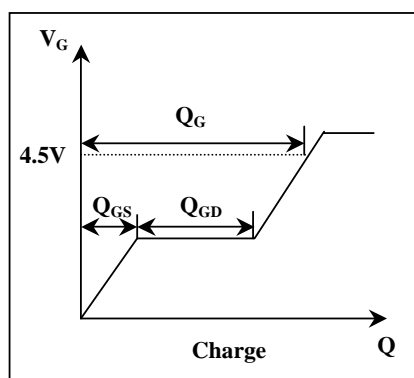


Fig 12. Gate Charge Waveform