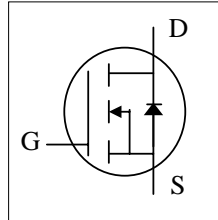




- ▼ Simple Drive Requirement
- ▼ SO-8 Compatible with Heatsink
- ▼ Low On-resistance
- ▼ RoHS Compliant

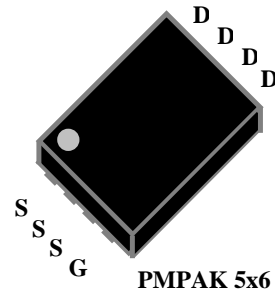


BV_{DSS}	30V
$R_{DS(ON)}$	3.3m Ω
I_D	105A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The PMPAK 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current (Chip)	105	A
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	31	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	25	A
I_{DM}	Pulsed Drain Current ¹	250	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	56.8	W
$P_D@T_A=25^\circ C$	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy ⁴	28.8	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	2.2	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	25	$^\circ C/W$



Electrical Characteristics @ $T_J=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	-	-	3.3	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	-	5	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=20A$	-	60	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=30A$	-	13.3	21	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=15V$	-	2.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	7.2	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=15V$	-	8	-	ns
t_r	Rise Time	$I_D=1A$	-	5.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	25	-	ns
t_f	Fall Time	$R_D=15\Omega$	-	17	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1400	2240	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	440	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	170	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.4	2.1	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=30A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=10A, V_{GS}=0V,$	-	35	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	32	-	nC

Notes:

1. Pulse width limited by Max. junction temperature
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$, 60°C/W at steady state.
4. Starting $T_J=25^{\circ}\text{C}$, $V_{DD}=25V$, $L=0.1\text{mH}$, $R_G=25\Omega$, $I_{AS}=24A$.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

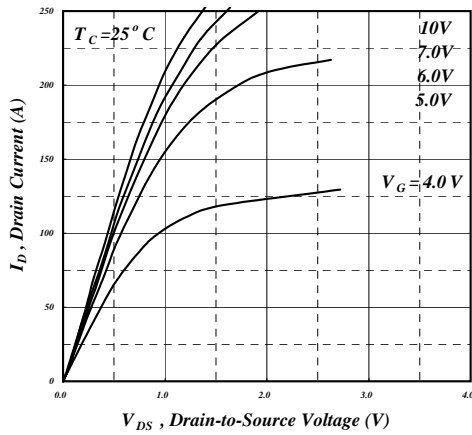


Fig 1. Typical Output Characteristics

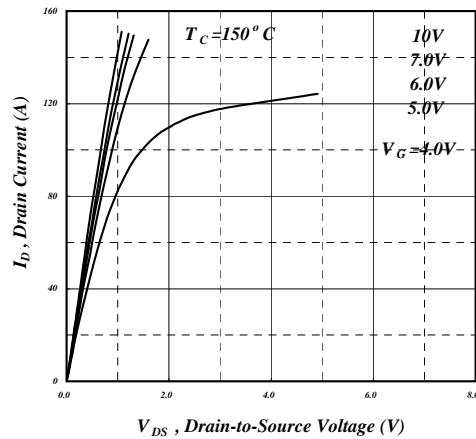


Fig 2. Typical Output Characteristics

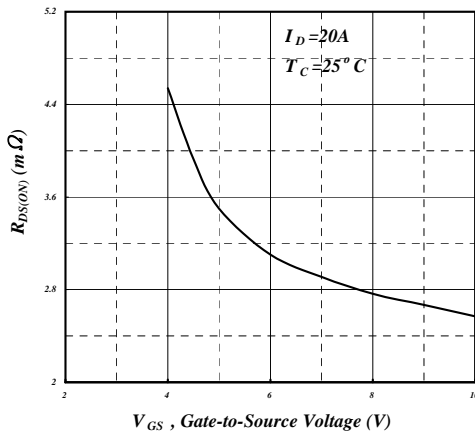


Fig 3. On-Resistance v.s. Gate Voltage

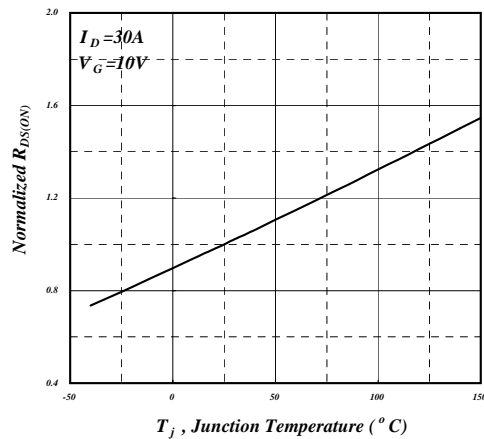


Fig 4. Normalized On-Resistance v.s. Junction Temperature

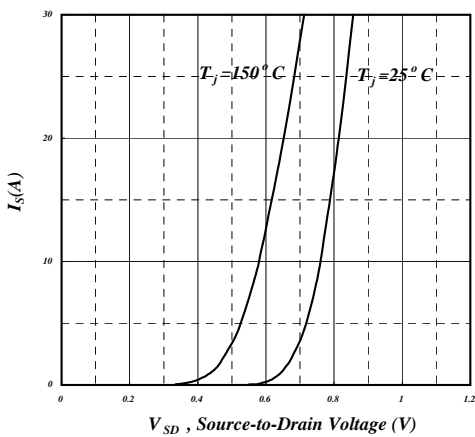


Fig 5. Forward Characteristic of Reverse Diode

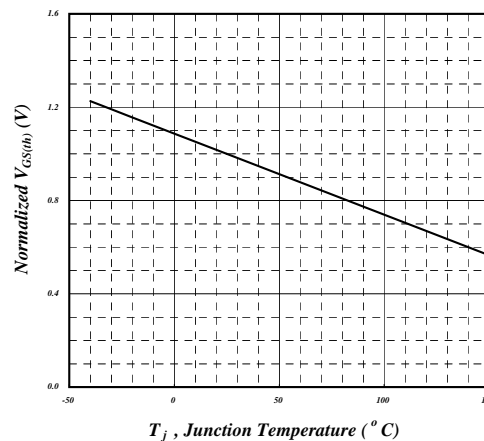


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

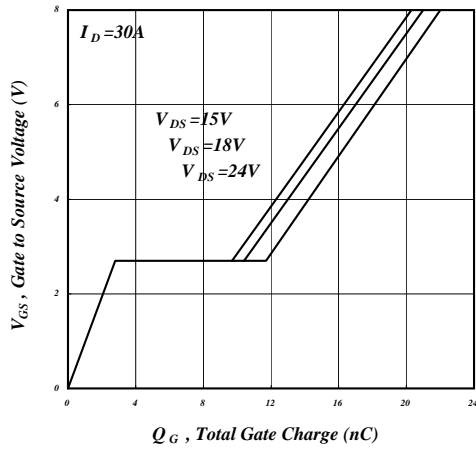


Fig 7. Gate Charge Characteristics

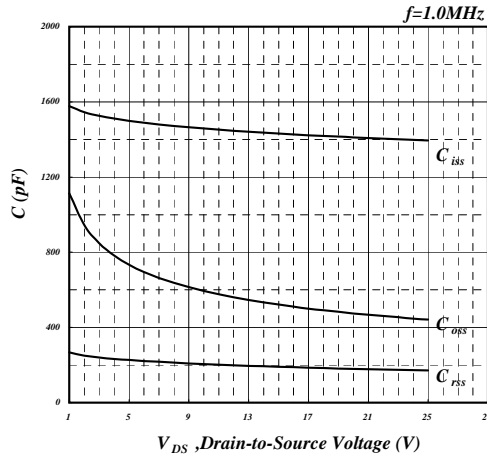


Fig 8. Typical Capacitance Characteristics

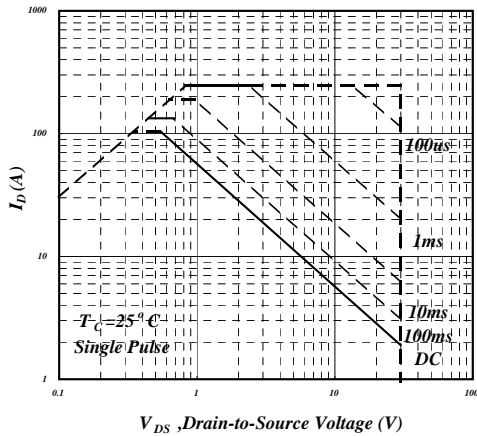


Fig 9. Maximum Safe Operating Area

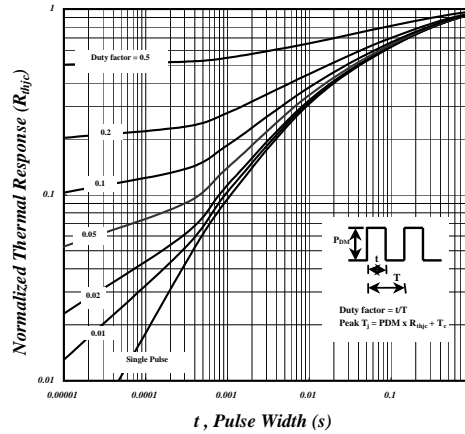


Fig 10. Effective Transient Thermal Impedance

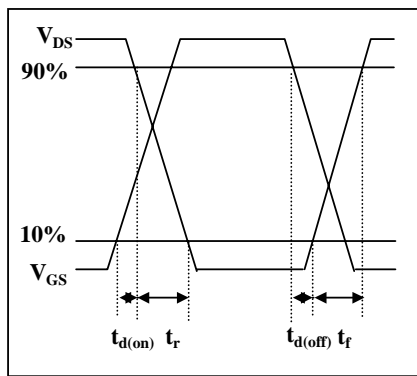


Fig 11. Switching Time Waveform

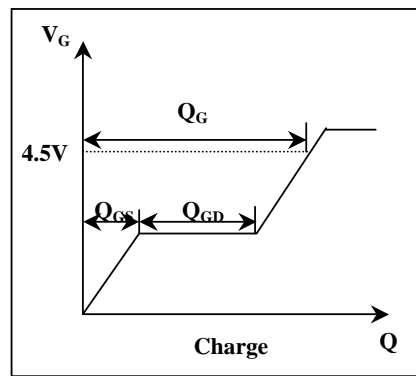


Fig 12. Gate Charge Waveform