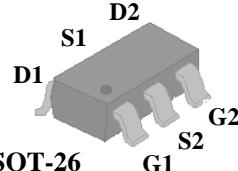




- ▼ Low Gate Charge
- ▼ Fast Switching Performance
- ▼ Surface Mount Package
- ▼ RoHS Compliant & Halogen-Free

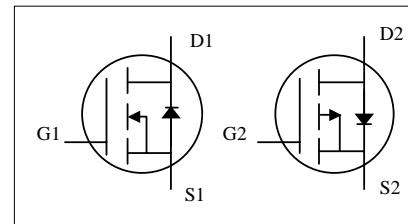


N-CH	BV_{DSS}	16V
	$R_{DS(ON)}$	150mΩ
	I_D	2.2A
P-CH	BV_{DSS}	-16V
	$R_{DS(ON)}$	320mΩ
	I_D	-1.5A

Description

Advanced Power MOSFETs utilized advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device.

The SOT-26 package is widely used for commercial surface mount applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	16	-16	V
V_{GS}	Gate-Source Voltage	± 8	± 8	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current ³	2.2	-1.5	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current ³	1.8	-1.2	A
I_{DM}	Pulsed Drain Current ¹	8.0	-6.0	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	1.14		W
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	110	°C/W



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N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	16	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =2A	-	-	150	mΩ
		V _{GS} =2.5V, I _D =1.5A	-	-	230	mΩ
		V _{GS} =1.8V, I _D =0.5A	-	-	450	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.2	-	1	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =2A	-	8	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =12V, V _{GS} =0V	-	-	1	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±8V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =2A	-	6.5	10.4	nC
Q _{gs}	Gate-Source Charge	V _{DS} =10V	-	0.5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge		-	1.5	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =10V	-	8	-	ns
t _r	Rise Time		-	15	-	ns
t _{d(off)}	Turn-off Delay Time		-	18	-	ns
t _f	Fall Time	V _{GS} =5V	-	4	-	ns
C _{iss}	Input Capacitance		-	350	560	pF
C _{oss}	Output Capacitance		-	70	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	60	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =0.9A, V _{GS} =0V	-	-	1.2	V

**P-CH Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-16	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-1.5\text{A}$	-	-	320	$\text{m}\Omega$
		$V_{\text{GS}}=-2.5\text{V}, I_{\text{D}}=-1\text{A}$	-	-	550	$\text{m}\Omega$
		$V_{\text{GS}}=-1.8\text{V}, I_{\text{D}}=-0.5\text{A}$	-	-	900	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-0.2	-	-1	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=-5\text{V}, I_{\text{D}}=-1\text{A}$	-	3.6	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=-12\text{V}, V_{\text{GS}}=0\text{V}$	-	-	-1	uA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=+8\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_{\text{D}}=-2\text{A}$	-	5.5	8.8	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=-10\text{V}$	-	0.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=-4.5\text{V}$	-	1.5	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time ²	$V_{\text{DS}}=-10\text{V}$	-	8	-	ns
t_r	Rise Time	$I_{\text{D}}=-1\text{A}$	-	17	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_{\text{G}}=3.3\Omega$	-	18	-	ns
t_f	Fall Time	$V_{\text{GS}}=-5\text{V}$	-	7	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	410	660	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=-16\text{V}$	-	60	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	45	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward On Voltage ²	$I_{\text{S}}=-0.9\text{A}, V_{\text{GS}}=0\text{V}$	-	-	-1.2	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t \leq 5sec ; 180°C/W when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



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N-Channel

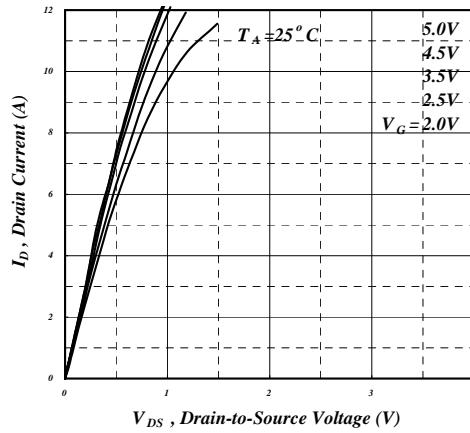


Fig 1. Typical Output Characteristics

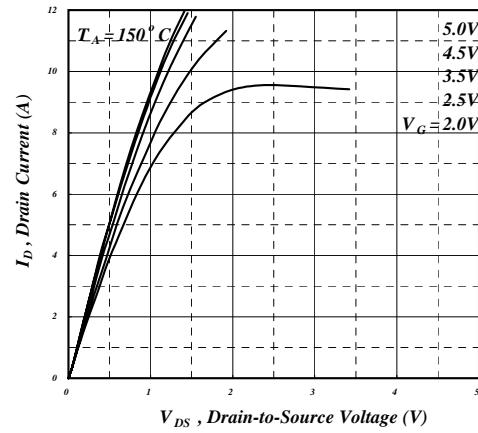


Fig 2. Typical Output Characteristics

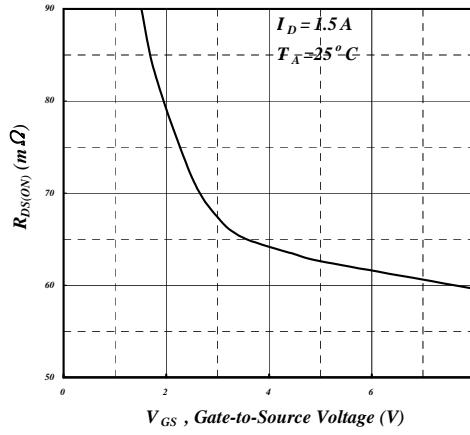


Fig 3. On-Resistance v.s. Gate Voltage

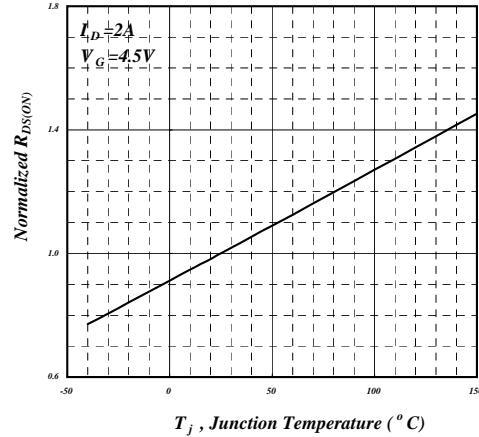


Fig 4. Normalized On-Resistance v.s. Junction Temperature

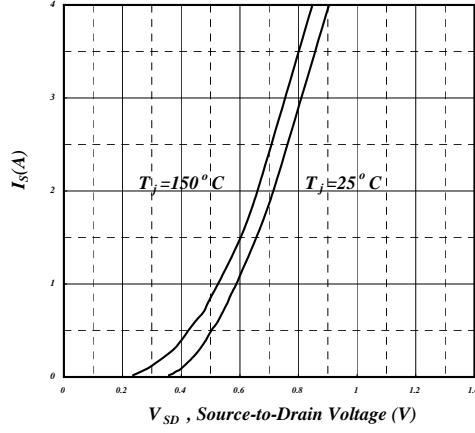


Fig 5. Forward Characteristic of Reverse Diode

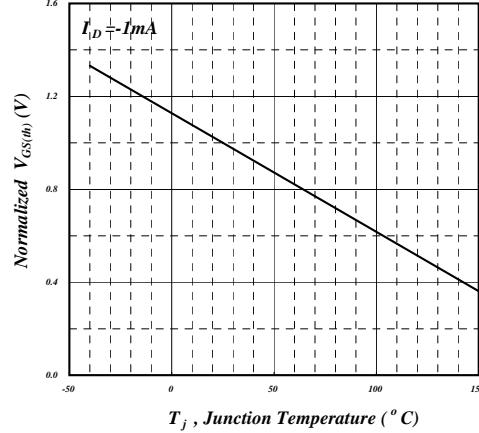


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

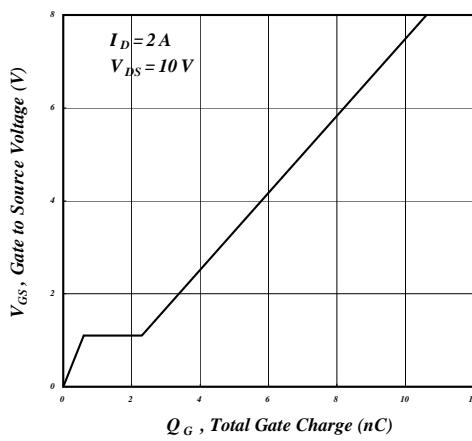


Fig 7. Gate Charge Characteristics

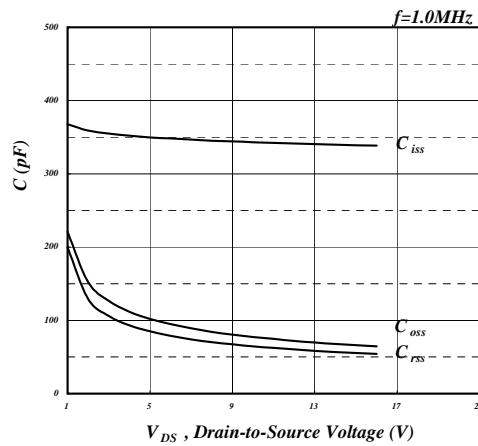


Fig 8. Typical Capacitance Characteristics

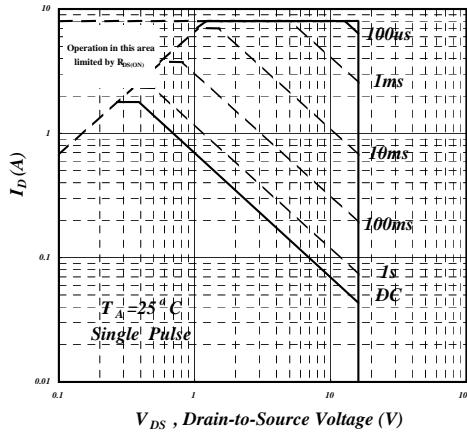


Fig 9. Maximum Safe Operating Area

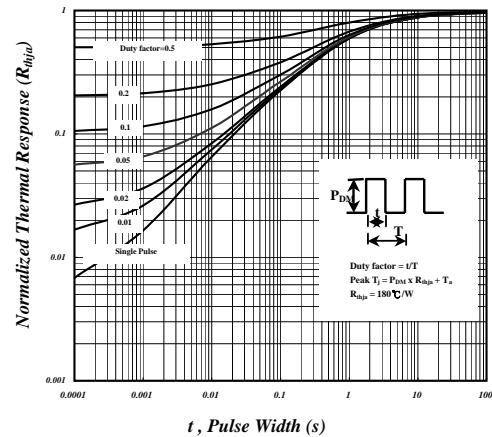


Fig 10. Effective Transient Thermal Impedance

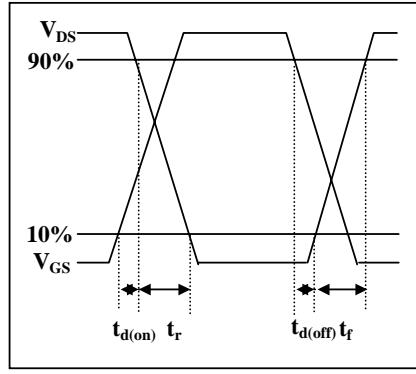


Fig 11. Switching Time Waveform

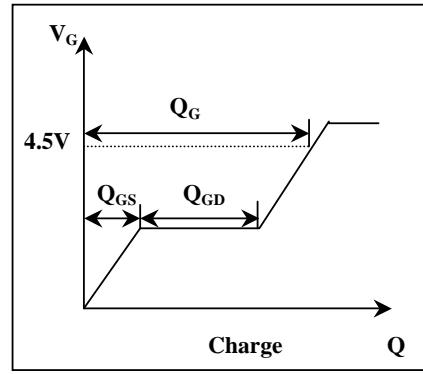


Fig 12. Gate Charge Waveform



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P-Channel

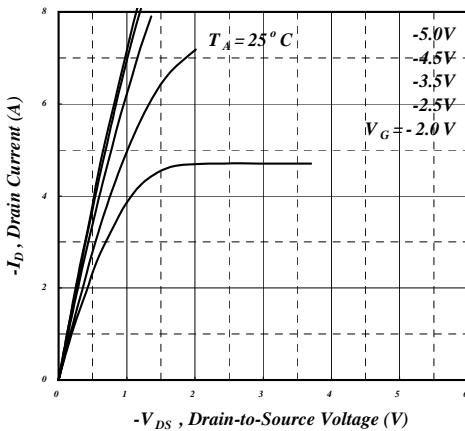


Fig 1. Typical Output Characteristics

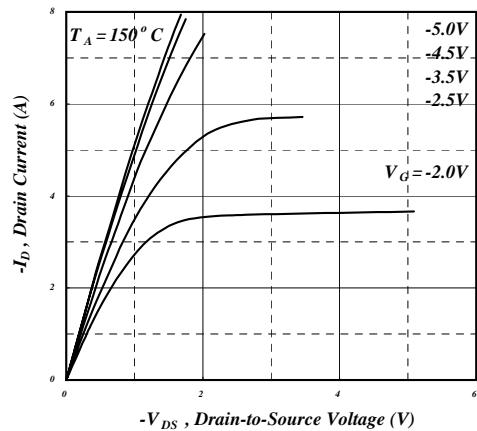


Fig 2. Typical Output Characteristics

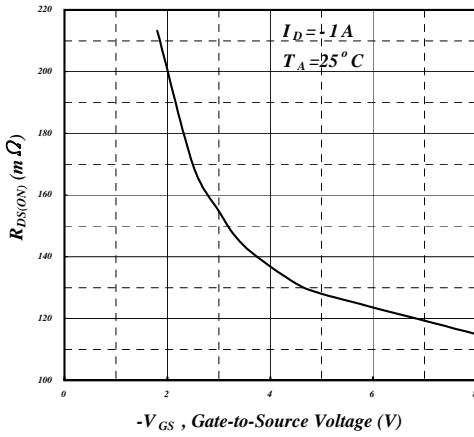


Fig 3. On-Resistance v.s. Gate Voltage

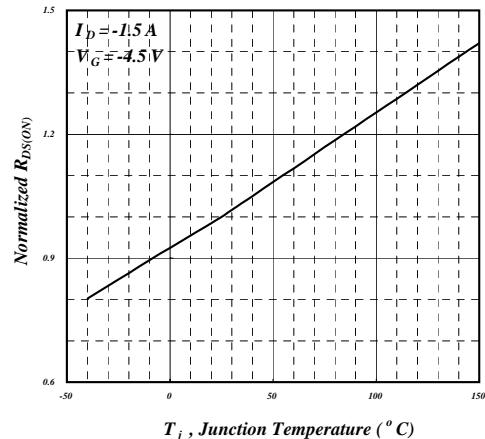


Fig 4. Normalized On-Resistance v.s. Junction Temperature

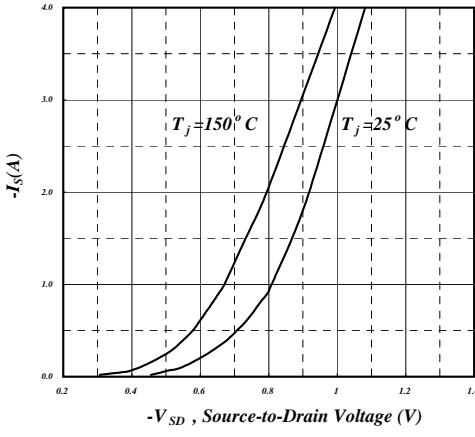


Fig 5. Forward Characteristic of Reverse Diode

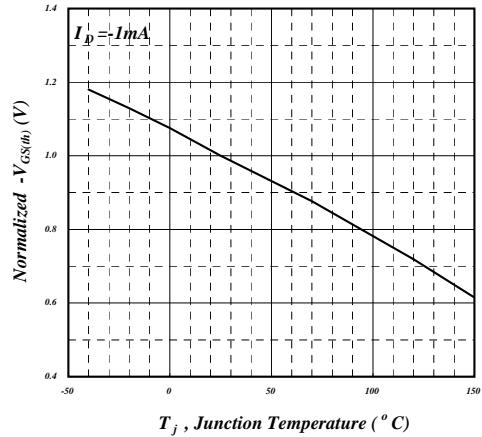


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

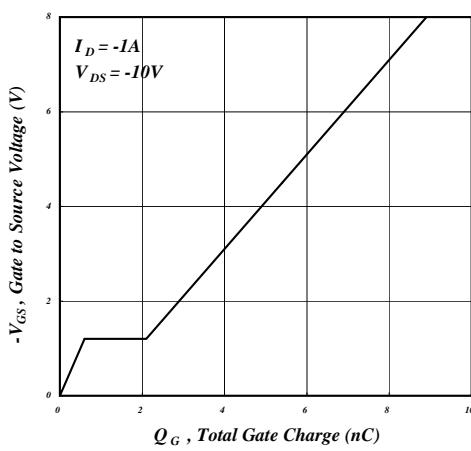


Fig 7. Gate Charge Characteristics

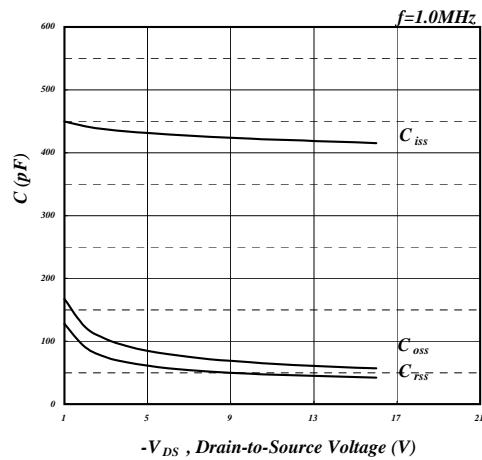


Fig 8. Typical Capacitance Characteristics

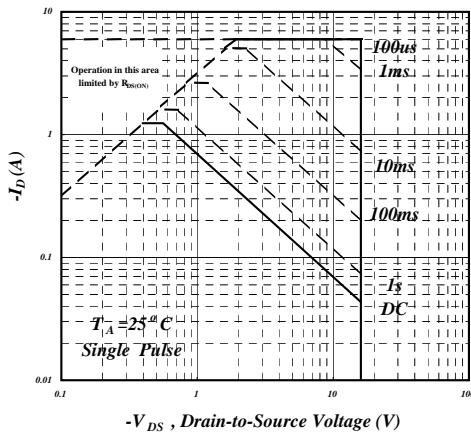


Fig 9. Maximum Safe Operating Area

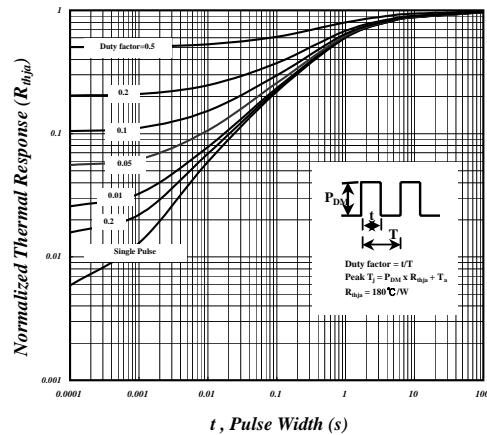


Fig 10. Effective Transient Thermal Impedance

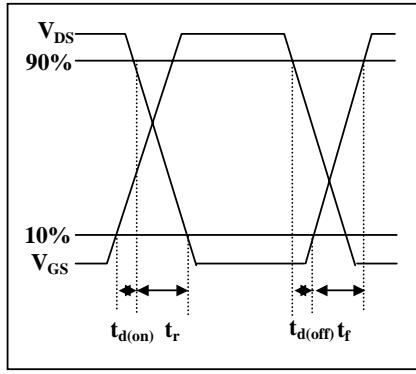


Fig 11. Switching Time Waveform

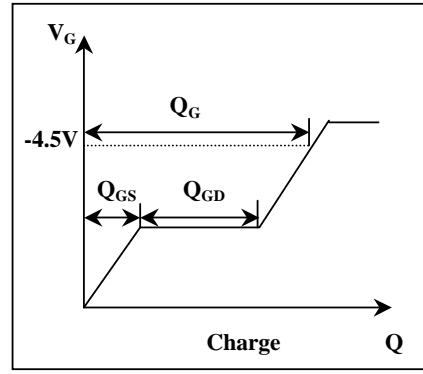


Fig 12. Gate Charge Waveform