19-1991; Rev 0; 4/01

EVALUATION KIT AVAILABLE

Quad LVDS Line Driver

MAX9124

General Description

The MAX9124 quad low-voltage differential signaling (LVDS) line driver is ideal for applications requiring high data rates, low power, and low noise. The MAX9124 is guaranteed to transmit data at speeds up to 800Mbps (400MHz) over controlled impedance media of approximately 100Ω. The transmission media may be printed circuit (PC) board traces, backplanes, or cables.

The MAX9124 accepts four LVTTL/LVCMOS input levels and translates them to LVDS output signals. Moreover, the MAX9124 is capable of setting all four outputs to a high-impedance state through two enable inputs, EN and $\overline{EN}$, thus dropping the device to an ultra-low-power state of 16mW (typ) during high impedance. The enables are common to all four transmitters. Outputs conform to the ANSI TIA/EIA-644 LVDS standard.

The MAX9124 operates from a single +3.3V supply and is specified for operation from -40°C to +85°C. It is available in 16-pin TSSOP and SO packages. Refer to the MAX9125/MAX9126 data sheet for quad LVDS line receivers.

Features

- ♦ **Pin Compatible with DS90LV031A**
- ♦ **Guaranteed 800Mbps Data Rate**
- ♦ **250ps Maximum Pulse Skew**
- ♦ **Conforms to TIA/EIA-644 LVDS Standard**
- ♦ **Single +3.3V Supply**
- ♦ **16-Pin TSSOP and SO Packages**

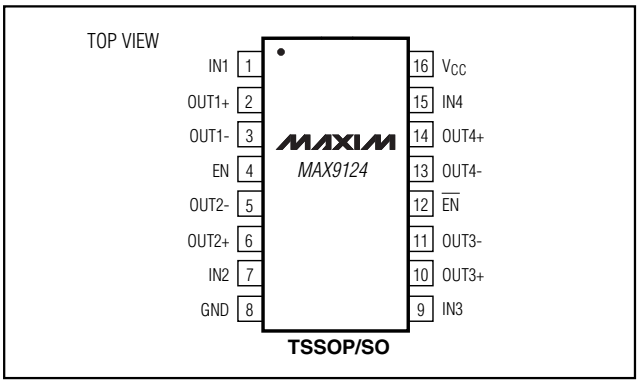
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9124EUE	-40°C to +85°C	16 TSSOP
MAX9124ESE	-40°C to +85°C	16 SO

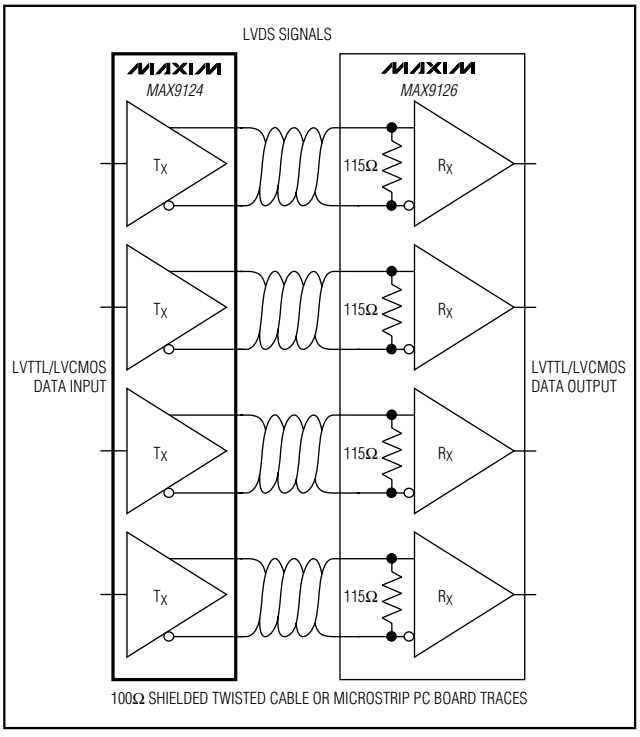
Applications

- Digital Copiers
- Laser Printers
- Cell Phone Base Stations
- Add/Drop Muxes
- Digital Cross-Connects
- DSLAMs
- Network Switches/Routers
- Backplane Interconnect
- Clock Distribution

Pin Configuration



Typical Applications Circuit



** Future product—contact factory for availability.*

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN_, EN, $\overline{EN}$ to GND.....-0.3V to (V_{CC} + 0.3V)
OUT_+, OUT_- to GND.....-0.3V to +3.9V
Short-Circuit Duration (OUT_+, OUT_-) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
16-Pin SO (derate 8.7mW/°C above +70°C).....696mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C
ESD Protection
Human Body Model, OUT_+, OUT_- .....±6kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS OUTPUT (OUT_+, OUT_-)						
Differential Output Voltage	V_{OD}	Figure 1	250	368	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1		1	25	mV
Offset Voltage	V_{OS}	Figure 1	1.125	1.25	1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1		4	25	mV
Output High Voltage	V_{OH}				1.6	V
Output Low Voltage	V_{OL}		0.90			V
Differential Output Short-Circuit Current (Note 3)	I_{OSD}	Enabled, V_{OD} = 0			-9	mA
Output Short-Circuit Current	I_{OS}	OUT_+ = 0 at IN_ = V_{CC} or OUT_- = 0 at IN_ = 0, enabled		-3.8	-9	mA
Output High-Impedance Current	I_{OZ}	EN = low and $\overline{EN}$ = high, OUT_+ = 0 or V_{CC}, OUT_- = 0 or V_{CC} , R_L = ∞	-10		10	µA
Power-Off Output Current	I_{OFF}	V_{CC} = 0 or open, OUT_+ = 0 or 3.6V, OUT_- = 0 or 3.6V, R_L = ∞	-10		10	µA
INPUTS (IN_, EN, $\overline{EN}$)						
High-Level Input Voltage	V_{IH}		2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}		GND		0.8	V
Input Current	I_{IN}	IN_, EN, $\overline{EN}$ = 0 or V_{CC}	-20		20	µA
SUPPLY CURRENT						
No-Load Supply Current	I_{CC}	R_L = ∞, IN_ = V_{CC} or 0 for all channels		9.2	11	mA
Loaded Supply Current	I_{CCL}	R_L = 100Ω, IN_ = V_{CC} or 0 for all channels		22.7	30	mA
Disabled Supply Current	I_{CCZ}	Disabled, IN_ = V_{CC} or 0 for all channels, EN = 0, $\overline{EN}$ = V_{CC}		4.9	6	mA

SWITCHING CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 10pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 4, 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	Figures 2 and 3	0.8	1.42	2.0	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figures 2 and 3	0.8	1.44	2.0	ns
Differential Pulse Skew (Note 7)	t_{SKD1}	Figures 2 and 3		0.02	0.25	ns
Differential Channel-to-Channel Skew (Note 8)	t_{SKD2}	Figures 2 and 3			0.35	ns
Differential Part-to-Part Skew (Note 9)	t_{SKD3}	Figures 2 and 3			0.8	ns
Differential Part-to-Part Skew (Note 10)	t_{SKD4}	Figures 2 and 3			1.2	ns
Rise Time	t_{TLH}	Figures 2 and 3	0.1	0.35	0.7	ns
Fall Time	t_{THL}	Figures 2 and 3	0.1	0.35	0.7	ns
Disable Time High to Z	t_{PHZ}	Figures 4 and 5			5	ns
Disable Time Low to Z	t_{PLZ}	Figures 4 and 5			5	ns
Enable Time Z to High	t_{PZH}	Figures 4 and 5			5	ns
Enable Time Z to Low	t_{PZL}	Figures 4 and 5			5	ns
Maximum Operating Frequency (Note 11)	f_{MAX}		400			MHz

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.

Note 2: Currents into the device are positive, and current out of the device is negative. All voltages are referenced to ground except V_{OD}.

Note 3: Guaranteed by correlation data.

Note 4: AC parameters are guaranteed by design and characterization.

Note 5: C_L includes probe and jig capacitance.

Note 6: Signal generator conditions for dynamic tests: V_{OL} = 0, V_{OH} = 3V, f = 100MHz, 50% duty cycle, R_O = 50Ω, $t_R \le$ 1ns, $t_F \le$ 1ns (0% to 100%).

Note 7: t_{SKD1} is the magnitude difference of differential propagation delay. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 8: t_{SKD2} is the magnitude difference of t_{PHLD} or t_{PLHD} of one channel to the t_{PHLD} or t_{PLHD} of another channel on the same device.

Note 9: t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.

Note 10: t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

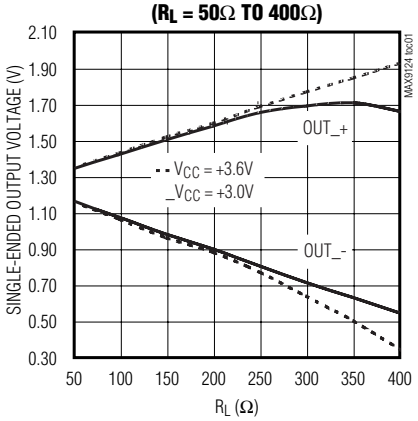
Note 11: f_{MAX} signal generator conditions: V_{OL} = 0, V_{OH} = 3V, f = 400MHz, 50% duty cycle, R_O = 50Ω, $t_R \le$ 1ns, $t_F \le$ 1ns (0% to 100%). Transmitter output criteria: duty cycle = 45% to 55%, $V_{OD} \ge$ 250mV.

Quad LVDS Line Driver

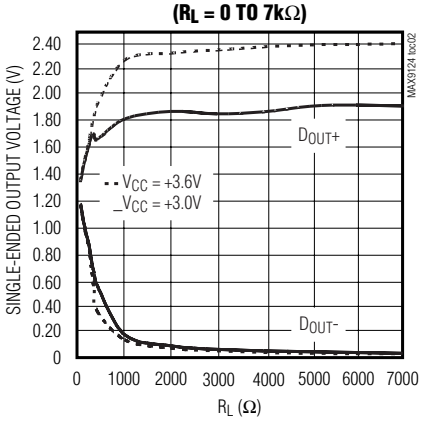
Typical Operating Characteristics

(T_A = +25°C)

SINGLE-ENDED OUTPUT VOLTAGE vs. LOAD RESISTANCE (R_L = 50Ω TO 400Ω)



SINGLE-ENDED OUTPUT VOLTAGE vs. LOAD RESISTANCE (R_L = 0 TO 7kΩ)



Pin Description

PIN	NAME	FUNCTION
1, 7, 9, 15	IN_	LVTTL/LVCMOS Driver Inputs
2, 6, 10, 14	OUT_+	Noninverting LVDS Driver Outputs
3, 5, 11, 13	OUT_-	Inverting LVDS Driver Outputs
4, 12	EN, $\overline{EN}$	Driver Enable Inputs. The driver is disabled and in high impedance when EN is low and $\overline{EN}$ is high. For other combinations of EN and $\overline{EN}$, the outputs are active.
8	GND	Ground
16	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF ceramic capacitors.

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9124 is an 800Mbps quad differential LVDS driver that is designed for high-speed, point-to-point, and low-power applications. This device accepts LVTTL/LVCMOS input levels and translates them to LVDS output signals.

The MAX9124 generates a 2.5mA to 4.0mA output current using a current-steering configuration. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited and enter a high-impedance state when the device is not powered or is disabled.

The current-steering architecture of the MAX9124 requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver. Logic states are determined by the direction of current flow through the termination resistor. With a typical 3.7mA output current, the MAX9124 produces an output voltage of 370mV when driving a 100Ω load.

Termination

Because the MAX9124 is a current-steering device, no output voltage will be generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels depend upon the value of the termination resistor. The MAX9124 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90Ω and 132Ω, depending on the characteristic impedance of the transmission medium.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Table 1. Input/Output Function Table

ENABLES		INPUTS	OUTPUTS	
EN	$\overline{EN}$	IN_	OUT_+	OUT_ -
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Differential Traces

Output trace characteristics affect the performance of the MAX9124. Use controlled-impedance traces to match trace impedance to the transmission medium. Eliminate reflections and ensure that noise couples as common mode by running the differential trace pairs close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a nominal differential impedance of 100Ω. To minimize impedance discontinuities, use cables and connectors that have matched differential impedance.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the LVTTL/LVCMOS and LVDS signals from each other to prevent coupling.

Chip Information

TRANSISTOR COUNT: 2007

PROCESS: CMOS

Quad LVDS Line Driver

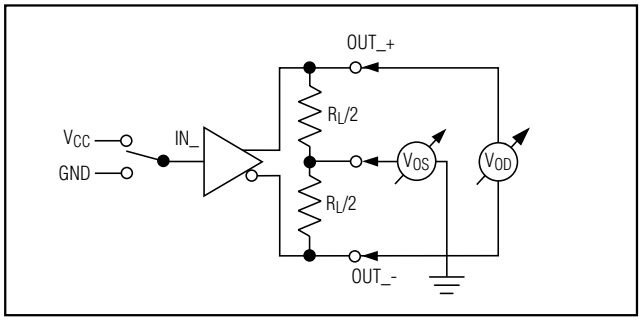


Figure 1. Driver V_{OD} and V_{OS} Test Circuit

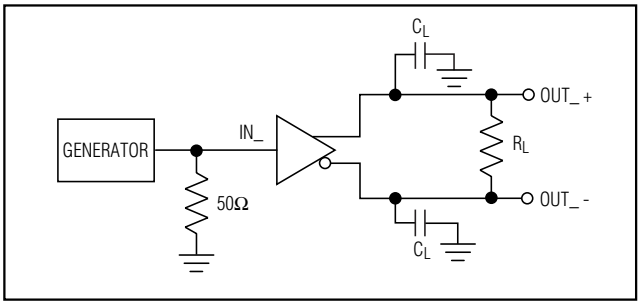


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

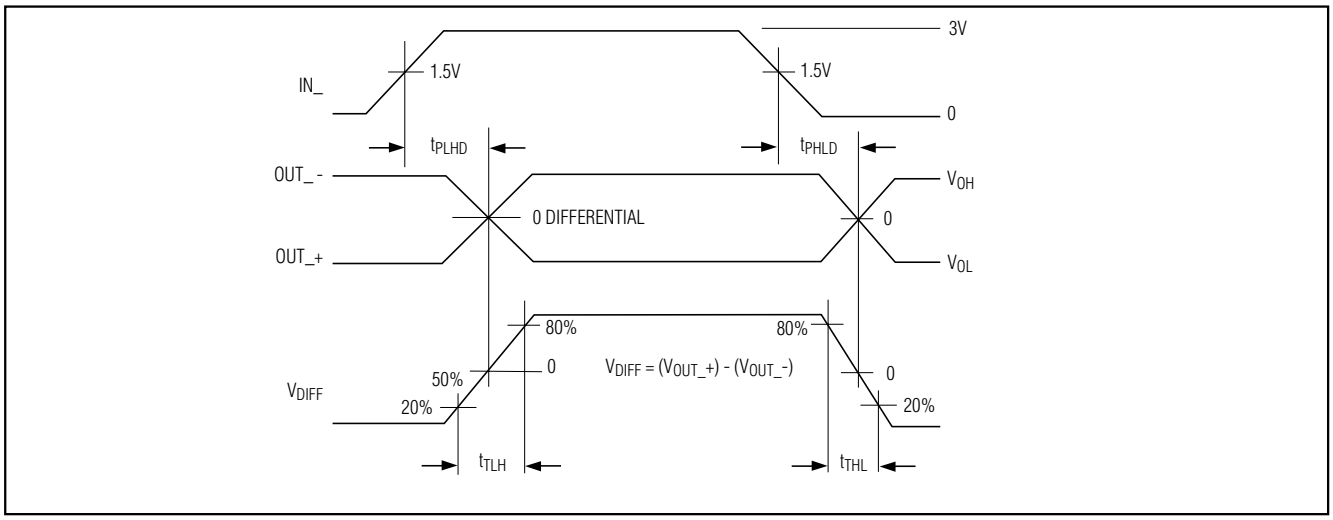


Figure 3. Driver Propagation Delay and Transition Time Waveforms

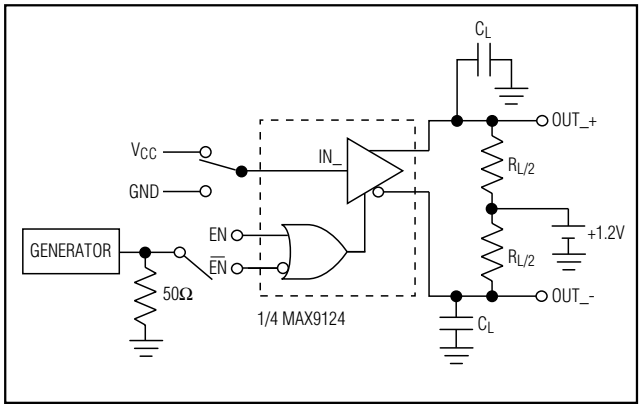


Figure 4. Driver High-Impedance Delay Test Circuit

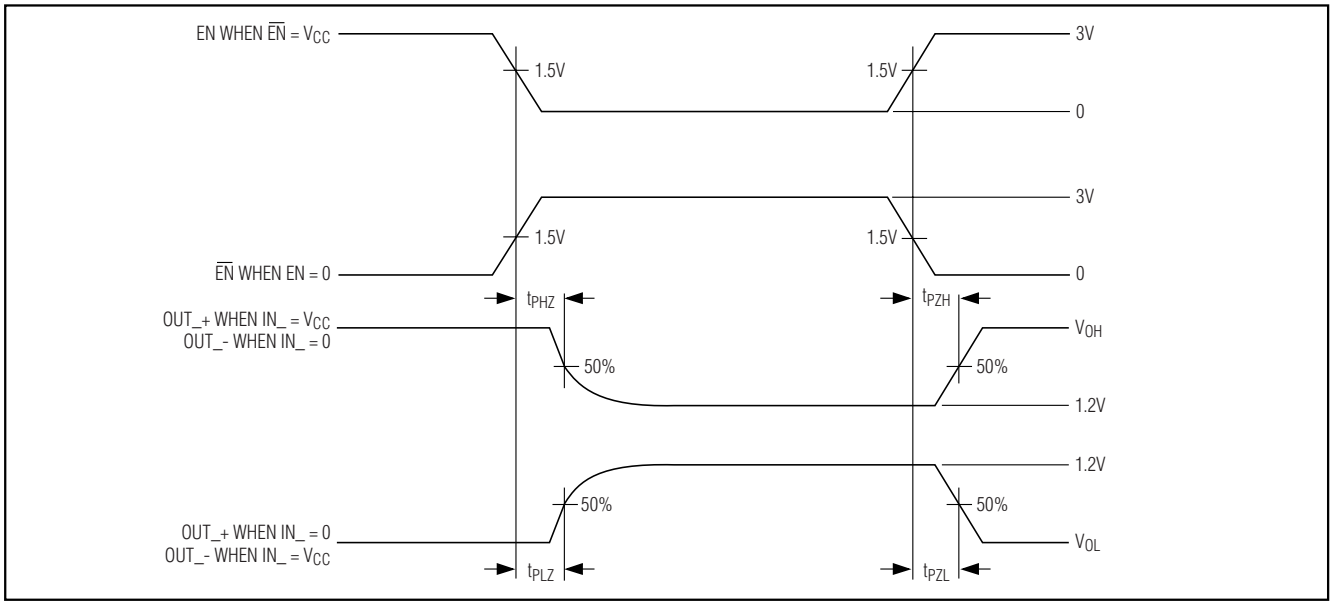
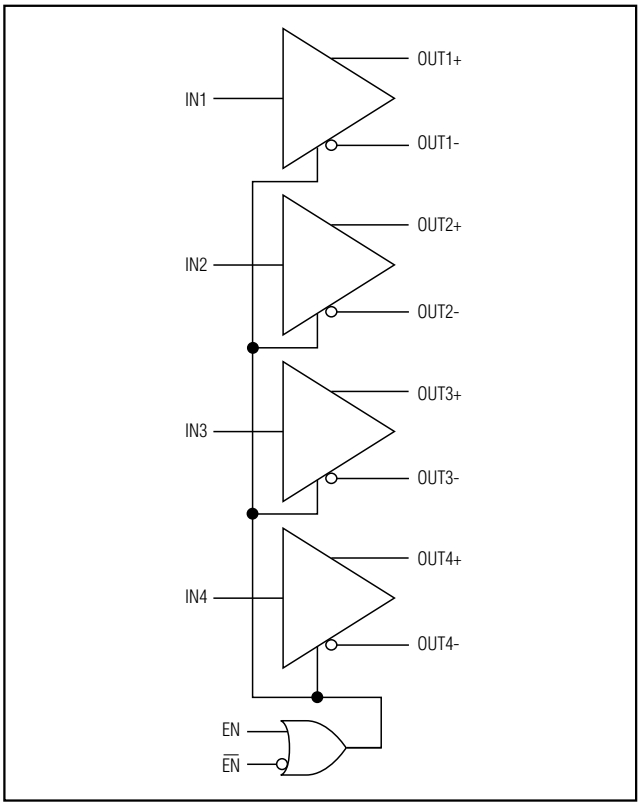


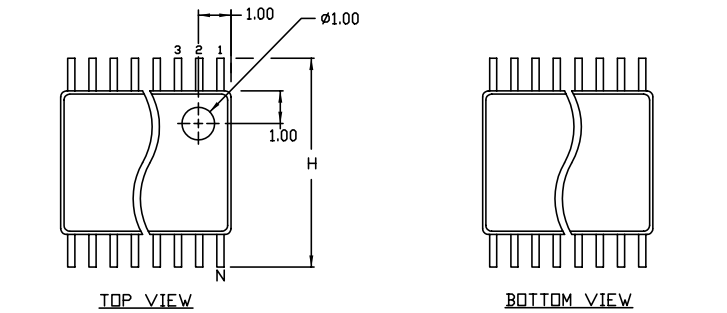
Figure 5. Driver High-Impedance Delay Waveform

Functional Diagram



Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AD	20	D	6.40	6.60	.252	.260
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386

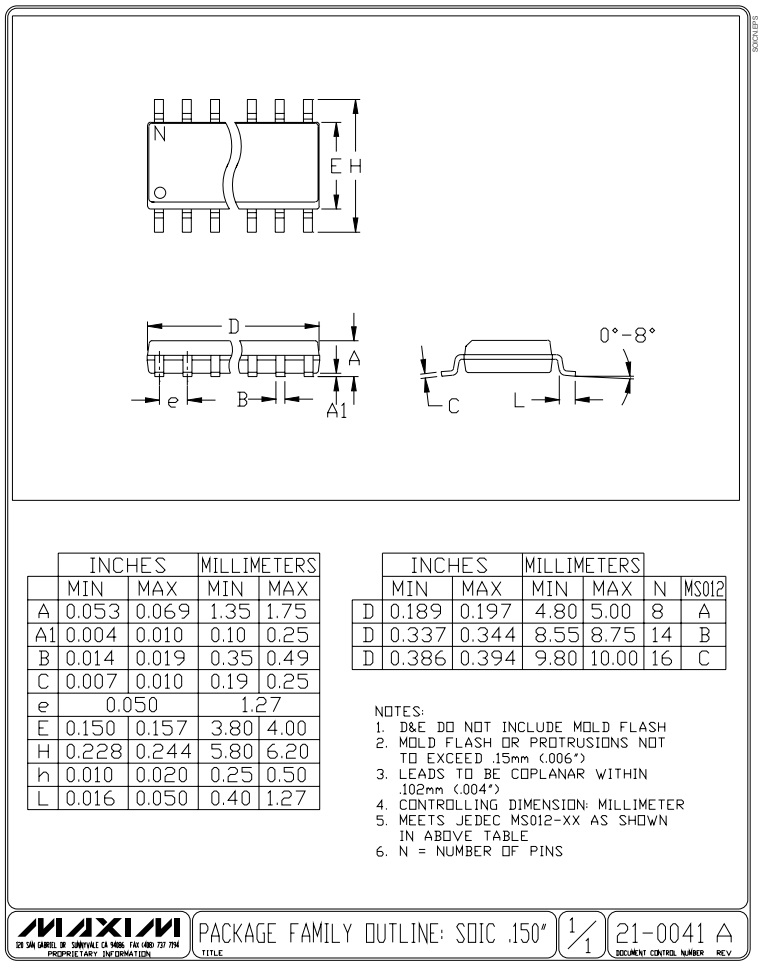
NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS- AB, AC, AD, AE, AF
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	D	1/1

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: SOIC .150" TITLE | 1/1 | 21-0041 A DOCUMENT CONTROL NUMBER REV