19-1854; Rev 5; 9/07

MAXIM

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

General Description

The MAX3840 is a dual 2 × 2 asynchronous crosspoint switch for SDH/SONET DWDM and other high-speed data switching applications where serial data stream loop-through and protection channel switching are required. It is ideal for OC-48 systems with forward error correction. A high-bandwidth, fully differential signal path minimizes jitter accumulation, crosstalk, and signal skew. Each 2 × 2 crosspoint switch can fan out and/or multiplex up to 2.7Gbps data and 2.7GHz clock signals. All inputs and outputs are current mode logic (CML) compatible and easily adaptable to interface with an AC-coupled LVPECL signal. When not used, each CML output stage can be powered down with an enable control to conserve power. The typical power consumption is 460mW with all outputs enabled.

The MAX3840 is compatible with the MAX3876 2.5Gbps clock and data recovery (CDR) circuit.

The MAX3840 is available in a 32-pin exposed-pad QFN package (5mm × 5mm footprint) and operates from a +3.3V supply over a temperature range of -40°C to +85°C.

Applications

SDH/SONET and DWDM Transport Systems

Add-Drop Multiplexers

ATM Switch Cores

WDM Cross-Connects

High-Speed Backplanes

Features

- **Single +3.3V Supply**
- **460mW Power Consumption**
- **2ps$_{RMS}$ Random Jitter**
- **7ps$_{P-P}$ Deterministic Jitter**
- **Power-Down Feature for Deselected Outputs**
- **CML Inputs/Outputs**
- **6ps Channel-to-Channel Skew**
- **100ps Output Edge Speed**
- **5mm × 5mm 32 QFN or Thin QFN Package**

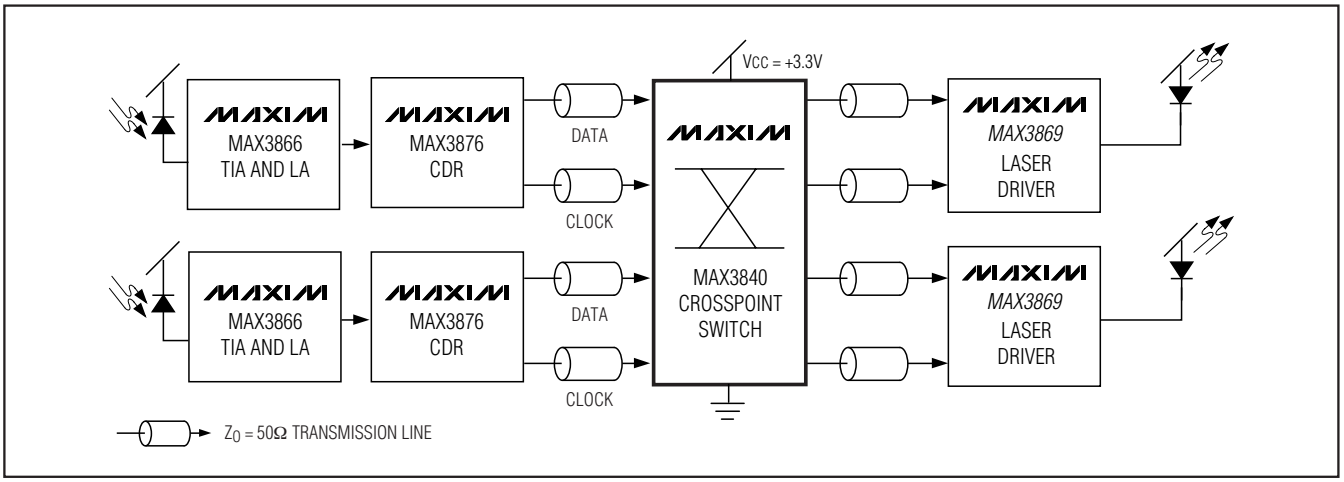
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3840ETJ+	-40°C to +85°C	32 TQFN	T3255-3
MAX3840EGJ	-40°C to +85°C	32 QFN	G3255-1

+Denotes a lead-free package.

Pin Configurations appear at end of data sheet.

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .....-0.5V to +5.0V
Input Voltage (CML) .....(VCC - 1.0) to (V_{CC} + 0.5V)
TTL Control Input Voltage.....-0.5V to (V_{CC} + 0.5V)
Output Currents (CML) 22mA
Continuous Power Dissipation (T_A = +85°C)
32-Pin TQFN
(derate 21.3mW/°C above +85°C).....1.38W
32-Pin QFN
(derate 21.3mW/°C above +85°C).....1.38W
Operating Temperature Range .....-40°C to +85°C
Operating Junction Temperature Range.....-55°C to +150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	All outputs enabled		140	190	mA
CML INPUT AND OUTPUT SPECIFICATIONS						
CML Differential Output Swing		R_L = 50Ω to V_{CC} (Figure 2)	640	800	1000	mV_{P-P}
Differential Output Impedance			85	100	115	Ω
CML Output Common-Mode Voltage		R_L = 50Ω to V_{CC}		V_{CC} - 0.2		V
CML Single-Ended Input Voltage Range	V_{IS}		V_{CC} - 0.8		V_{CC} + 0.5	V
CML Differential Input Voltage Swing			300		2000	mV_{P-P}
CML Single-Ended Input Impedance			42.5	50	57.5	Ω
TTL SPECIFICATIONS						
TTL Input High Voltage	V_{IH}		2.0			V
TTL Input Low Voltage	V_{IL}				0.8	V
TTL Input High Current	I_{IH}		-10		+10	µA
TTL Input Low Current	I_{IL}		-10		+10	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CML Input and Output Data Rate				2.7		Gbps
CML Input and Output Clock Rate				2.7		GHz
CML Output Rise and Fall Time	t_r, t_f	20% to 80%		100	136	ps
CML Output Random Jitter	RJ	(Note 2)		2		ps_{RMS}
CML Output Deterministic Jitter	DJ	(Note 3)		7	20	ps_{P-P}
CML Output Differential Skew	t_{skew1}	Any differential pair		7	25	ps
CML Output Channel-to-Channel Skew	t_{skew2}	Any two outputs		15	40	ps
Propagation Delay from Input-to-Output	t_d			185		ps
CML Differential Output Swing for 2.7Gbps Input Data		R_L = 50Ω to V_{CC} (Note 4)	600			mV_{P-P}
CML Differential Output Swing for 2.7GHz Input Clock		R_L = 50Ω to V_{CC} (Note 5)	520			mV_{P-P}

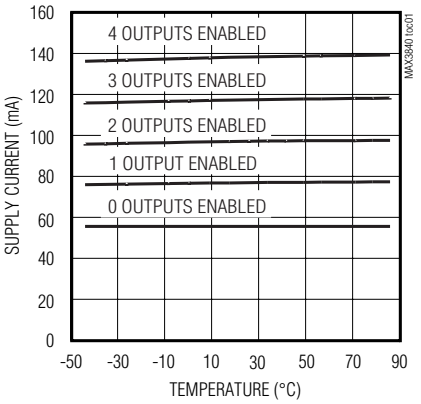
Note 1: AC characteristics are guaranteed by design and characterization.
Note 2: Measured with $100mV_{P-P}$ noise (f ≤ 2MHz) on the power supply.
Note 3: Deterministic jitter (DJ) is the arithmetic sum of pattern-dependent jitter and pulse-width distortion.
Note 4: Measured with $300mV_{P-P}$ differential 1010... data pattern driving the inputs.
Note 5: Measured with $300mV_{P-P}$ differential clock at 2.7GHz driving the inputs.

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

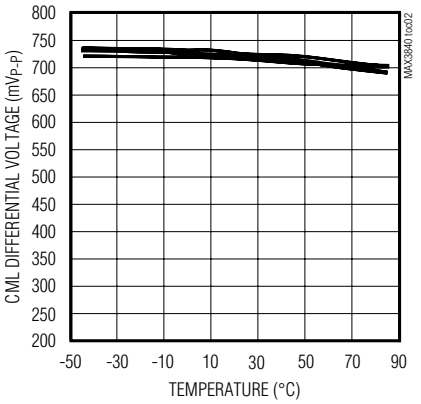
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

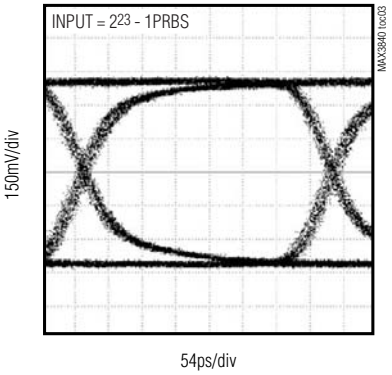
SUPPLY CURRENT vs. TEMPERATURE



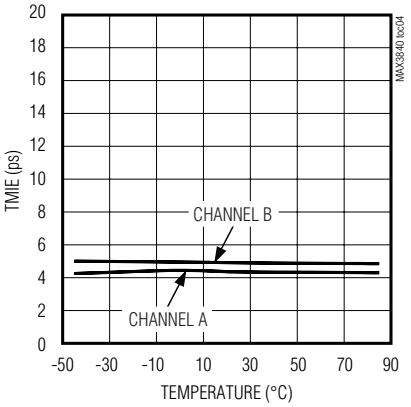
CML DIFFERENTIAL VOLTAGE



2.7Gbps EYE DIAGRAM



CHANNEL-TO-CHANNEL SKEW vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	ENB1	Channel B1 Output Enable, TTL Input. A TTL low input powers down B1 output stage.
2	DIB1+	Channel B1 Positive Signal Input, CML
3	DIB1-	Channel B1 Negative Signal Input, CML
4	ENB0	Channel B0 Output Enable, TTL Input. A TTL low input powers down B0 output stage.
5	SELB0	Channel B0 Output Select, TTL Input. See Table 1.
6	DIB0+	Channel B0 Positive Signal Input, CML
7	DIB0-	Channel B0 Negative Signal Input, CML
8	SELB1	Channel B1 Output Select, TTL Input. See Table 1.
9, 24	GND	Supply Ground
10, 13, 16, 17, 20, 23	V_{CC}	Positive Supply
11	DOB0-	Channel B0 Negative Output, CML
12	DOB0+	Channel B0 Positive Output, CML
14	DOB1-	Channel B1 Negative Output, CML
15	DOB1+	Channel B1 Positive Output, CML
18	DOA1-	Channel A1 Negative Output, CML
19	DOA1+	Channel A1 Positive Output, CML
21	DOA0-	Channel A0 Negative Output, CML
22	DOA0+	Channel A0 Positive Output, CML
25	SELA1	Channel A1 Output Select, TTL Input. See Table 1.
26	DIA0+	Channel A0 Positive Signal Input, CML
27	DIA0-	Channel A0 Negative Signal Input, CML
28	SELA0	Channel A0 Output Select, TTL Input. See Table 1.
29	ENA0	Channel A0 Output Enable, TTL Input. A TTL low input powers down A0 output stage.
30	DIA1+	Channel A1 Positive Signal Input, CML
31	DIA1-	Channel A1 Negative Signal Input, CML
32	ENA1	Channel A1 Output Enable, TTL Input. A TTL low input powers down A1 output stage.
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground for proper electrical and thermal operation.

Table 1. Output Routing

ROUTING CONTROLS		OUTPUT CONTROLS		OUTPUT SIGNALS	
SELA0/SELB0	SELA1/SELB1	ENA0/ENA1	ENB0/ENB1	Signal at DOA0/DOB0	Signal at DOA1/DOB1
0	0	1	1	DIA0/DIB0	DIA0/DIB0
0	1	1	1	DIA0/DIB0	DIA1/DIB1
1	0	1	1	DIA1/DIB1	DIA0/DIB0
1	1	1	1	DIA1/DIB1	DIA1/DIB1
X	X	0	0	Power Down	Power Down

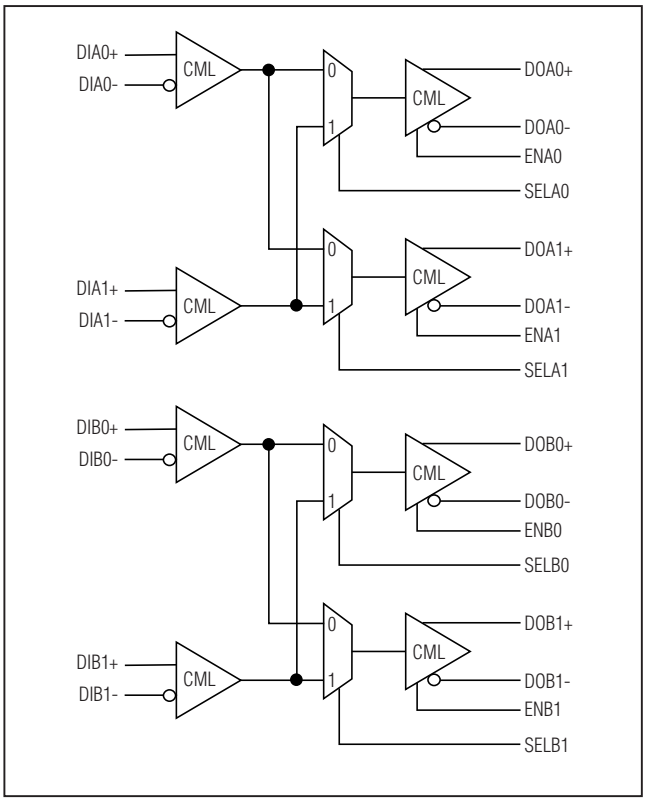


Figure 1. Functional Block Diagram

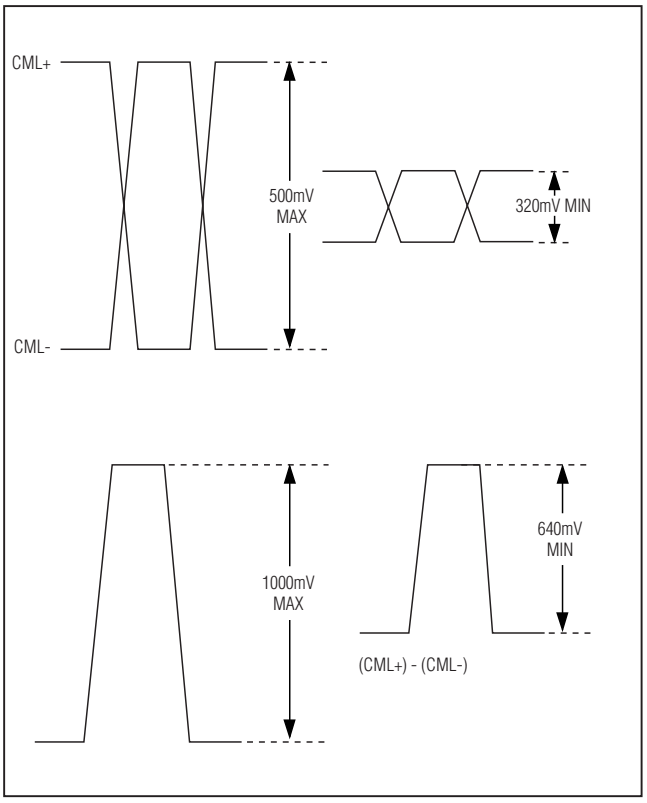


Figure 2. CML Output Levels

Detailed Description

The block diagram in Figure 1 shows the MAX3840 architecture. The SELA_ and SELB_ pins control the routing of the signals through the crosspoint switch. Each output of the crosspoint switch drives a CML output driver. Each of the outputs, DOA_ and DOB_, is enabled or disabled by the respective ENA_ and ENB_ pins.

CML Inputs and Outputs

CML is used to simplify high-speed interfacing. On-chip input and output terminations minimize the number of external components required while improving signal integrity. The CML output signal swing is small, resulting in lower power consumption. The internal 50Ω input and output terminations minimize reflections and eliminate the need for external terminations.

Applications Information

Interfacing PECL Inputs and Outputs to the MAX3840

For information on interfacing with CML, refer to Maxim Application Note HFAN-01.0, *Introduction to LVDS, PECL, and CML*.

Layout Techniques

For best performance, use good high-frequency layout techniques, filter V_{CC} supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3840 data inputs and outputs.

Interface Models

Figure 3 shows the interface model for the CML inputs, and Figure 4 shows the model for CML outputs.

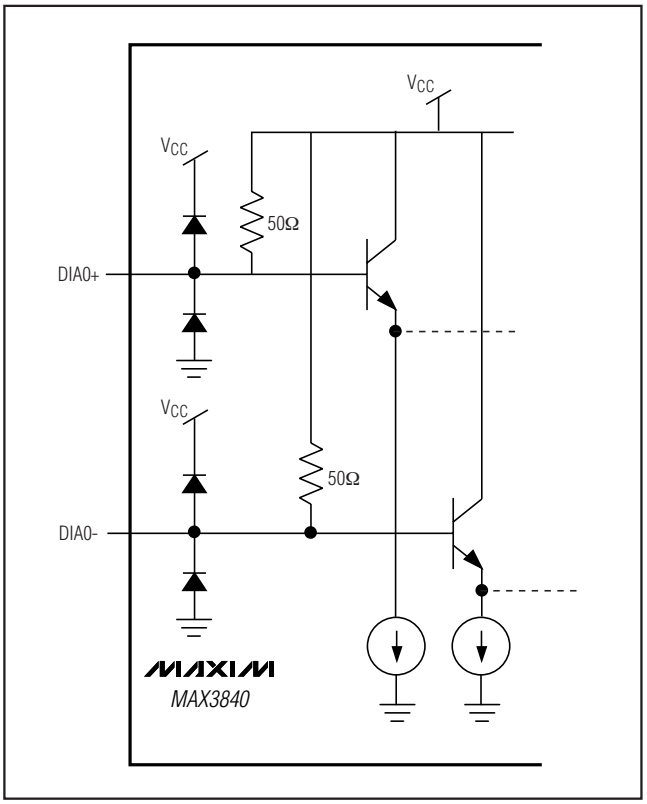


Figure 3. CML Input Model

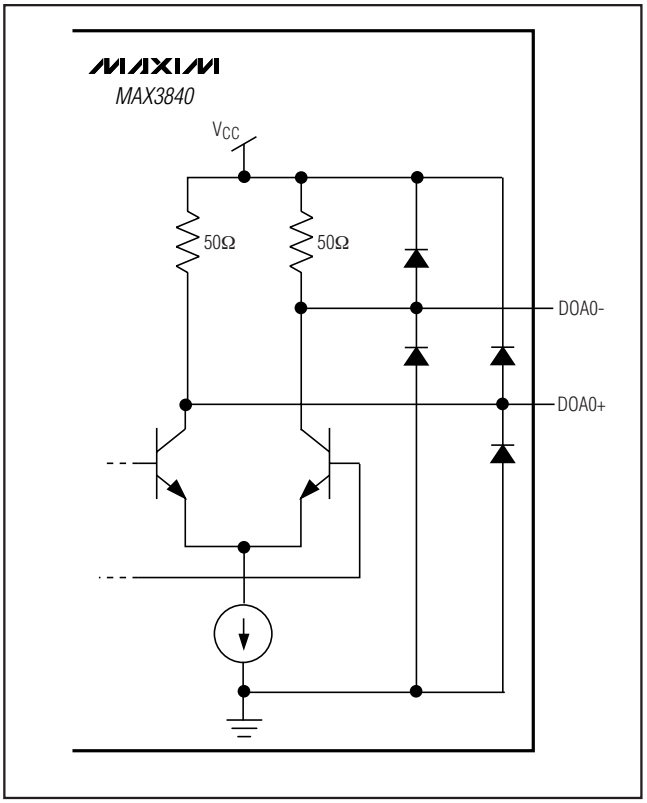


Figure 4. CML Output Model

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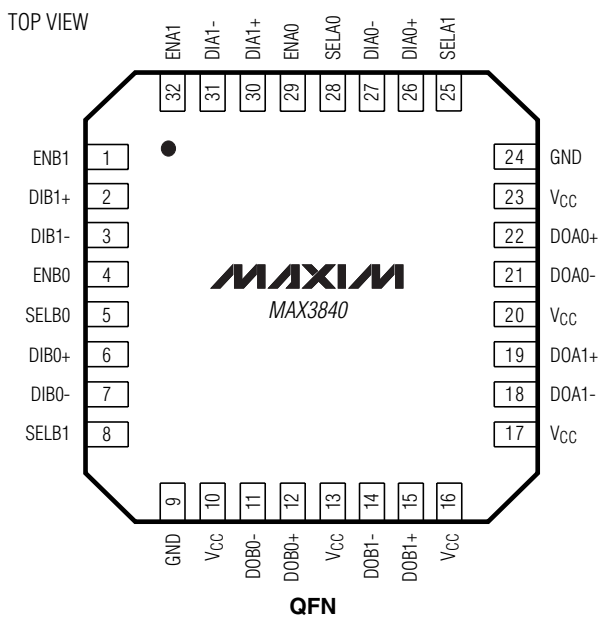
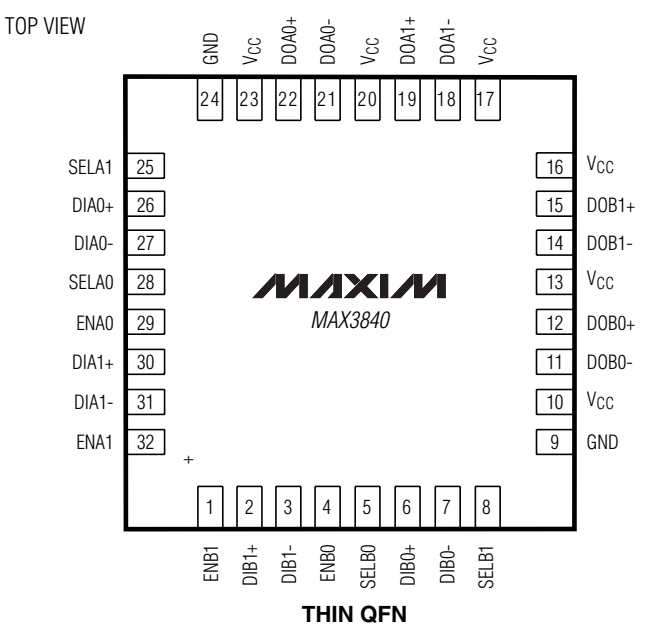
Pin Configurations



QFN

NOTE: THE EXPOSED PAD MUST BE SOLDERED TO THE SUPPLY GROUND.



THIN QFN

NOTE: THE EXPOSED PAD MUST BE SOLDERED TO THE SUPPLY GROUND.

Chip Information

TRANSISTOR COUNT: 1200

PROCESS: Bipolar (SiGe)

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	DOCUMENT NO.
32 QFN	21-0091
32 TQFN	21-0140

Revision History

Rev 1; 11/01: Corrected specification.

Rev 2; 5/03: Added package code (page 1); updated package drawing (page 10).

Rev 3; 5/05: Added lead-free package (pages 1, 2, 8, 11, 12).

Rev 4; 12/05: Changed input voltage swing from 1.5V_{P-P} (max) to 2.0V_{P-P} (max).

Rev 5; 9/07: Added two AC amplitude specifications to increase test coverage for 2.5Gbps and 2.7GHz clock inputs (page 3); removed package drawings and added package table (page 8).