

## Low voltage fast-switching NPN power transistor

### Features

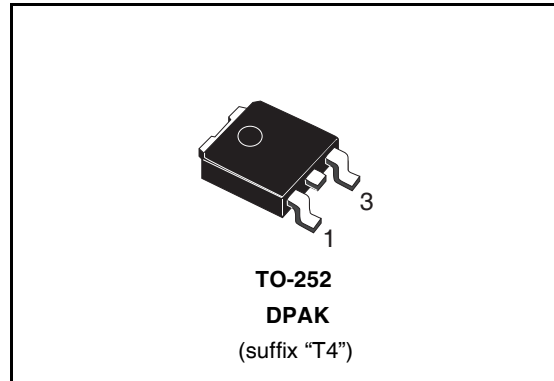
- Very low collector to emitter saturation voltage
- High current gain characteristic
- Fast-switching speed
- Surface-mounting DPAK (TO-252) power package in tape & reel (suffix "T4")

### Description

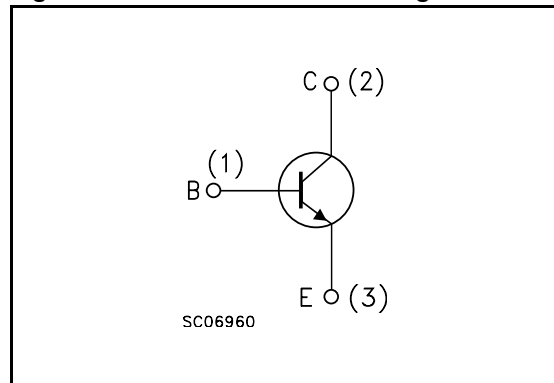
The device is manufactured in Planar technology with "Base Island" layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.

### Applications

- CCFL drivers
- Voltage regulators
- Relay drivers
- High efficiency, low voltage, switching applications



**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STD1802T4	D1802	DPAK	Tape & reel

# 1 Electrical ratings

**Table 2. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CBO}$	Collector-base voltage ( $I_E = 0$ )	80	V
$V_{CEO}$	Collector-emitter voltage ( $I_B = 0$ )	60	V
$V_{EBO}$	Emitter-base voltage ( $I_C = 0$ )	6	V
$I_C$	Collector current	3	A
$I_{CM}$	Collector peak current ( $t_P < 5\text{ms}$ )	6	A
$I_B$	Base current	1	A
$P_{tot}$	Total dissipation at $T_C \leq 25^\circ\text{C}$	15	W
$T_{stg}$	Storage temperature	-65 to 150	$^\circ\text{C}$
$T_J$	Max. operating junction temperature	150	$^\circ\text{C}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	8.33	$^\circ\text{C/W}$

## 2 Electrical characteristics

( $T_{\text{case}} = 25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. Electrical characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{\text{CBO}}$	Collector cut-off current ( $I_{\text{E}} = 0$ )	$V_{\text{CB}} = 40\text{V}$			0.1	$\mu\text{A}$
$I_{\text{EBO}}$	Emitter cut-off current ( $I_{\text{C}} = 0$ )	$V_{\text{EB}} = 4\text{V}$			0.1	$\mu\text{A}$
$V_{(\text{BR})\text{CBO}}$	Collector-base breakdown voltage ( $I_{\text{E}} = 0$ )	$I_{\text{C}} = 100\mu\text{A}$	80			V
$V_{(\text{BR})\text{CEO}}$	Collector-emitter breakdown voltage ( $I_{\text{B}} = 0$ )	$I_{\text{C}} = 1\text{mA}$	60			V
$V_{(\text{BR})\text{EBO}}$	Emitter-base breakdown voltage ( $I_{\text{C}} = 0$ )	$I_{\text{E}} = 100\mu\text{A}$	6			V
$V_{\text{CE}(\text{sat})}^{(1)}$	Collector-emitter saturation voltage	$I_{\text{C}} = 2\text{A}$ $I_{\text{B}} = 100\text{mA}$ $I_{\text{C}} = 3\text{A}$ $I_{\text{B}} = 150\text{mA}$		150 200	300 400	mV mV
$V_{\text{BE}(\text{sat})}^{(1)}$	Base-emitter saturation voltage	$I_{\text{C}} = 2\text{A}$ $I_{\text{B}} = 100\text{mA}$		0.9	1.2	V
$h_{\text{FE}}^{(1)}$	DC current gain	$I_{\text{C}} = 100\text{mA}$ $V_{\text{CE}} = 2\text{V}$ $I_{\text{C}} = 3\text{A}$ $V_{\text{CE}} = 2\text{V}$	200 100		400	
$f_{\text{T}}$	Transition frequency	$V_{\text{CE}} = 10\text{V}$ $I_{\text{C}} = 50\text{mA}$		150		MHz
$C_{\text{CBO}}$	Collector-base capacitance	$V_{\text{CB}} = 10\text{V}$ $f = 1\text{MHz}$		50		pF
$t_{\text{ON}}$ $t_{\text{s}}$ $t_{\text{f}}$	Resistive load Turn-on time Storage time Fall time	$I_{\text{C}} = 1\text{A}$ $V_{\text{CC}} = 30\text{V}$ $I_{\text{B1}} = -I_{\text{B2}} = 0.1\text{A}$		50 1.35 120		ns $\mu\text{s}$ ns

Note (1) Pulsed duration = 300  $\mu\text{s}$ , duty cycle  $\leq 1.5\%$

## 2.1 Electrical characteristics (curves)

Figure 2. Derating curve

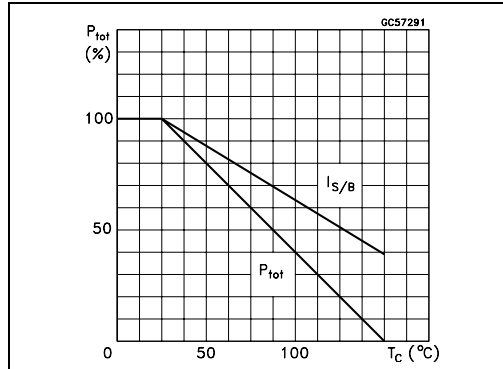


Figure 3. DC current gain

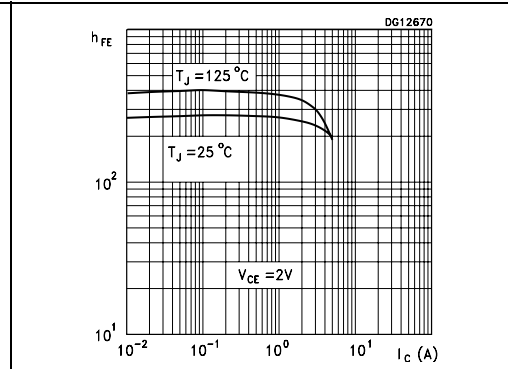


Figure 4. Collector-emitter saturation voltage

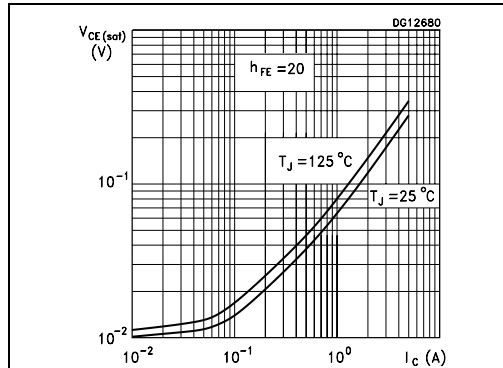


Figure 5. Collector-emitter saturation voltage

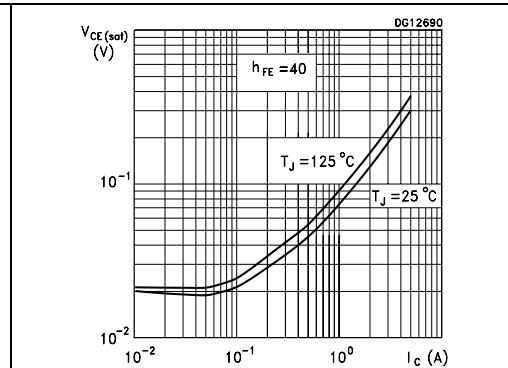


Figure 6. Base-emitter saturation voltage

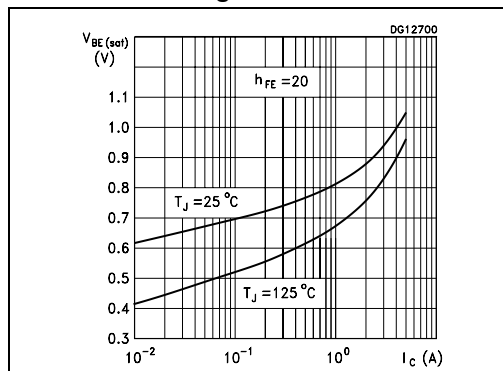
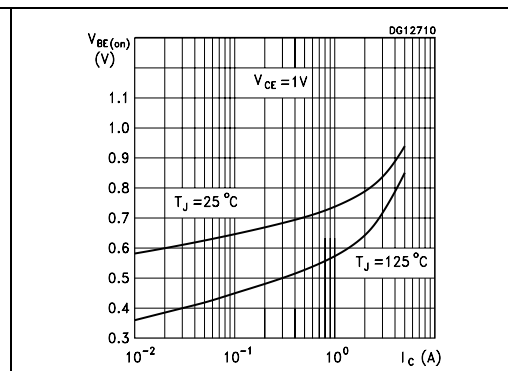
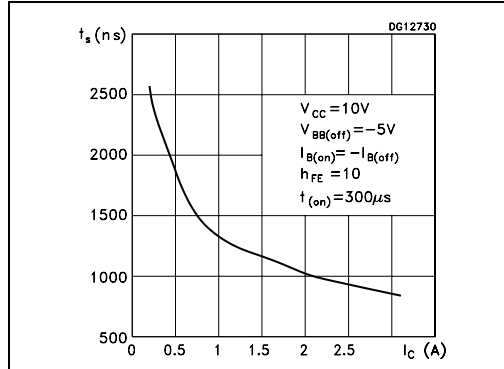


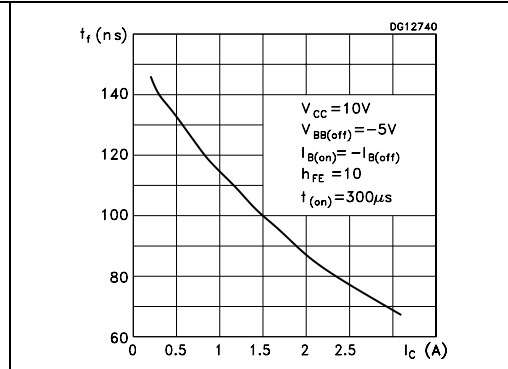
Figure 7. Base-emitter on voltage



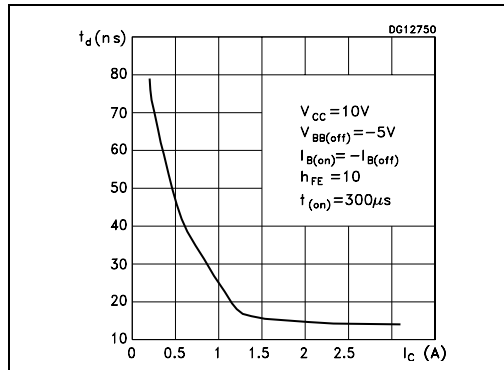
**Figure 8. Switching times resistive load**



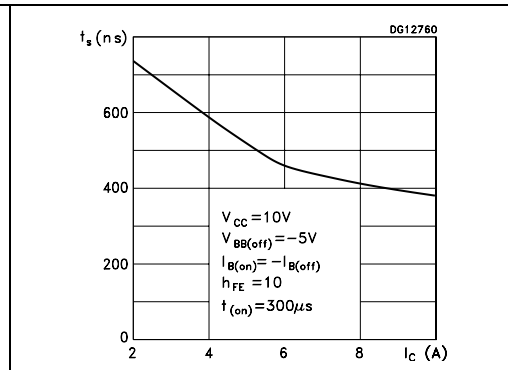
**Figure 9. Switching times resistive load**



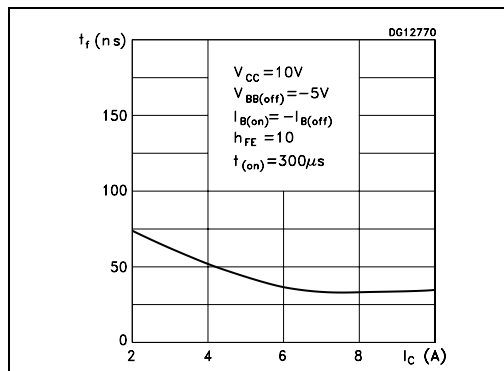
**Figure 10. Switching times resistive load**



**Figure 11. Switching times inductive load**

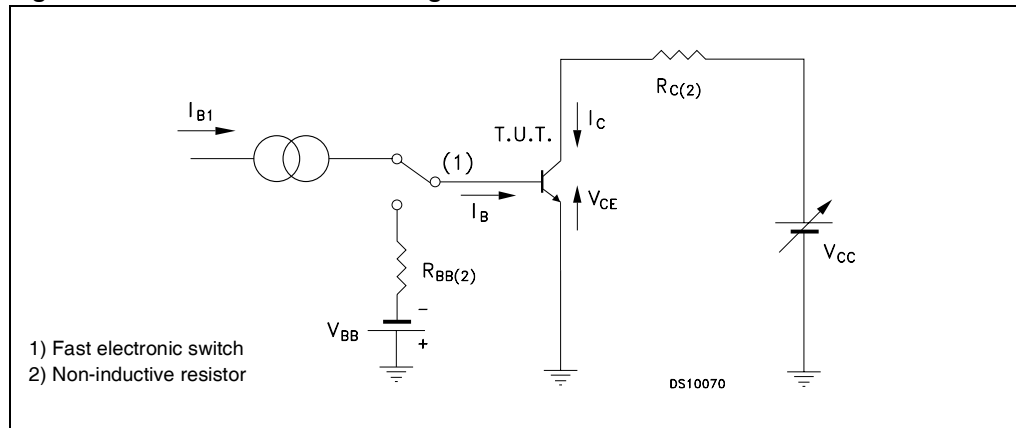


**Figure 12. Switching times resistive load**



## 2.2 Test circuits

Figure 13. Resistive load switching test circuit

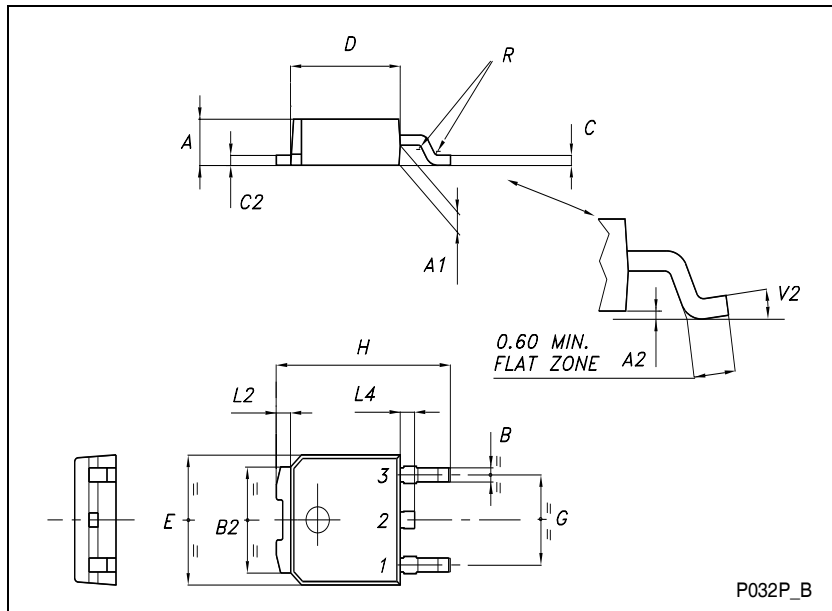


### 3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-252 (DPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°





## 4 Revision history

**Table 5. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
11-Mar-2003	1	Initial release.
05-Sep-2003	2	Minor text change
12-Jun-2004	3	New disclaimer
12-Jul-2007	4	Package name added on table 1.

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