STFI20NK50Z

N-channel 500 V, 0.23 Ω, 17 A Zener-protected SuperMESH™ Power MOSFET in I²PakFP

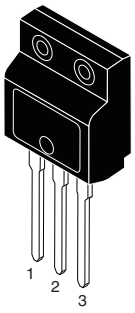
Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STFI20NK50Z	500 V	< 0.27 Ω	17 A(1)	40 W

1. Limited by maximum junction temperature

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized



I²PakFP

Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well-established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

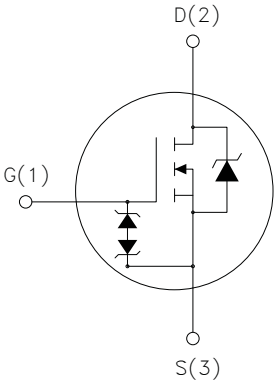


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFI20NK50Z	20NK50Z	I²PakFP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	17(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10.71(1)	A
I_{DM} (2)	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at T_C = 25 °C	40	W
ESD	Gate-source human body model (R=1,5 kΩ, C=100 pF)	6	kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max operating junction temperature	150	°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} < 17 A, di/dt < 200 A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Repetitive or non repetitive avalanche current	17	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	850	mJ

1. Limited by maximum junction temperature.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D =1 mA	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V V_{DS} = 500 V, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8.5 A		0.23	0.27	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 8.5 A	-	13		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2600 328 72		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{DS} =0, V_{DS} = 0 to 640 V	-	187		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 250 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15*)	-	28 20 70 15		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 10 V (see *Figure 16*)	-	85 15.5 42	119	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		17 68	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_R = 100 V (see *Figure 17*)	-	355 3.90 22		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_R = 100 V, Tj = 150 °C (see *Figure 17*)	-	440 5.72 26		ns µC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Pulse width limited by safe operating area.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage (I_D = 0)	I_{GS}= ± 1mA	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

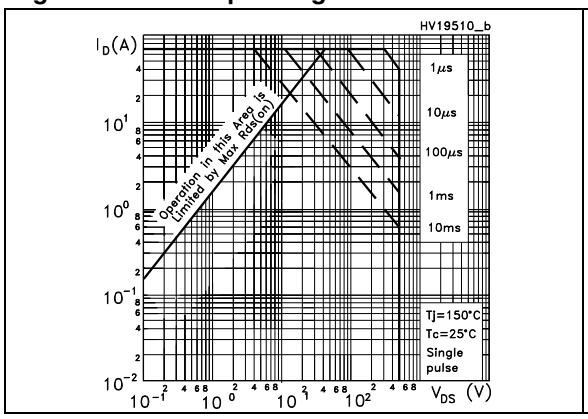


Figure 3. Thermal impedance

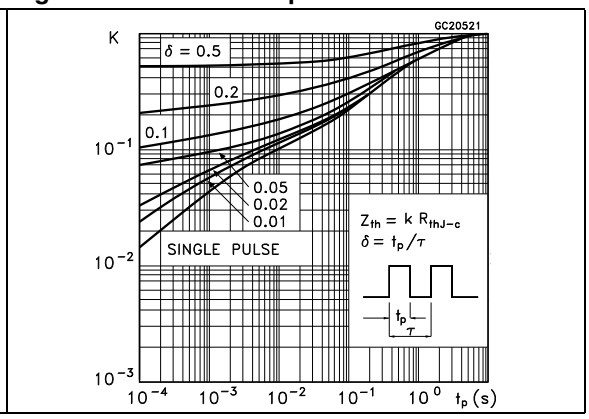


Figure 4. Output characteristics

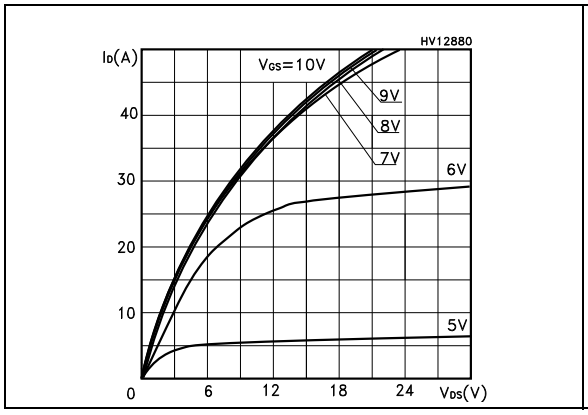


Figure 5. Transfer characteristics

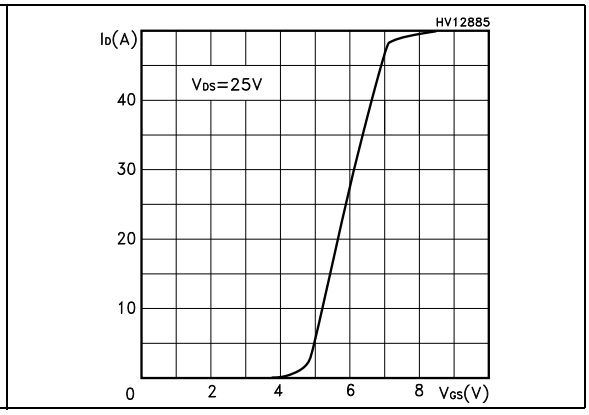


Figure 6. Transconductance

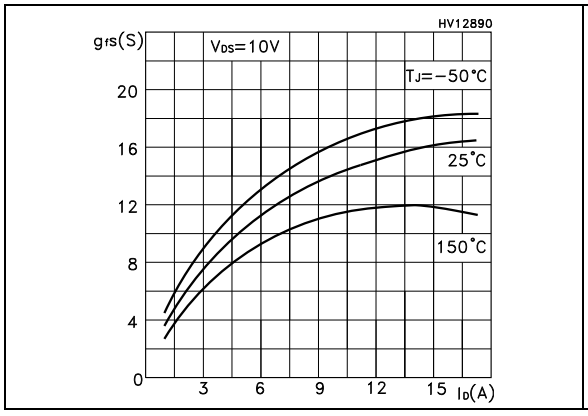


Figure 7. Static drain-source on resistance

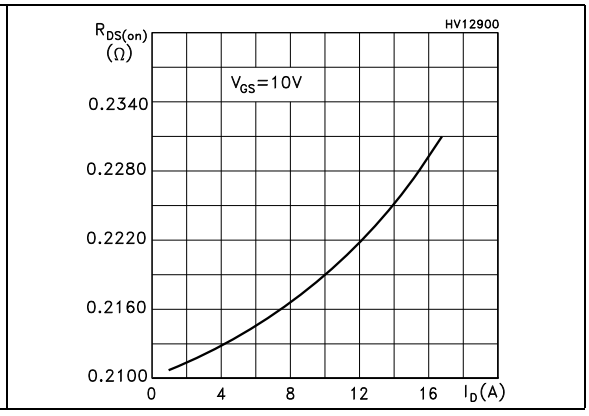


Figure 8. Gate charge vs gate-source voltage

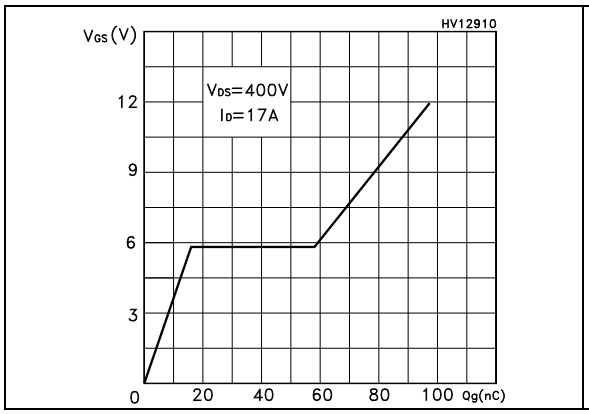


Figure 9. Capacitance variations

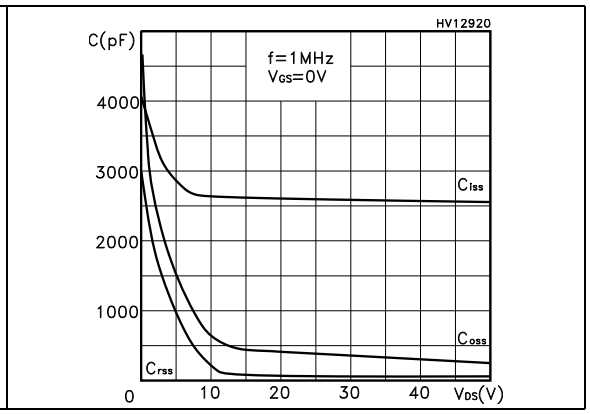


Figure 10. Normalized gate threshold voltage vs temperature

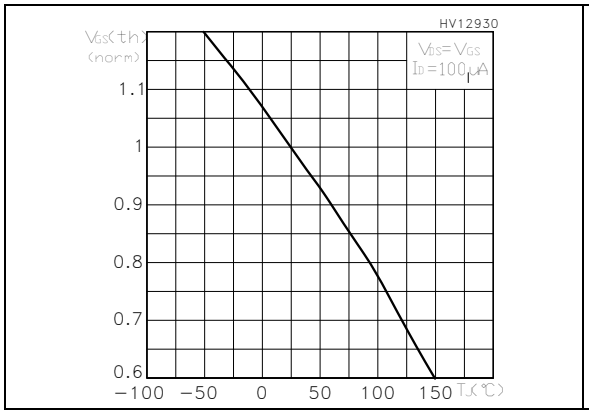


Figure 11. Normalized on resistance vs temperature

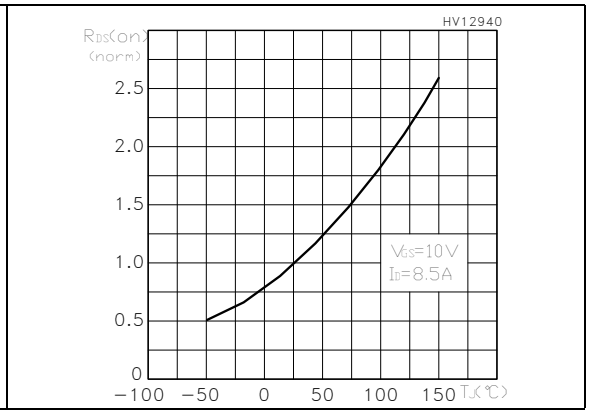


Figure 12. Maximum avalanche energy vs temperature

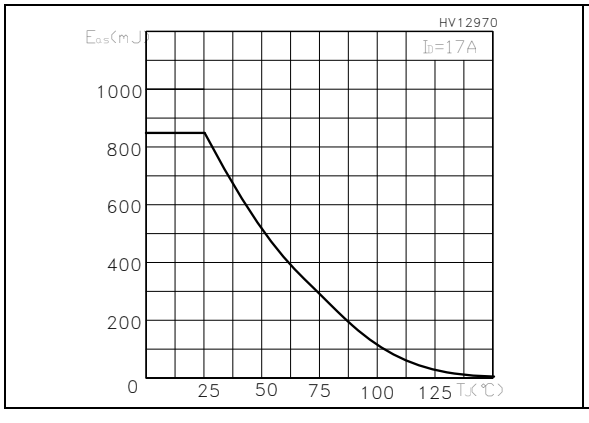


Figure 13. Normalized B_{VDSS} vs temperature

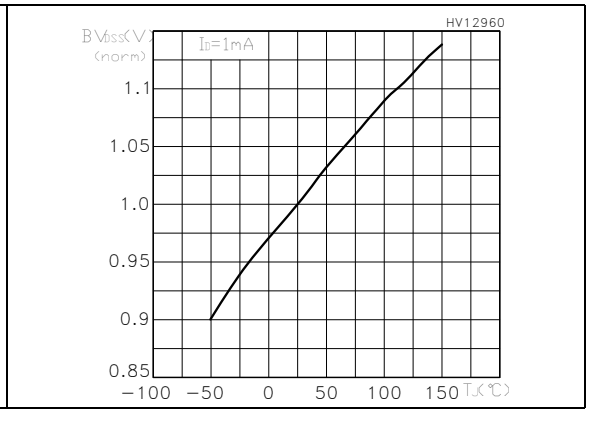
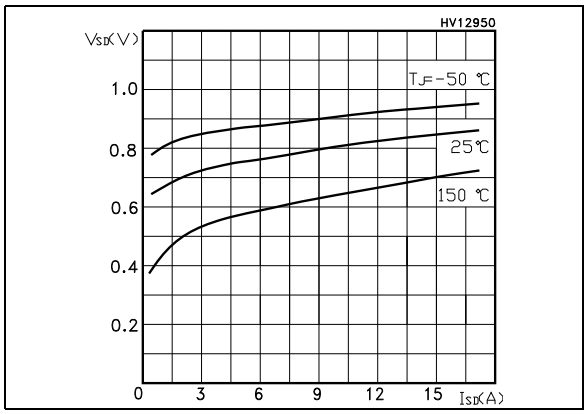


Figure 14. Source-drain diode forward characteristic



3 Test circuits

Figure 15. Switching times test circuit for resistive load

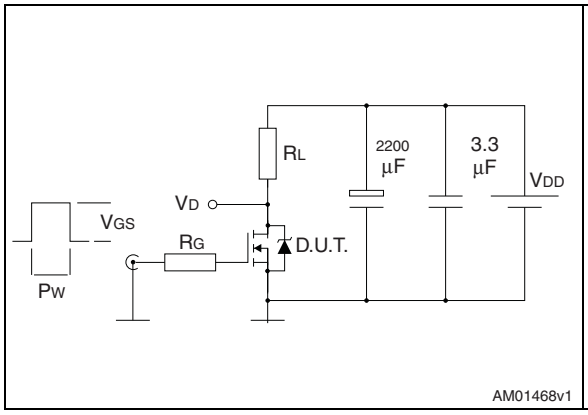


Figure 16. Gate charge test circuit

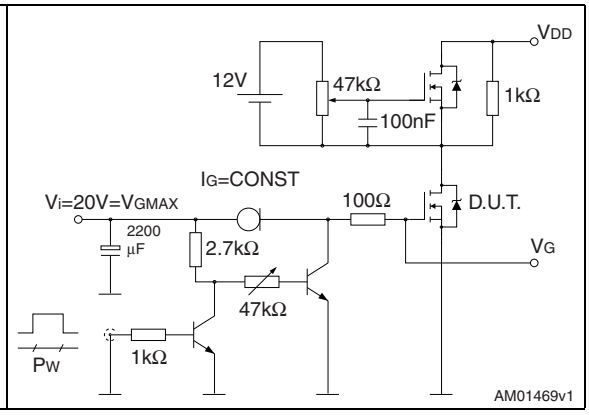


Figure 17. Test circuit for inductive load switching and diode recovery times

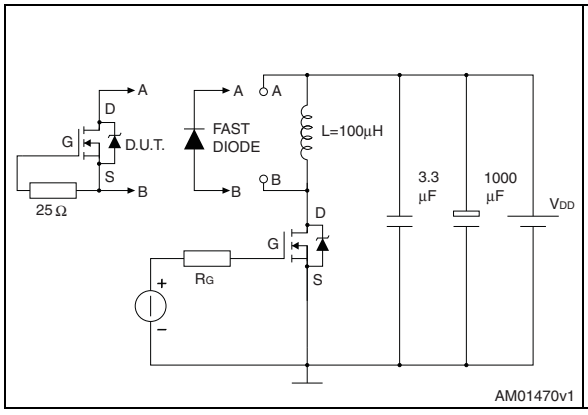


Figure 18. Unclamped inductive load test circuit

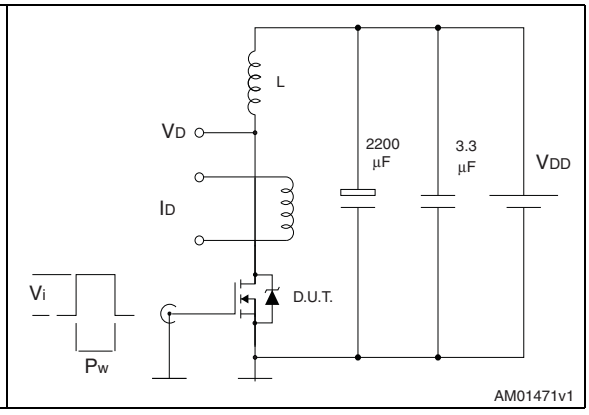


Figure 19. Unclamped inductive waveform

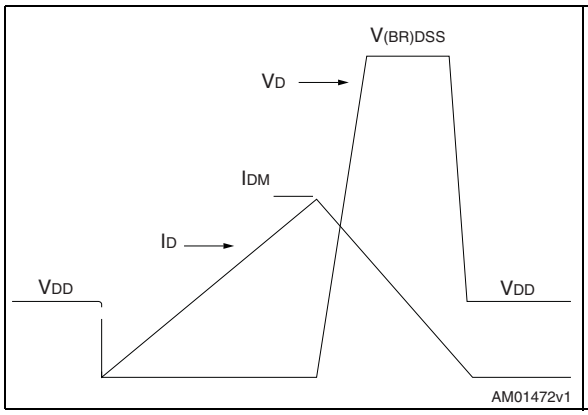
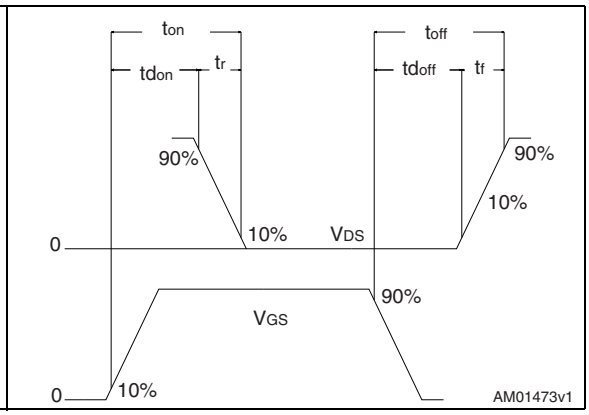


Figure 20. Switching time waveform



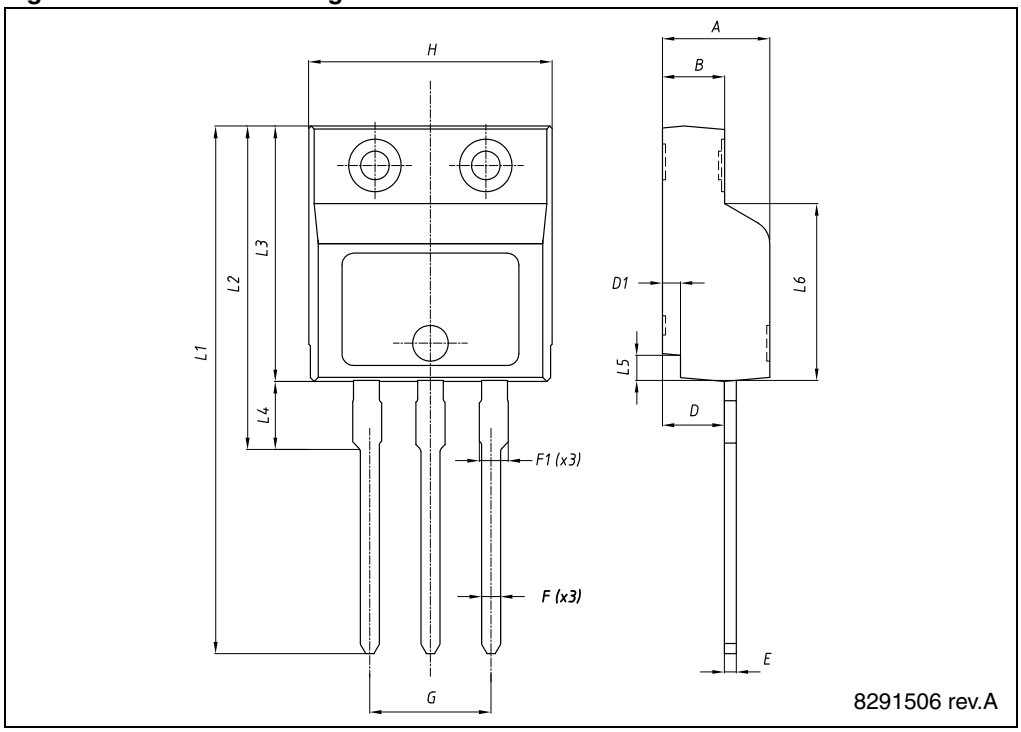
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. I^2PakFP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I^2PakFP drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Jul-2011	1	First release.
11-Nov-2011	2	*Figure 2: Safe operating area* and *Figure 3: Thermal impedance* have been added.

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