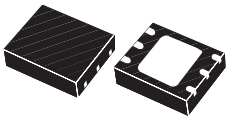
ST1L02xx

Very low quiescent BiCMOS voltage regulator

Features

- Fixed output voltage: 1.8 V, 2.5 V, 3.3 V (1.5 V, under customer request)
- Output voltage tolerance: ± 2 % at 25 °C
- Output current capability: 1 A minimum
- Very low quiescent current: max 500 µA over temperature range
- Typ. dropout 0.7 V (@ I_O = 1 A)
- Stable with low ESR ceramic capacitors
- Available with and without the external output voltage sense pin
- Thermal shutdown protection with hysteresis
- Over current protection
- Operating junction temperature range: from 0 to 125 °C



DFN6D (3x3 mm)

Internal protection circuitry includes thermal protection with hysteresis and over current limiting.

The ST1L02xx is especially suitable for data storage applications such as HDDs, where can be used to supply the read channel and memory chips requiring 3.3 V.

The regulator is available in the small and thin DFN6D (3x3 mm) package.

Description

The ST1L02xx is a low drop linear voltage regulator capable to supply up to 1 A output current.

The output voltage is fixed to 3.3 V, but under customer request, it's possible to have also 1.5 V, 1.8 V and 2.5 V. Thanks to the BiCMOS technology, the quiescent current is well controlled and maintained below 650 µA over the whole allowed junction temperature range.

The ST1L02xx is stable with low ESR output ceramic capacitors.

Table 1. Device summary

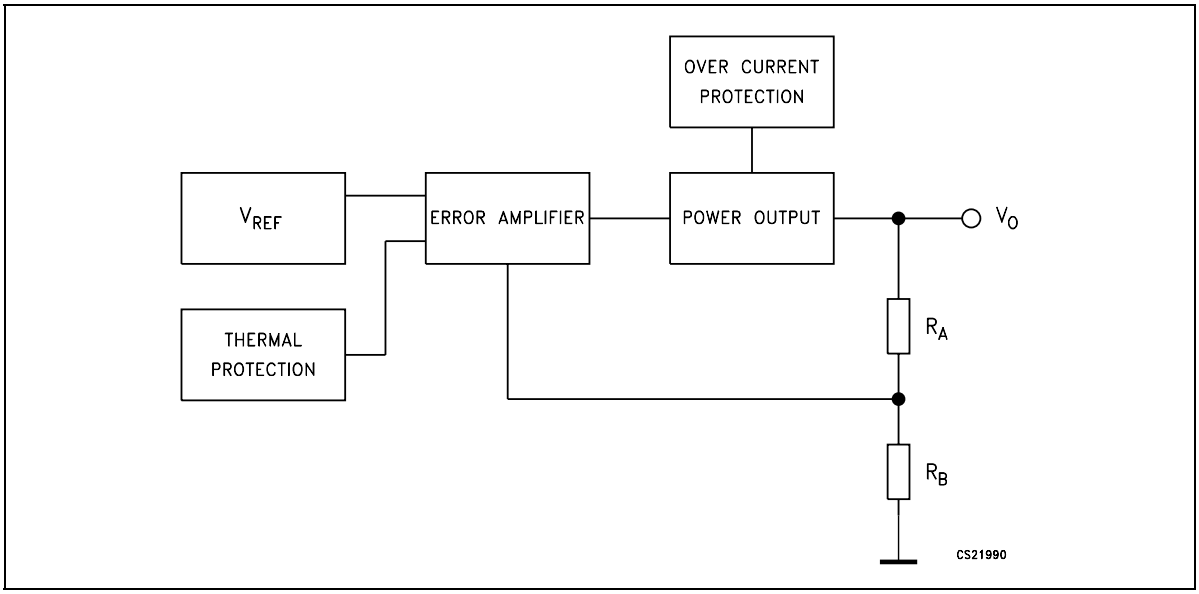
Part numbers	Order codes	Package
ST1L02XX18	ST1L02PU18R	DFN6D (3x3 mm)
ST1L02XX25	ST1L02PU25R	DFN6D (3x3 mm)
ST1L02XX33	ST1L02PU33R	DFN6D (3x3 mm)
ST1L02XX	ST1L02PUR (1)	DFN6D (3x3 mm)

1. Only 3.3 V

Contents

1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connections (top through view)

* Only 3.3 V.

Table 2. Pin description

Pin n° for ST1L02PXxx	Pin n° for ST1L02PX	Symbol	Name and function
1, 3	1, 4, 5	N.C.	Not connected.
2	6	GND	Ground. The exposed metallic pad of the package is connected to GND.
4	2	V_O	Output voltage pin. Bypass with a 4.7 µF capacitor to GND.
5	-	V_{O_SENSE}	Sense output voltage pin. Must be connected to pin 4.
6	3	V_I	Supply voltage input pin. Bypass with a 4.7 µF capacitor to GND.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC supply voltage	10	V
P_{TOT}	Power dissipation	internally limited	W
I_O	Output current	internally limited	A
T_{OP}	Operating junction temperature range	0 to 150	°C
T_{STG}	Storage temperature range (1)	-65 to 150	°C
T_{LEAD}	Lead temperature (Soldering) 10 Sec.	260	°C

1. Storage temperature >125 °C are acceptable only if the regulator is soldered to a PCBA.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	55	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics for ST1L02XX18
(refer to the typical application schematic, V_I = 4.5 V to 7 V, I_O = 5 mA to 1 A, C_I = 4.7 µF, C_O = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified). Typical values are intended at T_J = 25 °C unless otherwise specified.

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T=25°C	1.764	1.8	1.836	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	1.746	1.8	1.854	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1 A			10	mV
I_S	Output current limit	V_I = 5.5 V	1.0			A
I_{OMIN}	Minimum output current for regulation				2	mA
V_d	Dropout voltage (1)	I_O = 0.8 A			1.6	V
		I_O = 1 A			1.6	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1 A, T = 25°C			500	µA
I_Q	Quiescent current	V_I = 7 V, I_O = 2 mA to 1 A			650	µA
SVR	Supply voltage rejection (2)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	75		dB
eN	RMS Output noise (2)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising) (3)	V_I = 5 V, any 200 mA step from 100 mA to 1 A, $t_R \geq$ 1 µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling) (3)	V_I = 5 V, I_O = 1 A to 10 mA, $t_F \geq$ 1 µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient (3)	V_I =0 V to 5 V, I_O = 10 mA to 1 A, $t_R \geq$ 1 µs			3.5	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (3)	V_I = 5 V, I_O = short to 10 mA			3.5	V
T_{SH}	Thermal shutdown trip point (3)	V_I = 5 V		165		°C

1. See minimum start-up voltage, V_I = 3.3 V.
2. Guaranteed by design. Not tested in production.
3. C_I = 10 µF, C_O = 10 µF, all X7R ceramic capacitors.

Table 6. Electrical characteristics for ST1L02XX25
(refer to the typical application schematic, V_I = 4.5 V to 7 V, I_O = 5 mA to 1 A, C_I = 4.7 µF, C_O = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified). Typical values are intended at T_J = 25 °C unless otherwise specified.

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T = 25°C	2.45	2.5	2.55	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	2.4375	2.5	2.5625	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1 A			10	mV
I_S	Output current limit	V_I = 5.5 V	1.0			A
I_{OMIN}	Minimum output current for regulation				2	mA
V_d	Dropout voltage (1)	I_O = 0.8 A		0.6	1.0	V
		I_O = 1 A		0.7	1.1	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1 A, T= 25°C			500	µA
I_Q	Quiescent current	V_I = 7 V, I_O = 2 mA to 1 A			650	µA
SVR	Supply voltage rejection (2)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	75		dB
eN	RMS Output noise (2)	B = 10 Hz to 10 kHz, V_I = 5V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising) (3)	V_I =5 V, any 200 mA step from 100mA to 1A, $t_R \geq$ 1 µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling) (3)	V_I = 5 V, I_O = 1 A to 10 mA, $t_F \geq$ 1 µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient (3)	V_I =0 V to 5 V, I_O = 10 mA to 1 A, $t_R \geq$ 1 µs			3.5	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (3)	V_I = 5 V, I_O = short to 10 mA			3.5	V
T_{SH}	Thermal shutdown trip point (2)	V_I = 5 V		165		°C

1. See minimum start-up voltage, V_I = 3.2 V.
2. Guaranteed by design. Not tested in production
3. C_I = 10 µF, C_O = 10 µF, all X7R ceramic capacitors.

Table 7. Electrical characteristics for ST1L02XX33
(refer to the typical application schematic, V_I = 4.5V to 7V, I_O = 5mA to 1A, C_I = 4.7µF, C_O = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified). Typical values are intended at T_J = 25 °C unless otherwise specified.

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T = 25°C	3.234	3.3	3.366	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	3.2175	3.3	3.3825	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1 A			10	mV
I_S	Output current limit	V_I = 5.5 V	1.0			A
I_{OMIN}	Minimum output current for regulation				2	mA
V_d	Dropout voltage	I_O = 0.8 A		0.6	1.0	V
		I_O = 1 A		0.7	1.1	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1 A, T= 25°C			500	µA
I_Q	Quiescent current	V_I = 7 V, I_O = 2 mA to 1 A			650	µA
SVR	Supply voltage rejection (2)	V_I = 5 ± 0.5V, I_O = 5 mA, f = 120 Hz	50	75		dB
eN	RMS Output noise (2)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising) (1)	V_I = 5 V, any 200 mA step from 100 mA to 1 A, $t_R \geq$ 1 µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling) (1)	V_I = 5 V, I_O = 1 A to 10 mA, $t_F \geq$ 1 µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient (1)	V_I =0 V to 5 V, I_O = 10 mA to 1 A, $t_R \geq$ 1 µs			3.5	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (1)	V_I = 5 V, I_O = short to 10 mA			3.5	V
T_{SH}	Thermal shutdown trip point (2)	V_I = 5 V		165		°C

1. C_I = 10 µF, C_O = 10 µF, all X7R ceramic capacitors.
2. Guaranteed by design. Not tested in production.

5 Typical application

Figure 3. Application schematic for ST1L02PM

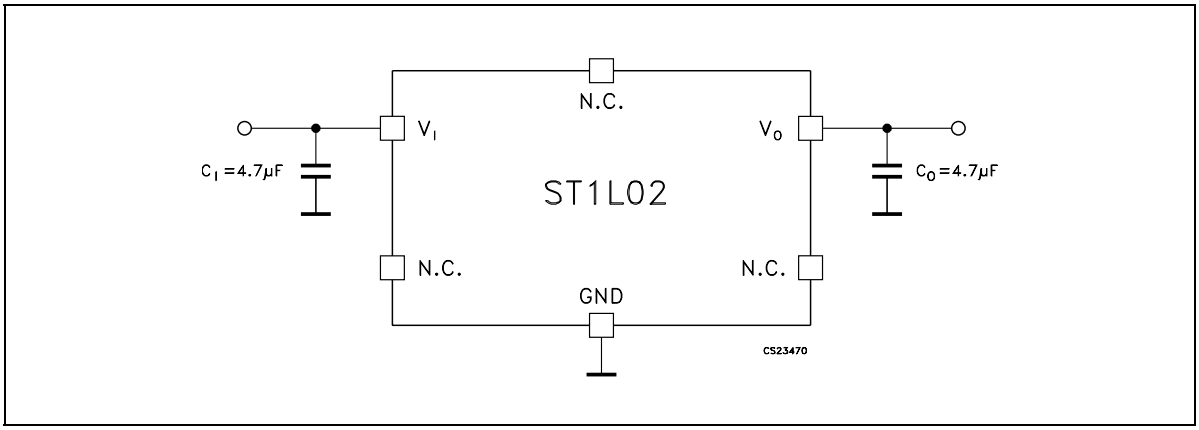
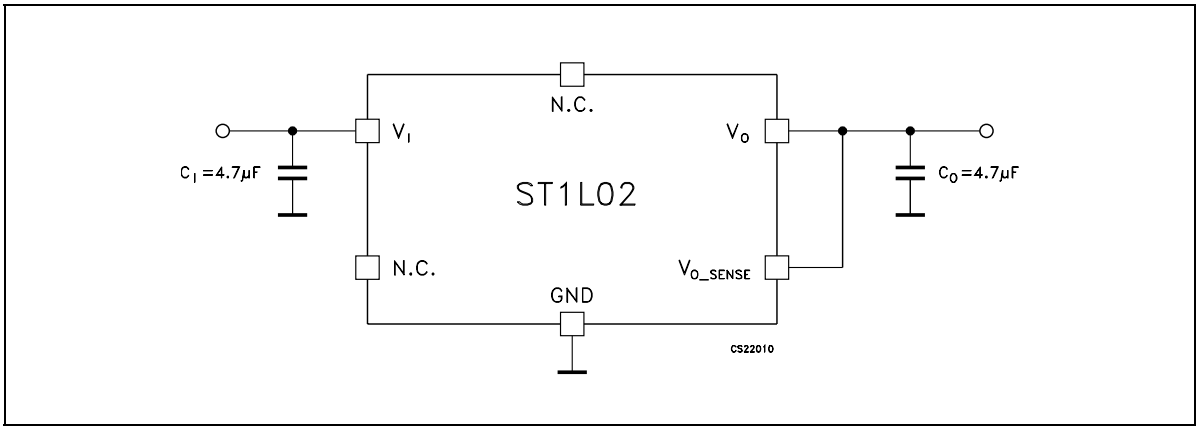


Figure 4. Application schematic for ST1L02PMxx



Note: The regulator is designed to be stable with either tantalum and ceramic capacitors on the input and the output. The expected values of the input and output ceramic capacitors are from 1 µF to 22 µF with 4.7 µF typical. The input capacitor must be connected within 0.5 inches of the V_I terminal. The output capacitor must also be connected within 0.5 inches of output pin. There is no upper limit to the value of the input capacitor.

6 Typical characteristics

Figure 5. Output voltage vs temperature

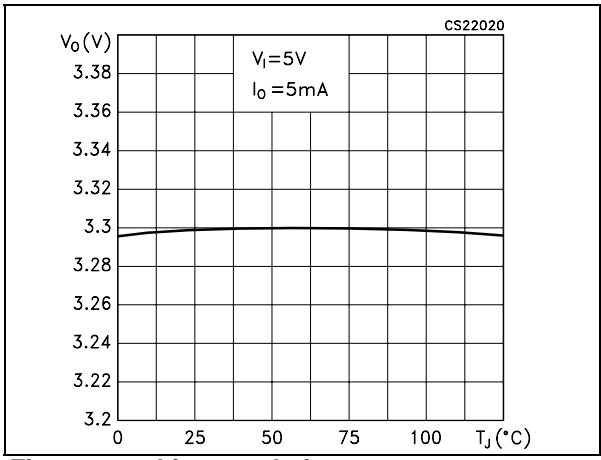


Figure 6. Line regulation vs temperature

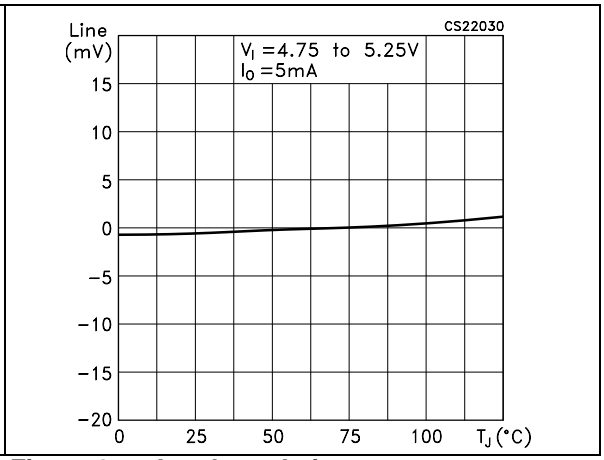


Figure 7. Line regulation vs temperature

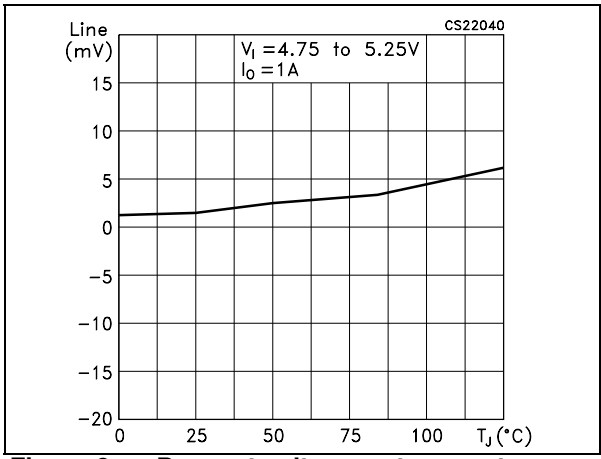


Figure 8. Load regulation vs temperature

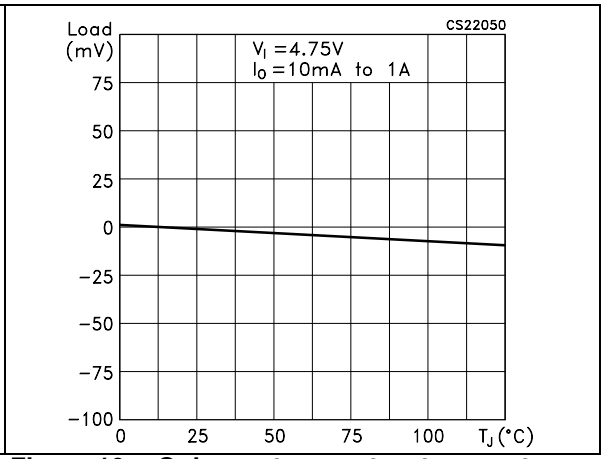


Figure 9. Dropout voltage vs temperature

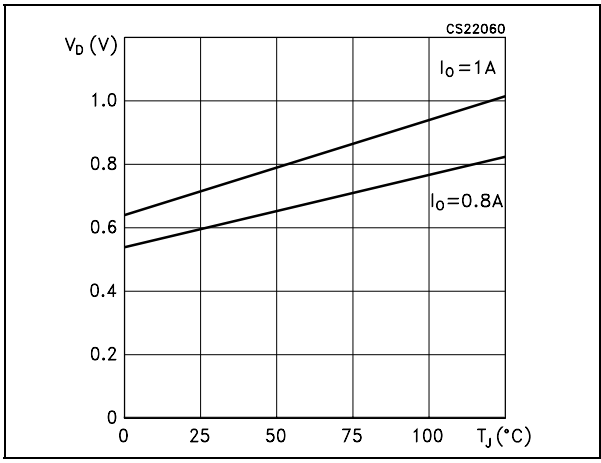


Figure 10. Quiescent current vs temperature

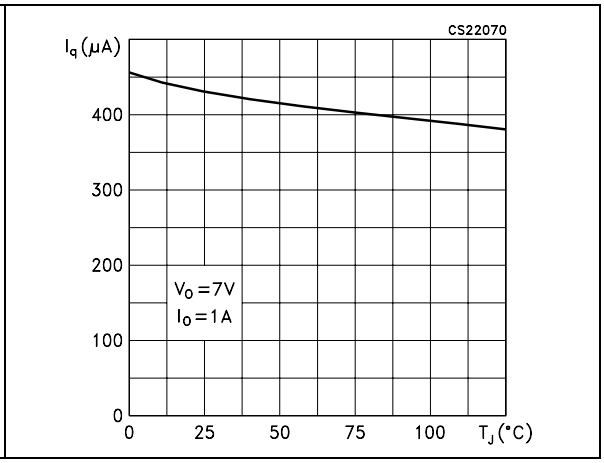


Figure 11. Quiescent current vs temperature

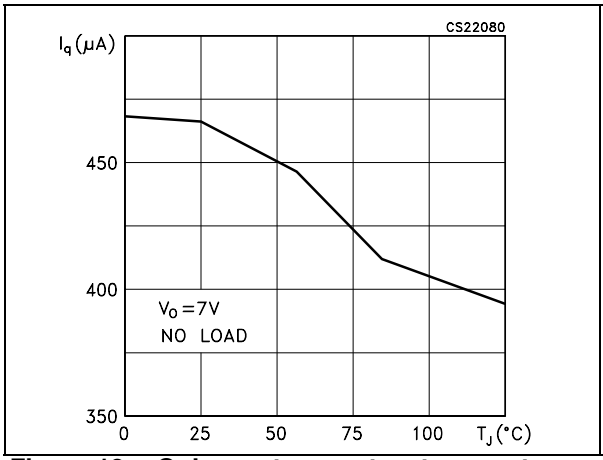


Figure 12. Quiescent current vs temperature

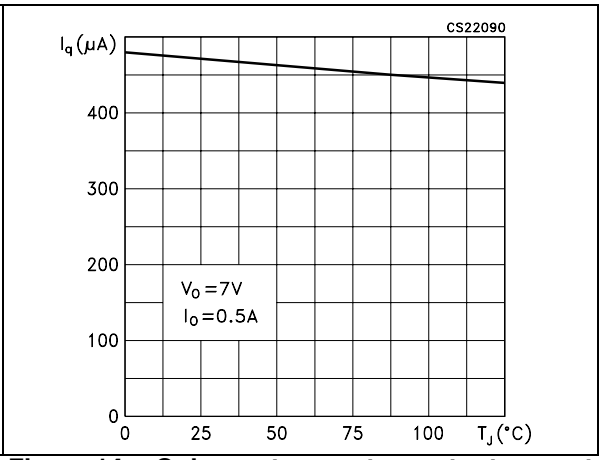


Figure 13. Quiescent current vs temperature

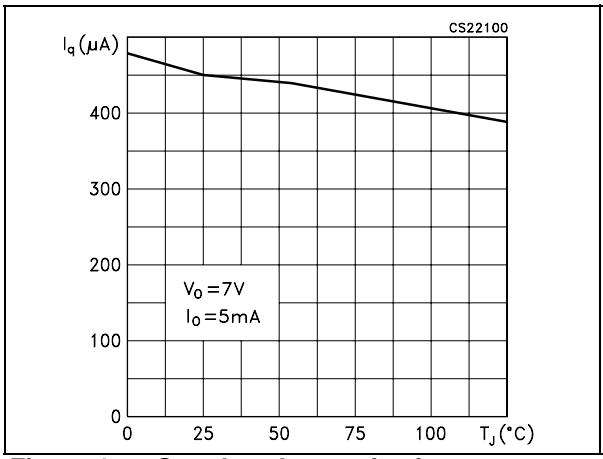


Figure 14. Quiescent current vs output current

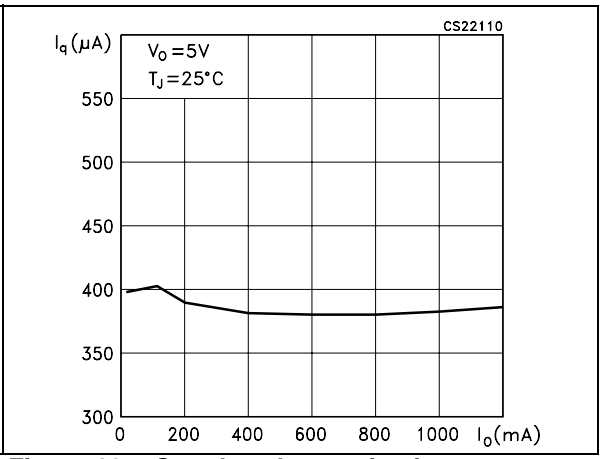


Figure 15. Supply voltage rejection vs temperature

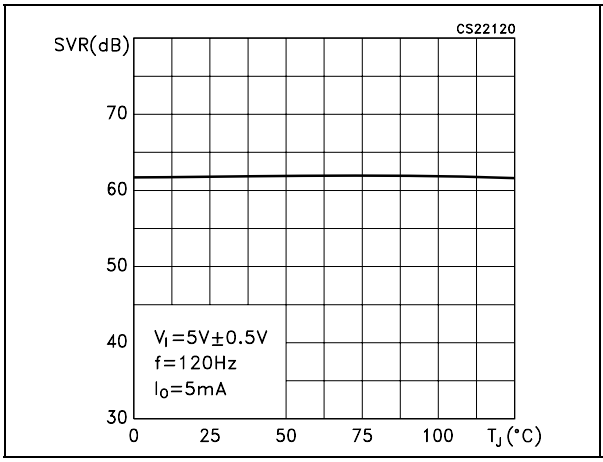


Figure 16. Supply voltage rejection vs frequency

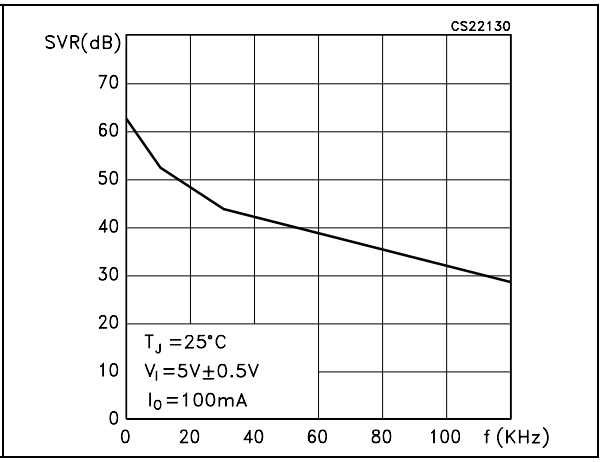


Figure 17. Output noise vs frequency

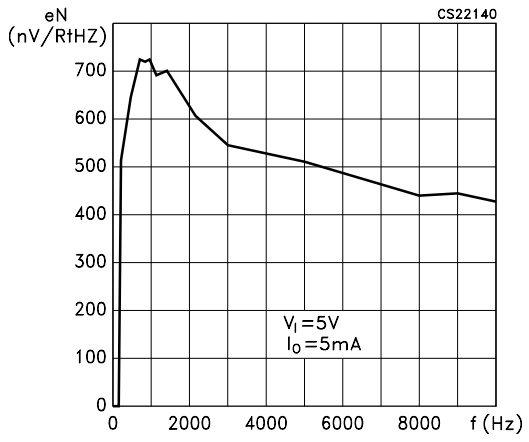
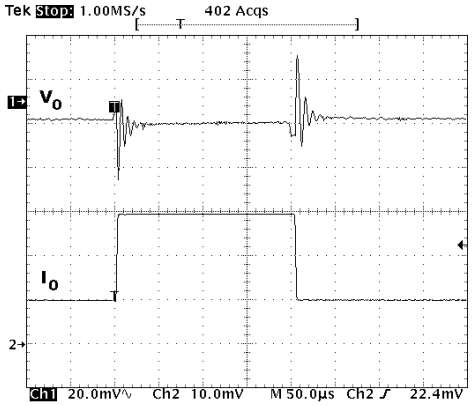
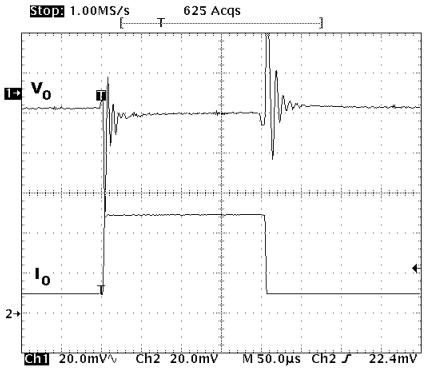


Figure 18. Change of V_O with step load change



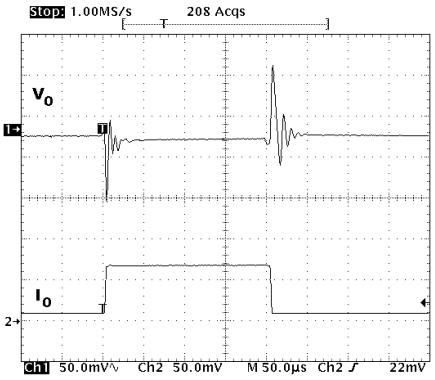
V_I=5V, I_O=100mA to 300mA, C_O=10μF, C_I=10μF, t_{RISE}≥1µs

Figure 19. Change of V_O with step load change



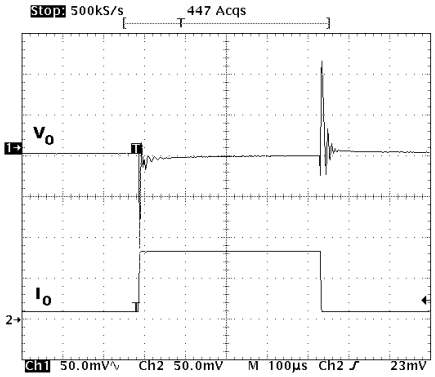
V_I=5V, I_O=300mA to 500mA, C_O=10µF, C_I=10µF, t_{RISE}≥1µs

Figure 20. Change of V_O with step load change



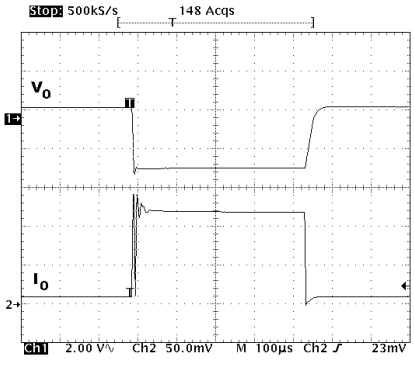
V_I=5V, I_O=500mA to 700mA, C_O=10µF, C_I=10µF, t_{RISE}≥1µs, T_J=25°C

Figure 21. Change of V_O with step load change



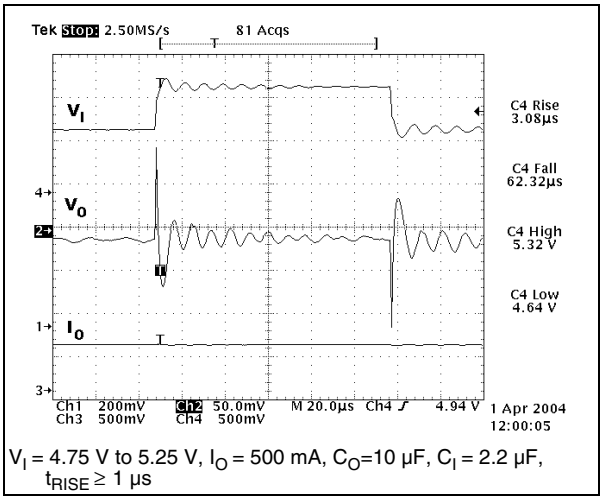
V_I=5V, I_O=700mA to 900mA, C_O=10µF, C_I=10µF, t_{RISE}≥1µs, T_J=25°C

Figure 22. Change of V_O with step load change



V_I=5V, I_O=10mA to S.C., C_O=10µF, C_I=10µF, t_{RISE}≥1µs, T_J=25°C

Figure 23. Line transient



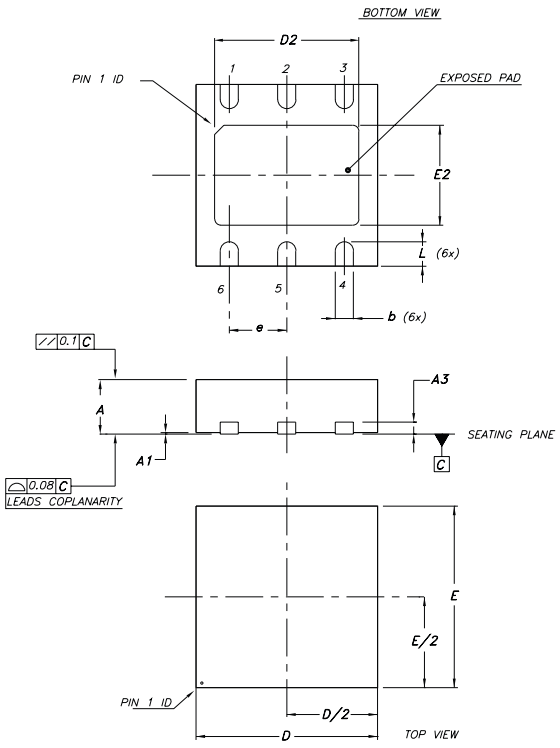
V_I = 4.75 V to 5.25 V, I_O = 500 mA, C_O=10 µF, C_I = 2.2 µF, $t_{RISE} \geq 1$ µs

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

DFN6D (3x3 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23		0.45	0.009		0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23		2.50	0.088		0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.75	0.059		0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020



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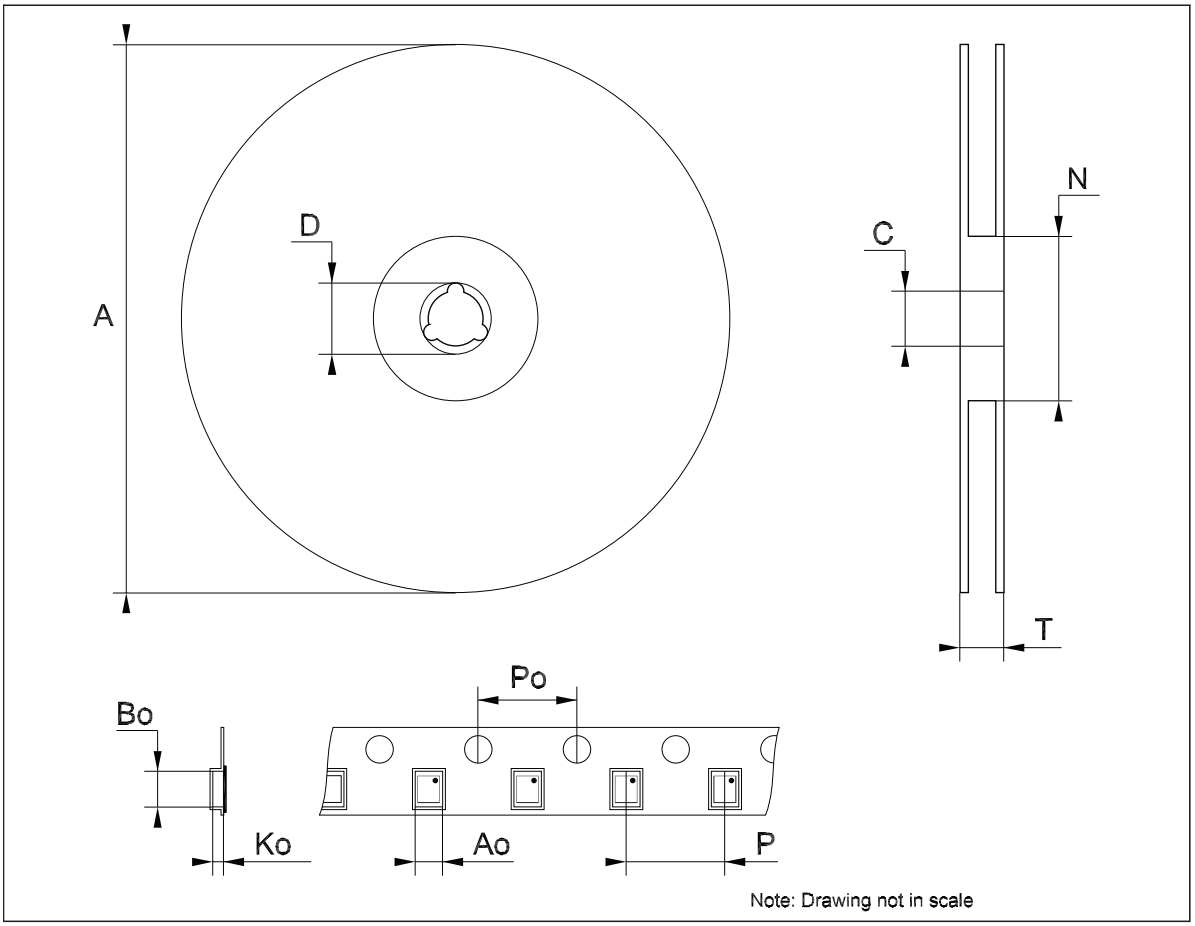
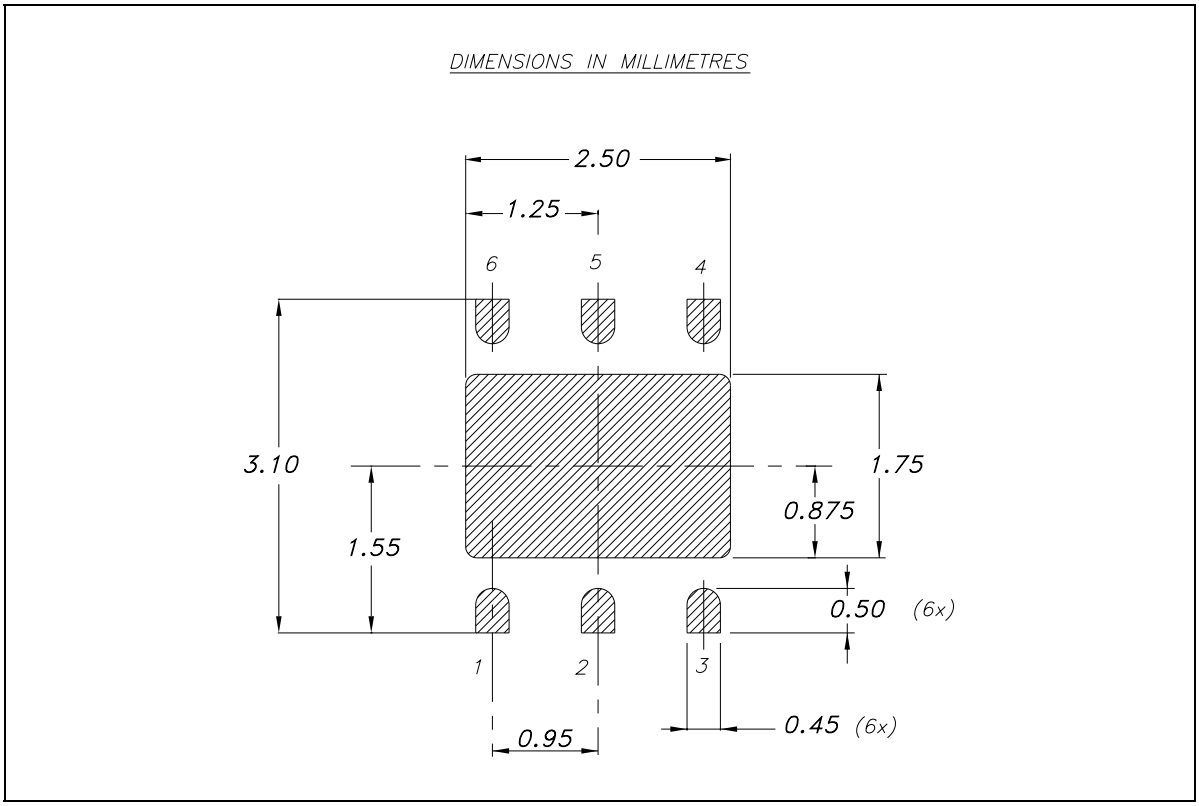
Tape & Reel QFNxx/DFNxx (3x3) Mechanical Data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 24. DFN6 (3x3 mm) footprint recommended data



8 Revision history

Table 8. Document revision history

Date	Revision	Changes
25-Feb-2005	1	First release.
10-Jan-2006	2	Add new order codes and tables of the electrical characteristics.
16-May-2006	3	General feature has been updated and add note 3 in table 6.
05-Jul-2006	4	Updated mechanical data DFN6 (3x3).
22-Feb-2007	5	Add note in *Figure 2* and in order codes.
03-Apr-2007	6	Add order codes and mechanical data DFN6D.
05-Sep-2007	7	Add *Table 1* in cover page.
12-Mar-2008	8	Removed: mechanical data DFN6.

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