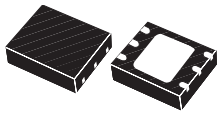
ST1L05 - ST1L05A
ST1L05B - ST1L05C - ST1L05D

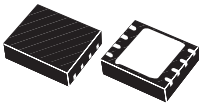
Very low quiescent BiCMOS voltage regulator

Features

- Fixed output voltage: 1.8 V, 2.5 V, 3.3 V and ADJ
- Output voltage tolerance: ± 2 % at 25 °C
- Output current capability: 1.3 A
- Very low quiescent current: max 650 µA Over temperature range
- Typ. dropout 0.3 V (@ I_O =1.3 A)
- Enable function for the B, C and D versions
- Power Good function for the B and D versions
- Stable with low ESR ceramic capacitors
- Thermal shutdown protection with hysteresis
- Overcurrent protection
- Operating junction temperature range: from 0 to 125 °C



DFN6 (3 x 3 mm)



DFN8 (4 x 4 mm)

Description

The ST1L05 family is a low drop linear voltage regulator capable of supplying up to 1.3 A output current.

The output voltage is fixed at 1.8 V, 2.5 V, 3.3 V and Adjustable. It is available in three different versions with different pin outs.

Thanks to BiCMOS technology, the quiescent current is controlled and maintained below 650 µA over the entire allowed junction temperature range. The ST1L05 is stable with low ESR output ceramic capacitors.

Internal protection circuitry includes thermal protection with hysteresis and overcurrent limiting.

The ST1L05 is especially suitable for data storage applications such as HDDs, where it can be used to supply the 3.3 V required by read channel and memory chips.

The regulator is available in the small and thin DFN6 (3 x 3) and DFN8 (4 x 4) packages.

Table 1. Device summary

Order codes	Packages	Output voltages
ST1L05PU25R	DFN6D (3 x 3 mm)	2.5 V
ST1L05APU33R	DFN6D (3 x 3 mm)	3.3 V
ST1L05BPUR	DFN6D (3 x 3 mm)	ADJ
ST1L05CPU33R	DFN6D (3 x 3 mm)	3.3 V
ST1L05DPUR	DFN8 (4 x 4 mm)	ADJ

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Contents

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1 Schematic diagrams

Figure 1. Schematic diagram for ST1L05

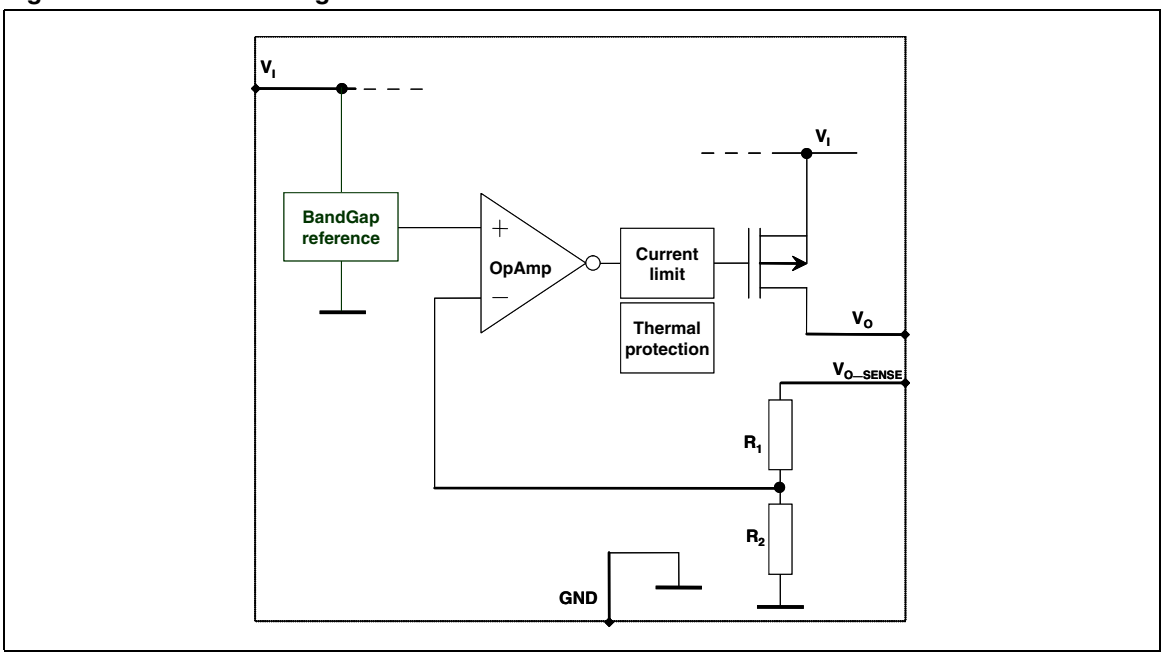

Figure 2. Schematic diagram for ST1L05A

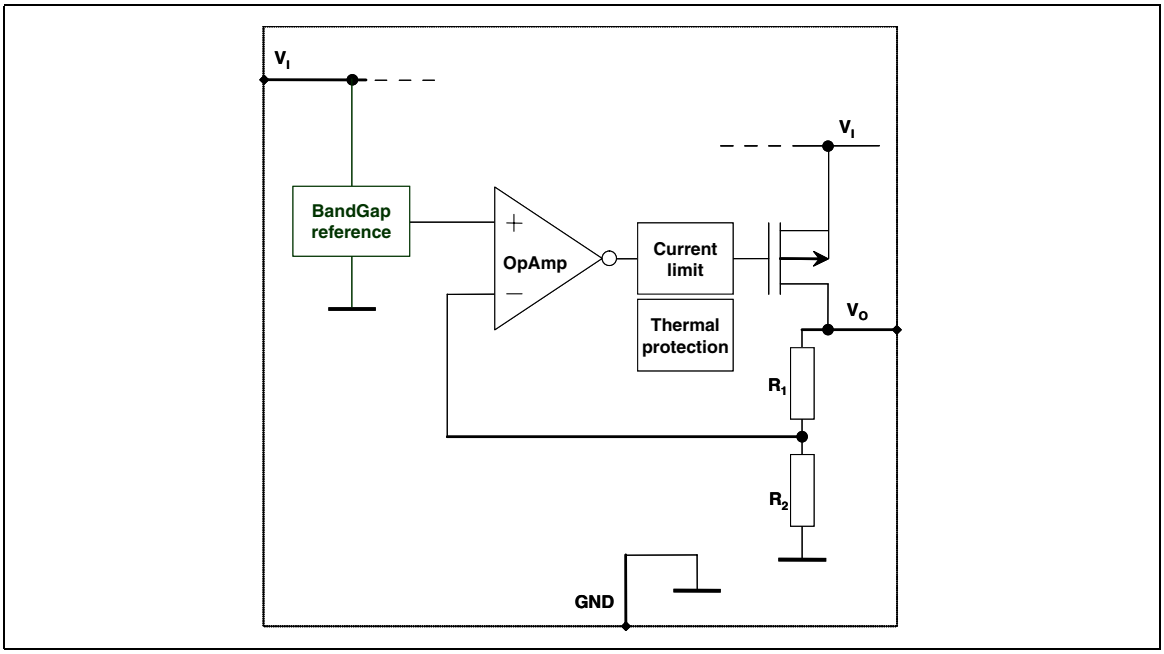

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Figure 3. Schematic diagram for ST1L05B and ST1L05D

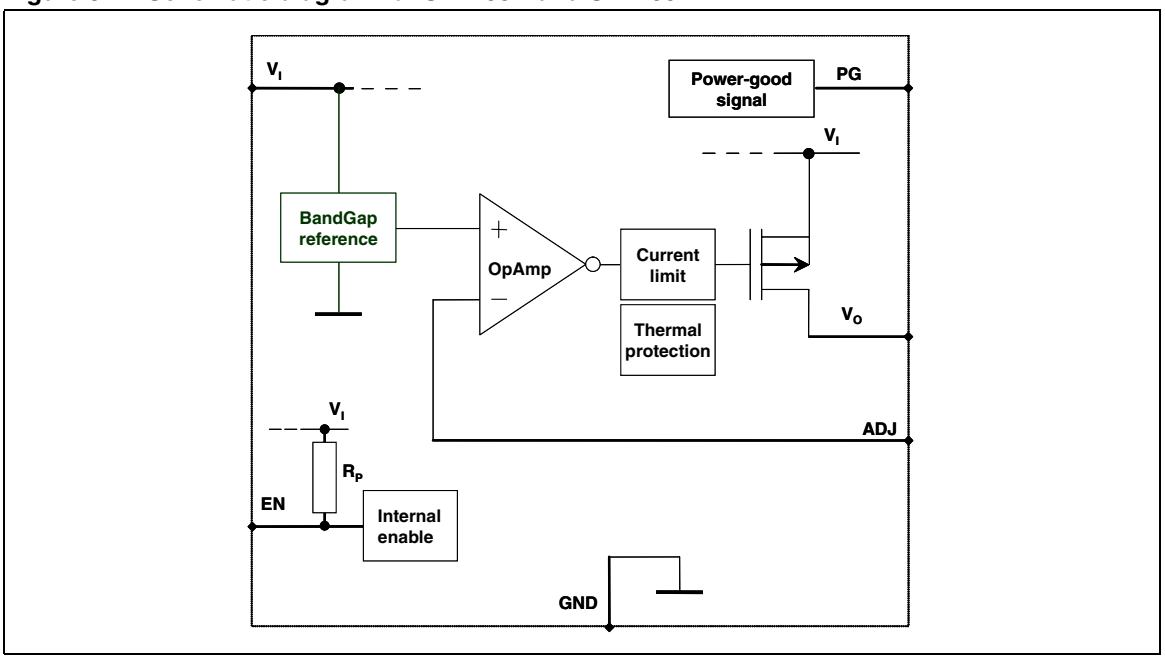
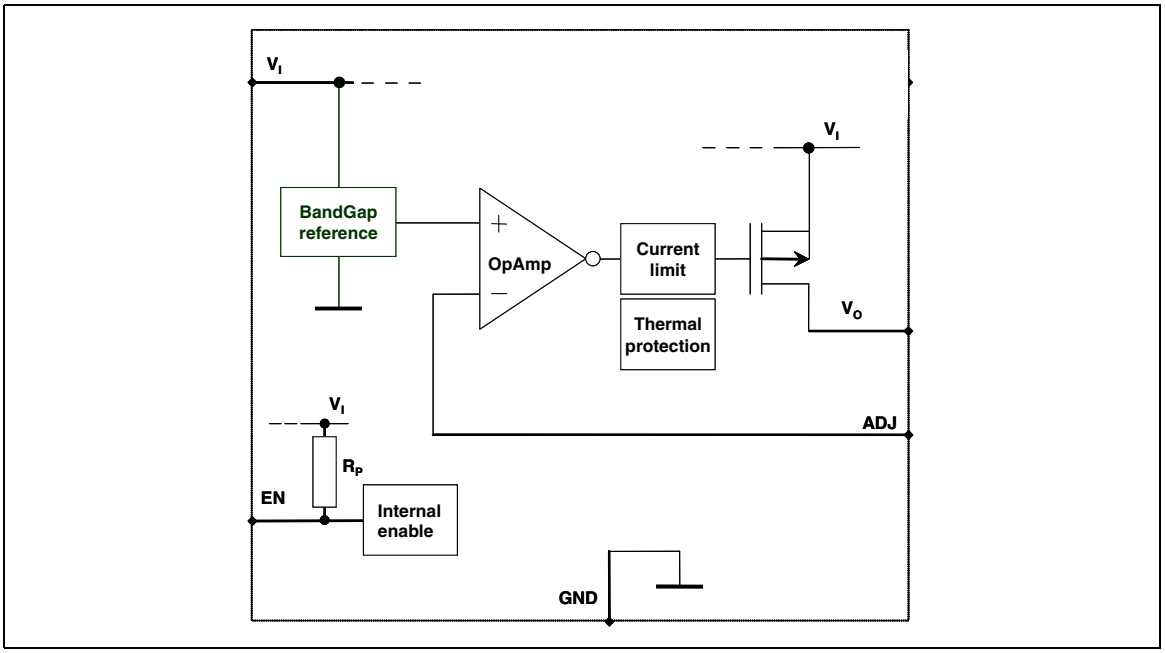


Figure 4. Schematic diagram for ST1L05C



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2 Pin configuration

Figure 5. Pin connections (top through view)

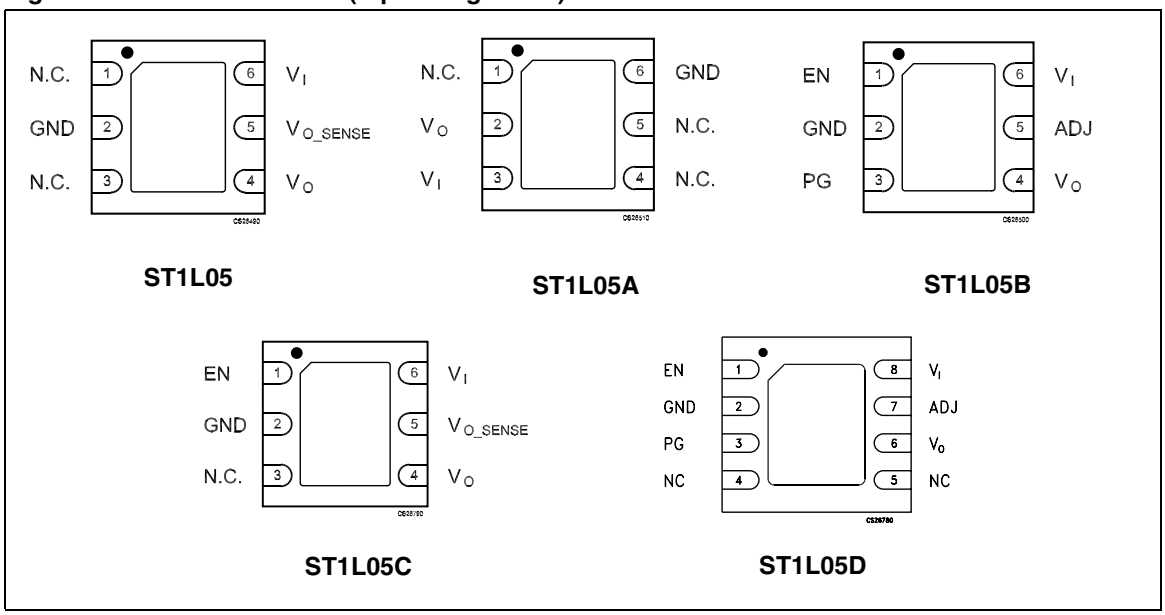

Table 2. Pin description

Symbol	Pin n°					Function
	ST1L05	ST1L05A	ST1L05B	ST1L05C	ST1L05D	
V_I	6	3	6	6	8	Supply voltage input pin. Bypass with a 4.7 µF capacitor to GND
V_O	4	2	4	4	6	Output voltage pin. Bypass with a 4.7 µF capacitor to GND
GND	2	6	2	2	2	Ground pin
ADJ	-	-	5	-	7	Adjust pin
V_{O_SENSE}	5	-	-	5	-	V_O sense
PG	-	-	3	-	3	Power Good pin
EN	-	-	1	1	1	Enable pin. Internal pull-up to V_I
NC	1,3	1,4,5	-	3	4, 5	Not connected
GND	EXP					Exposed pad must be connected to GND

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3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC supply voltage	-0.3 to 7	V
V_O	DC output voltage	-0.3 to 7	V
PG	Power Good pin	-0.3 to 7	V
EN	Enable pin	-0.3 to 7	V
ADJ/V_{OUT_SENSE}	Adjust pin or V_O sense	4	V
P_D	Power dissipation	internally limited	W
I_O	Output current	internally limited	A
T_{OP}	Operating junction temperature range	0 to 150	°C
T_{STG}	Storage temperature range (1)	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 Sec.	260	°C

1. Storage temperature > 125 °C are acceptable only if the regulator is soldered to a PCBA.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	DFN6	DFN8	Unit
R_{thJC}	Thermal resistance junction-case	10	4	°C/W
R_{thJA}	Thermal resistance junction-ambient	55	40	°C/W

Table 5. ESD data

Symbol	Parameter	Value	Unit
HBM	Human body model	2	kV
MM	Machine model	150	V

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4 Electrical characteristics

Refer to the typical application schematic, V_I = 3.3 V to 4.5 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Typical values are intended at T_J = 25 °C unless otherwise specified.

Table 6. Electrical characteristics for the ST1L05PU25

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I =3.3V to 5.25V, T=25°C	2.45	2.5	2.55	V
V_O	Output voltage	V_I = 3.3V to 5.25V	2.4375	2.5	2.5625	V
ΔV_O	Line regulation	V_I = 4.75V to 5.25V			15	mV
ΔV_O	Load regulation	V_I = 4.75V, I_O = 10mA to 1.3A		15	30	mV
I_S	Output current limit	V_I = 5.5V	1.3			A
I_{OMIN}	Minimum output current for regulation				0	mA
V_d	Dropout voltage	I_O = 0.8A		0.2	0.4	V
		I_O = 1A		0.25	0.45	V
		I_O = 1.3A		0.3	0.5	V
I_Q	Quiescent current	V_I = 5V, I_O = 2mA to 1.3A, T=25°C		350	500	µA
		V_I = 5.5V, I_O = 2mA to 1.3A		350	650	
SVR	Supply voltage rejection (1)	V_I = 5±0.5V, I_O = 5mA, f=120Hz	50	68		dB
eN	RMS output noise (1)	B = 10Hz to 10kHz, V_I = 5V, I_O=5mA		0.003		%V_O
$\Delta V_O/\Delta I_O$	Load transient (rising) (1)(2)	V_I =5V, any 200mA step from 100mA to 1.3A, $t_R \geq$ 1µs			5	%V_O
$\Delta V_O/\Delta I_O$	Load transient (falling) (1)(2)	V_I =5V, I_O = 1.3A to 10mA, $t_F \geq$ 1µs			2.75	V
$\Delta V_O/\Delta V_I$	Start-up transient (1)(2)	V_I =0V to 5V, I_O = 10mA to 1.3A, $t_R \geq$ 1µs			2.75	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (1)(2)	V_I =5V, I_O = short to 10mA			2.75	V
T_{SH}	Thermal shutdown trip point (1)	V_I =5V		165		°C

1. Guaranteed by design. Not tested in production
2. C_I =10µF, C_O =10µF, all X7R ceramic capacitors.

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Refer to the typical application schematic, V_I = 4.5 V to 5.5 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified). Typical values are intended at T_J = 25 °C unless otherwise specified.

Table 7. Electrical characteristics for ST1L05APU33

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75V to 5.25V, T=25°C	3.234	3.3	3.366	V
V_O	Output voltage	V_I = 4.75V to 5.25V	3.2175	3.3	3.3825	V
ΔV_O	Line regulation	V_I = 4.75V to 5.25V			15	mV
ΔV_O	Load regulation	V_I = 4.75V, I_O = 10mA to 1.3A		15	30	mV
I_S	Output current limit	V_I = 5.5V	1.3			A
I_{OMIN}	Minimum output current for regulation				0	mA
V_d	Dropout voltage	I_O = 0.8A		0.2	0.4	V
		I_O = 1A		0.25	0.45	V
		I_O = 1.3A		0.3	0.5	V
I_Q	Quiescent current	V_I = 5V, I_O = 2mA to 1.3A, T=25°C		350	500	µA
		V_I = 5.5V, I_O = 2mA to 1.3A		350	650	
SVR	Supply voltage rejection (1)	V_I = 5±0.5V, I_O = 5mA, f=120Hz	50	65		dB
eN	RMS output noise (1)	B = 10Hz to 10kHz, V_I = 5V, I_O =5mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising) (1)(2)	V_I =5V, any 200mA step from 100mA to 1.3A, $t_R \geq$ 1µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling) (1)(2)	V_I =5V, I_O = 1.3A to 10mA, $t_F \geq$ 1µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient (1)(2)	V_I =0V to 5V, I_O = 10mA to 1.3A, $t_R \geq$ 1µs			3.5	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (1)(2)	V_I =5V, I_O = short to 10mA			3.5	V
T_{SH}	Thermal shutdown trip point(1)	V_I =5V		165		°C

1. Guaranteed by design. Not tested in production.
2. C_I =10µF, C_O =10µF, all X7R ceramic capacitors.

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Refer to the typical application schematic, V_I = 4.5 V to 5.5 V, V_{EN} = 2 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Typical values are intended at T_J = 25 °C unless otherwise specified.

Table 8. Electrical characteristics for the ST1L05CPU33

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75V to 5.25V, T=25°C	3.234	3.3	3.366	V
V_O	Output voltage	V_I = 4.75V to 5.25V	3.2175	3.3	3.3825	V
ΔV_O	Line regulation	V_I = 4.75V to 5.25V			15	mV
ΔV_O	Load regulation	V_I = 4.75V, I_O = 10mA to 1.3A		15	30	mV
I_S	Output current limit	V_I = 5.5V	1.3			A
I_{OMIN}	Minimum output current for regulation				0	mA
V_d	Dropout voltage	I_O = 0.8A		0.2	0.4	V
		I_O = 1A		0.25	0.45	V
		I_O = 1.3A		0.3	0.5	V
I_Q	Quiescent current	V_I = 5V, I_O = 2mA to 1.3A, T=25°C		350	500	µA
		V_I = 5.5V, I_O = 2mA to 1.3A		350	650	
V_{EN_H}	Enable threshold high	V_I=4.5V to 5.25, I_O = 50mA	2			V
V_{EN_L}	Enable threshold low	V_I=4.5V to 5.25, I_O= 50mA			0.8	
I_{EN}	Enable pin current	V_{EN}=V_I = 5V			2	µA
SVR	Supply voltage rejection (1)	V_I = 5±0.5V, I_O = 5mA, f=120Hz	50	65		dB
eN	RMS output noise (1)	B = 10Hz to 10kHz, V_I = 5V, I_O =5mA		0.003		%V_O
$\Delta V_O/\Delta I_O$	Load transient (rising) (1)(2)	V_I =5V, any 200mA step from 100mA to 1.3A, $t_R \geq$ 1µs			5	%V_O
$\Delta V_O/\Delta I_O$	Load transient (falling) (1)(2)	V_I =5V, I_O = 1.3A to 10mA, $t_F \geq$ 1µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient (1)(2)	V_I =0V to 5V, I_O = 10mA to 1.3A, $t_R \geq$ 1µs			3.5	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (1)(2)	V_I =5V, I_O = short to 10mA			3.5	V
T_{SH}	Thermal shutdown trip point(1)	V_I =5V		165		°C

1. Guaranteed by design. Not tested in production.
2. C_I =10µF, C_O =10µF, all X7R ceramic capacitors.

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Refer to the typical application schematic, V_I = 3 V to 5.5 V, V_{EN} = 2 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Typical values are intended at T_J = 25 °C unless otherwise specified.

Table 9. Electrical characteristics for the ST1L05BPU and ST1L05DPU

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 3V to 5.25V, T=25°C	1.195	1.22	1.245	V
V_O	Output voltage	V_I = 3V to 5.25V	1.18	1.22	1.256	V
ΔV_O	Line regulation	V_I = 4.75V to 5.25V			15	mV
ΔV_O	Load regulation	V_I = 4.75V, I_O = 10mA to 1.3A		15	30	mV
I_{ADJ}	Adjust pin current	V_I = 3V to 5.25V		1		nA
I_S	Output current limit	V_I = 5.5V	1.3			A
I_{OMIN}	Minimum output current for regulation				1	mA
V_d	Dropout voltage (1)	I_O = 0.8A, V_O=3.3V		0.2		V
		I_O = 1A, V_O=3.3V		0.25		V
		I_O = 1.3A, V_O=3.3V		0.3		V
I_Q	Quiescent current	V_I = 5V, I_O = 2mA to 1.3A, T=25°C		300	500	µA
		V_I = 5.5V, I_O = 2mA to 1.3A		350	650	
		Device OFF(2)			1	
V_{EN_H}	Enable threshold high	V_I=3V to 5.25, I_O = 50mA	2			V
V_{EN_L}	Enable threshold low	V_I=3V to 5.25, I_O= 50mA			0.8	
I_{EN}	Enable pin current	V_{EN}=V_I = 5V			2	µA
PG	Power Good output threshold	Rising edge		0.92V_O		V
		Falling edge		0.8V_O		
	Power Good output voltage low(3)	I_{SINK}=6mA open drain output			0.4	V
SVR	Supply voltage rejection (3)	V_I = 5±0.5V, I_O = 5mA, f=120Hz	50	72		dB
eN	RMS output noise (3)	B = 10Hz to 10kHz, V_I = 5V, I_O=5mA		0.003		%V_O
$\Delta V_O/\Delta I_O$	Load transient (rising) (3)(4)	V_I =5V, any 200mA step from 100mA to 1.3A, $t_R \geq$ 1µs			5	%V_O
$\Delta V_O/\Delta I_O$	Load transient (falling) (3)(4)	V_I =5V, I_O = 1.3A to 10mA, $t_F \geq$ 1µs			1.38	V
$\Delta V_O/\Delta V_I$	Start-up transient (3)(4)	V_I =0V to 5V, I_O = 10mA to 1A, $t_R \geq$ 1µs			1.38	V
$\Delta V_O/\Delta I_O$	Short circuit removal response (3)(4)	V_I =5V, I_O = short to 10mA			1.38	V
T_{SH}	Thermal shutdown trip point (3)	V_I =5V		165		°C

1. See minimum start-up voltage, V_I = 2.9V.
2. PG pin floating
3. Guaranteed by design. Not tested in production.
4. C_I =10µF, C_O =10µF, all X7R ceramic capacitors.

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5 Typical characteristics

Figure 6. Output voltage vs. temperature

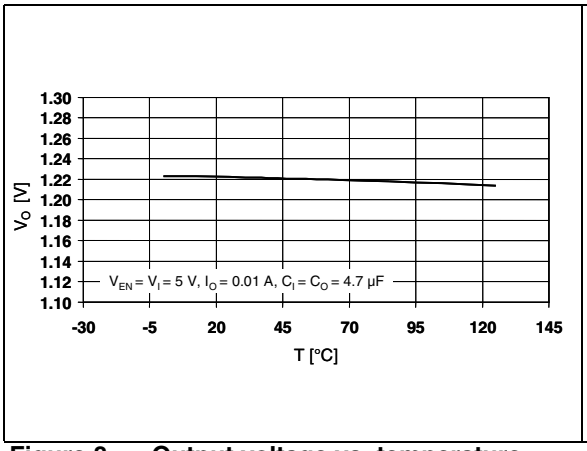

Figure 7. Output voltage vs. temperature

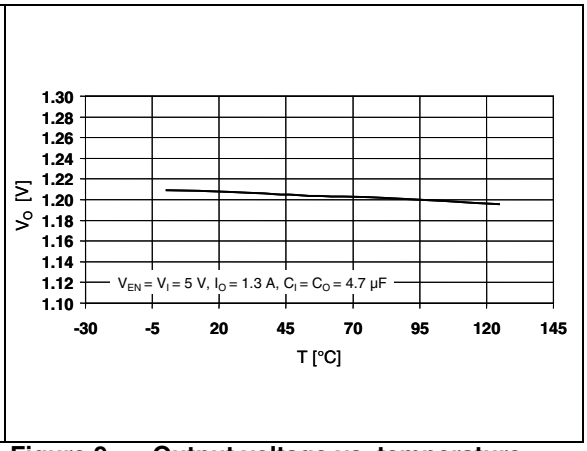

Figure 8. Output voltage vs. temperature

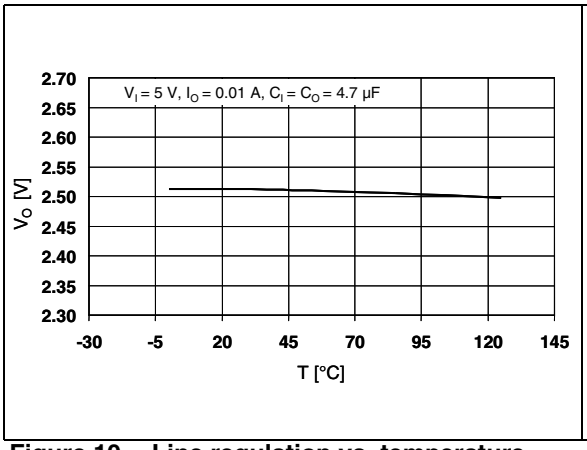

Figure 9. Output voltage vs. temperature

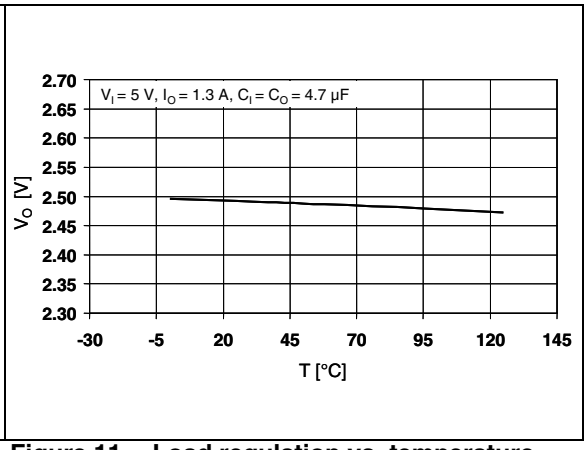

Figure 10. Line regulation vs. temperature

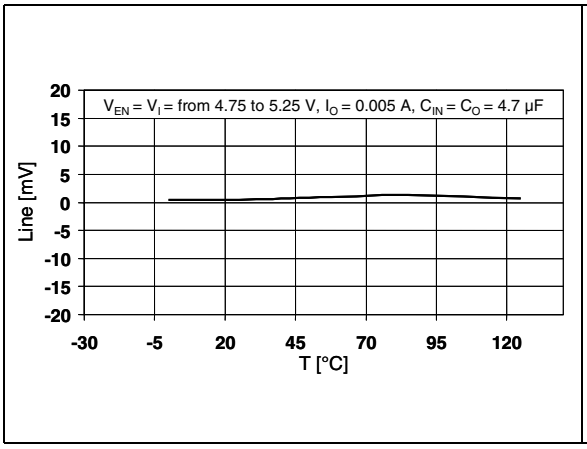

Figure 11. Load regulation vs. temperature

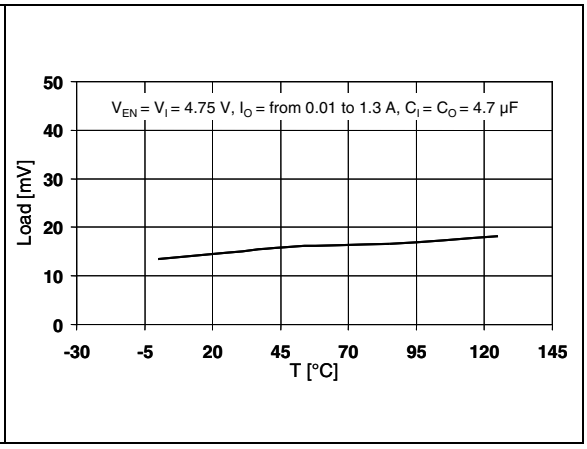

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Figure 12. Dropout voltage vs. temperature

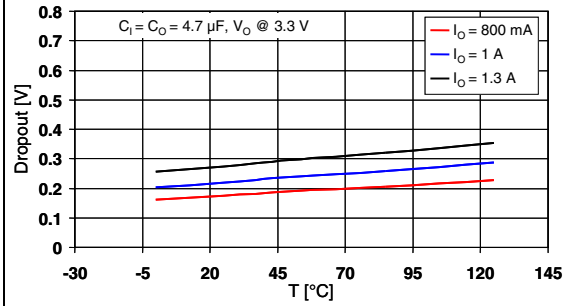

Figure 13. ESR required for stability with ceramic capacitors

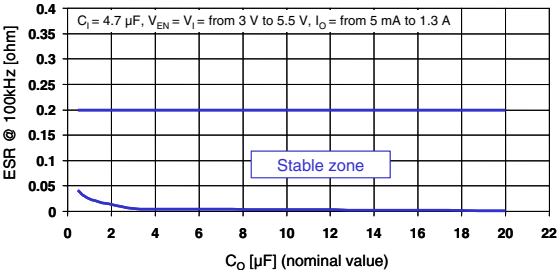

Figure 14. Quiescent current vs. temperature

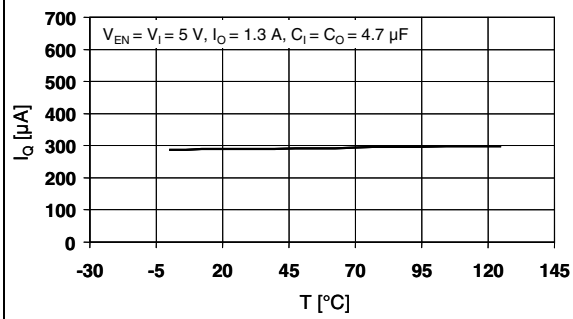

Figure 15. Quiescent current vs. output current

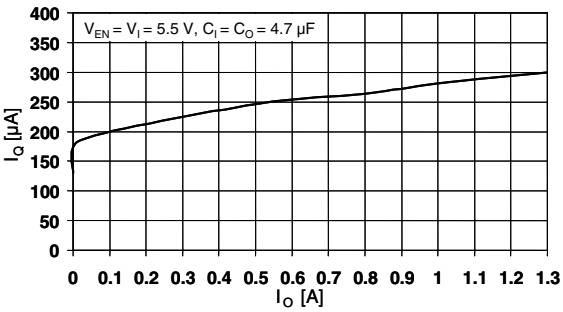

Figure 16. Enable voltage vs. temperature

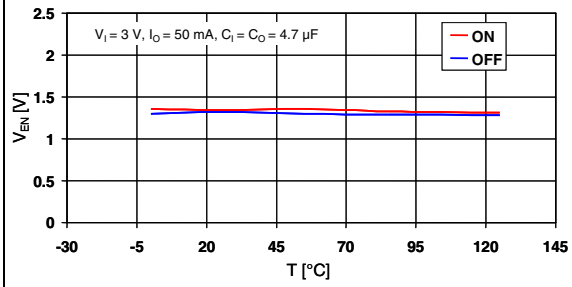

Figure 17. Enable voltage vs. temperature

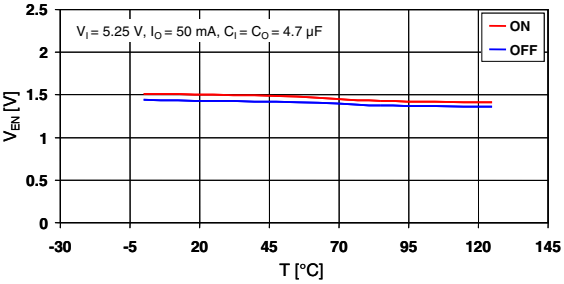

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Figure 18. Supply voltage rejection vs. temperature

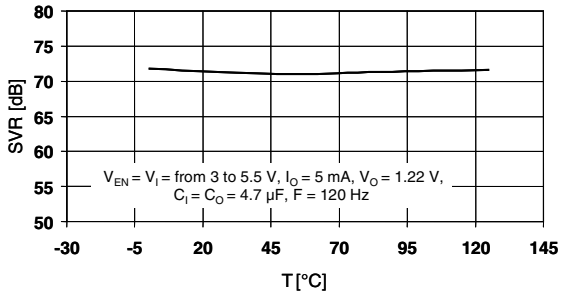


Figure 19. Supply voltage rejection vs. frequency

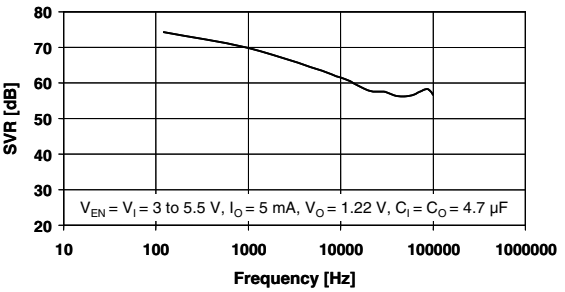
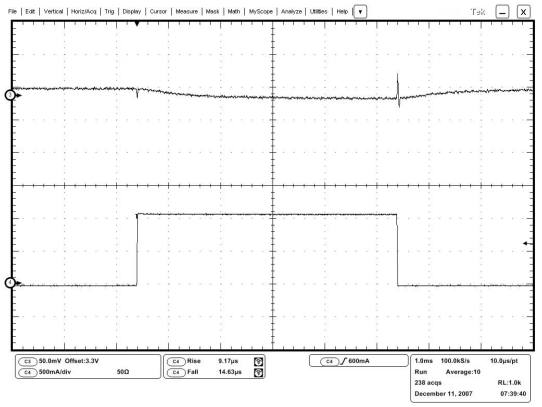
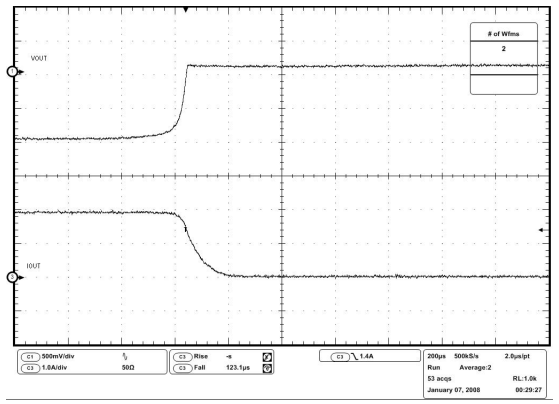


Figure 20. Load transient



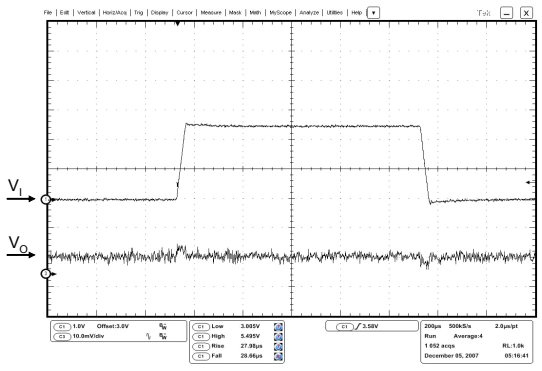
I_O=10 mA to 1.3 A, C_I=C_O=10 µF, V_{EN}=V_I=5 V, V_O@3.3 V

Figure 21. Short-circuit removal transient



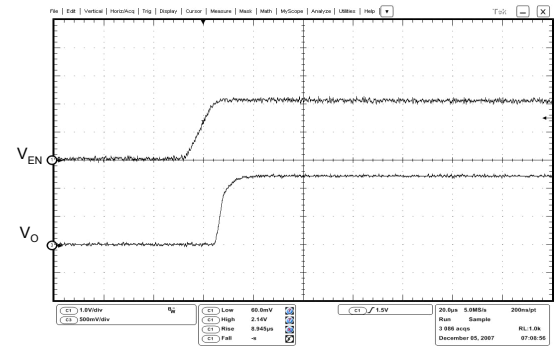
I_O=10 mA to short, C_I=C_O=10 µF, V_{EN}=V_I=5.5 V

Figure 22. Line transient



C_I=C_O=4.7 µF, V_I=3 to 5.5V, I_O=5 mA

Figure 23. Enable transient



C_O=C_I=4.7 µF, V_{EN}=0 to 2 V, V_I=5.5 V, I_O=5 mA

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6 Application information

The ST1L05 is a low dropout linear regulator. It provides up to 1.3 A with a low 300 mV dropout. The input voltage range is from 3 V to 5.5 V. The device is available in fixed and adjustable output versions.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

The regulator is designed to be stable with ceramic capacitors on the input and the output. The expected values of the input and output ceramic capacitors are from 1 µF to 22 µF with 4.7 µF typical. The input capacitor must be connected within 0.5 inches of the V_I terminal. The output capacitor must also be connected within 0.5 inches of output pin. There is no upper limit to the value of the input capacitor.

Figure 24, *Figure 25*, *Figure 26* and *Figure 27* illustrate the typical application schematics:

Figure 24. Application schematic for the ST1L05

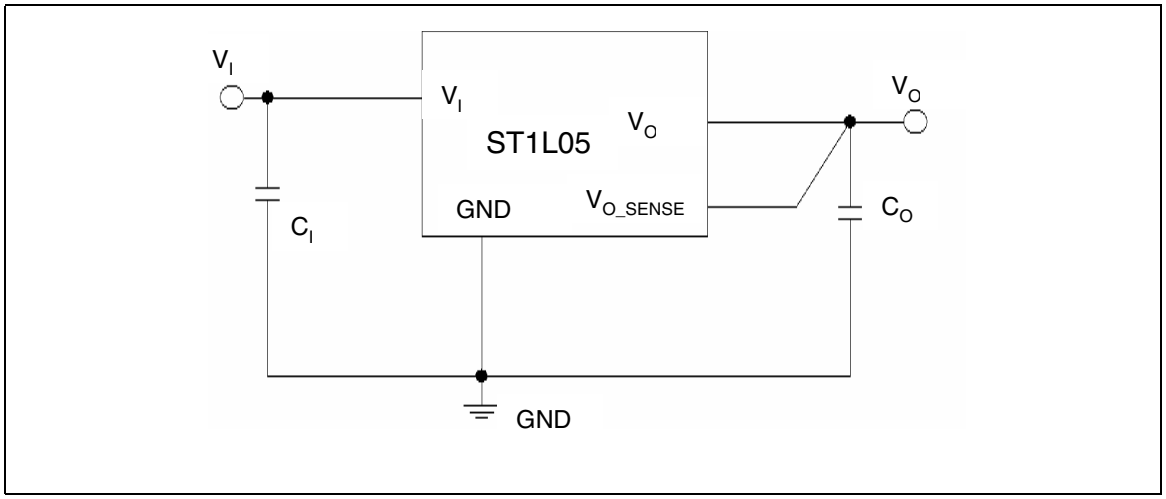

Figure 25. Application schematic for the ST1L05A

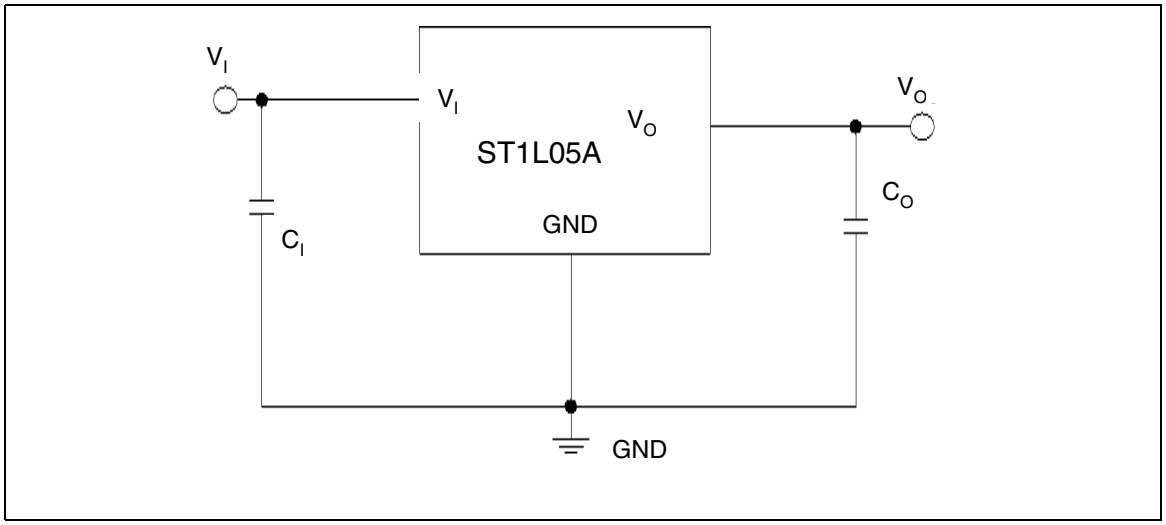

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Figure 26. Application schematic for the ST1L05B and ST1L05D

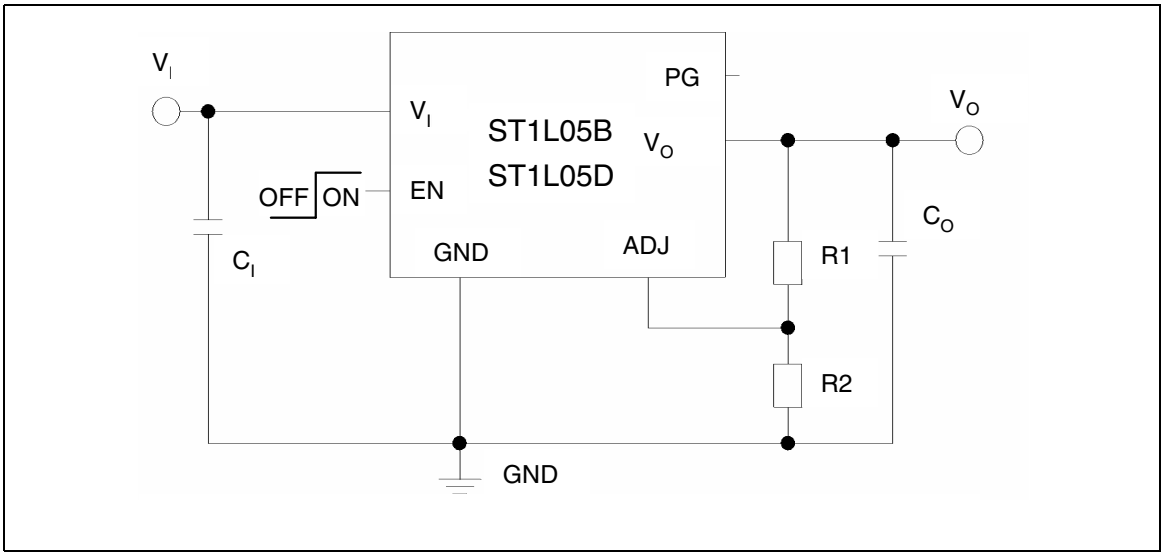
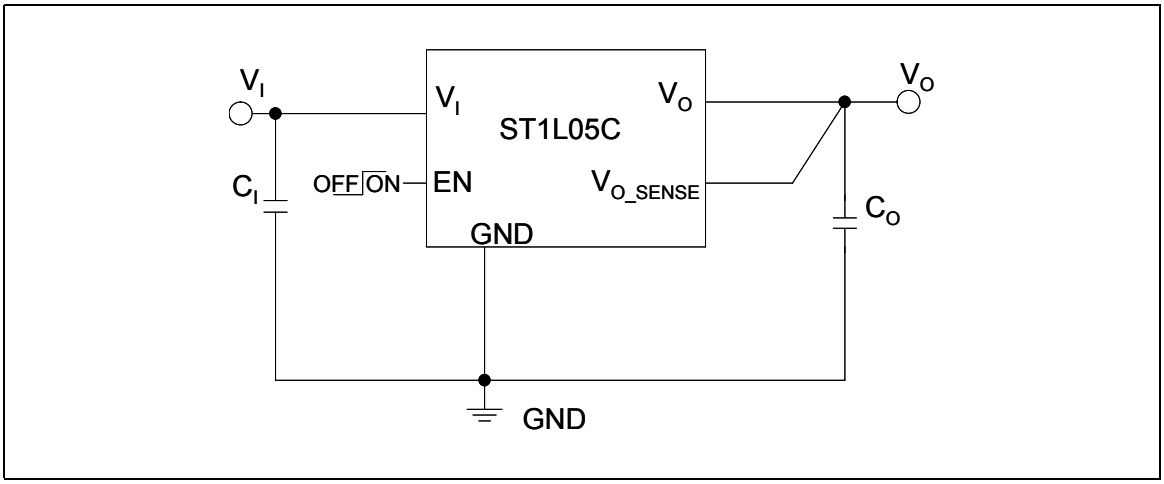


Figure 27. Application schematic for the ST1L05C



For the adjustable version, the output voltage can be adjusted from 1.22 V up to the input voltage, minus the voltage drop across the PMOS (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider should be selected using the following equation:

$V_O = V_{ADJ} (1 + R_1 / R_2)$ with $V_{ADJ} = 1.22$ V (typ.)

It is recommended to use resistors with values in the range of 10 kΩ to 100 kΩ. Lower values can also be suitable, but will increase current consumption.

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6.1 Power dissipation

An internal thermal feedback loop disables the output voltage if the die temperature rises to approximately 165 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device.

It is very important to use a good PC board layout to maximize the power dissipation. The thermal path for the heat generated by the device is from the die to the copper lead frame through the package leads and exposed pad to the PC board copper. The PC board copper acts as a heat sink. The footprint copper pads should be as wide as possible to spread and dissipate the heat to the surrounding ambient. Feed-through vias to inner or backside copper layers are also useful in improving the overall thermal performance of the device.

The power dissipation of the device depends on the input voltage, output voltage and output current, and is given by:

$P_D = (V_I - V_O) I_O$

The junction temperature of device will be:

$T_{J\_MAX} = T_A + R_{thJA} \times P_D$

where:

T_{J_MAX} is the maximum junction of the die,125 °C;

T_A is the ambient temperature;

R_{thJA} is the thermal resistance junction-to-ambient.

6.2 Enable function (ST1L05B, ST1L05C and ST1L05D only)

The ST1L05B, ST1L05C and ST1L05D features an enable function. When the EN voltage is higher than 2 V the device is ON, and if it is lower than 0.8 V the device is OFF. In shutdown mode, consumption is lower than 1 µA.

The EN pin has an internal pull-up, which means that it can be left floating if it is not used.

6.3 Power Good function (ST1L05B and ST1L05D only)

Most applications require a flag showing that the output voltage is in the correct range.

The Power Good threshold depends on the adjust voltage. When the adjust is higher than $0.92*V_{ADJ}$, the Power Good (PG) pin goes to high impedance. If the adjust is below $0.92*V_{ADJ}$ the PG pin goes in low impedance. If the device is functioning well, the Power Good pin is at high impedance.

If the output voltage is fixed using an external or internal resistor divider, the Power Good threshold is $0.92*V_O$.

The use of the Power Good function requires an external pull-up resistor, which must be connected between the PG pin and V_I or V_O. The typical current capability of the PG pin is up to 6 mA. The use of a pull-up resistor for PG in the range of 100 kΩ to 1 MΩ is recommended. If the Power Good function is not used, the PG pin must remain floating.

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7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

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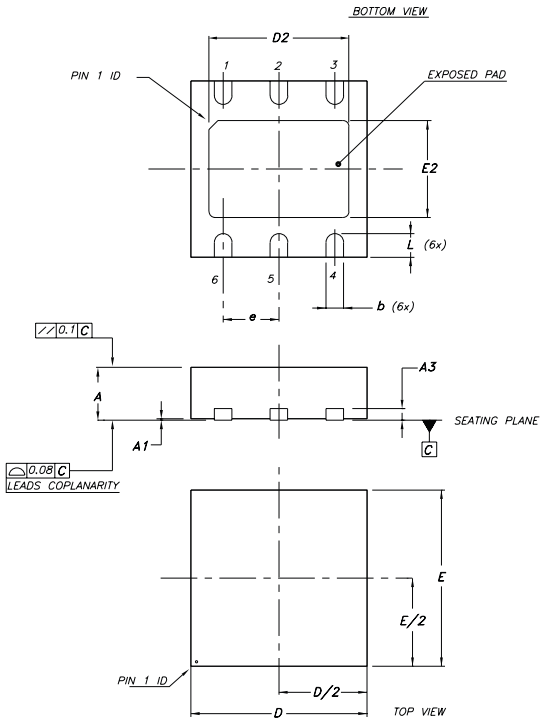
DFN6D (3x3 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23		0.45	0.009		0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23		2.50	0.088		0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.75	0.059		0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020



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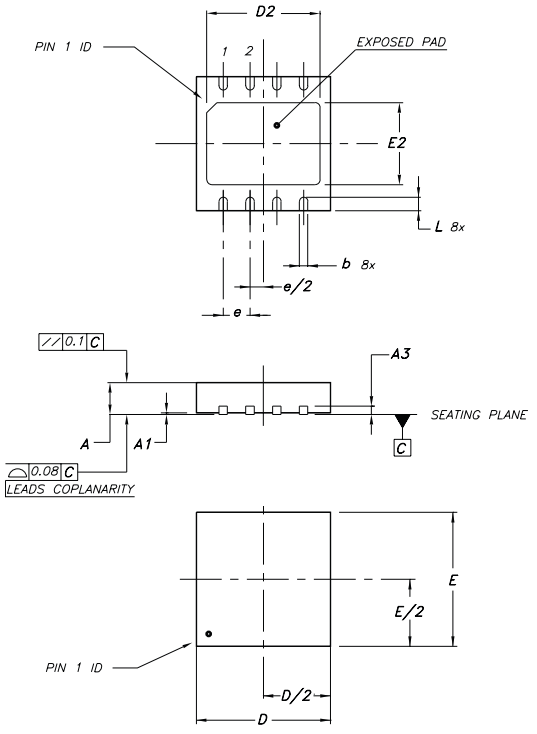
DFN8 (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23	0.30	0.38	0.009	0.012	0.015
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.82	3.00	3.23	0.111	0.118	0.127
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.05	2.20	2.30	0.081	0.087	0.091
e		0.80			0.031	
L	0.40	0.50	0.60	0.016	0.020	0.024



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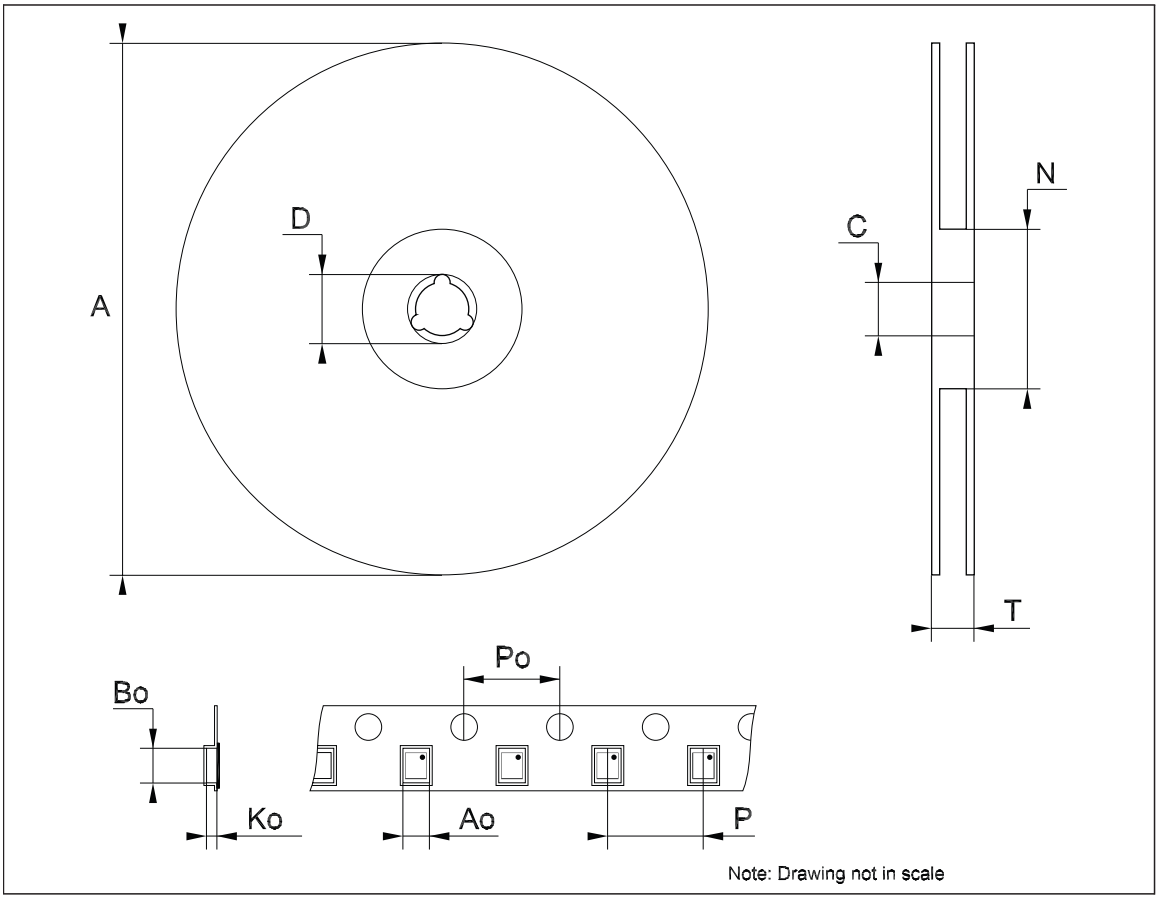
Tape & Reel QFNxx/DFNxx (3x3) Mechanical Data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



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Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

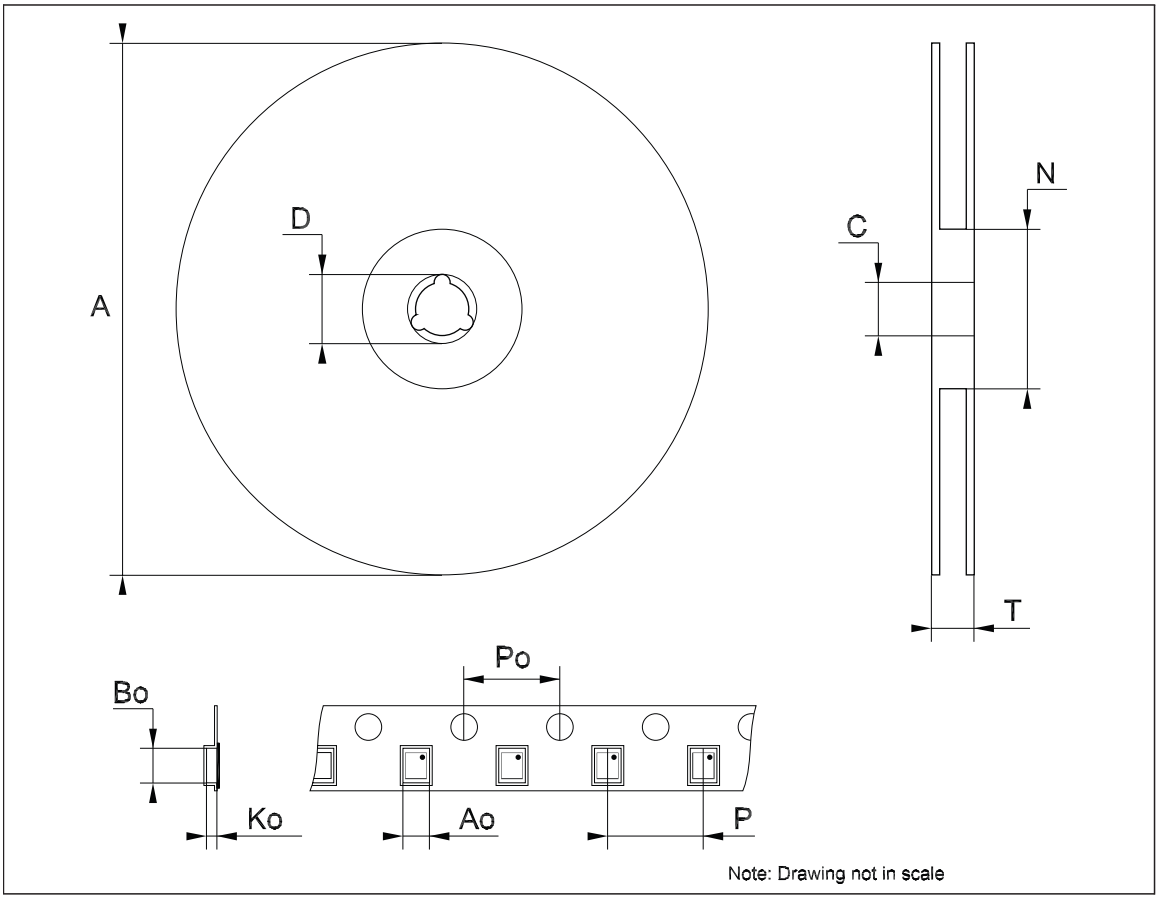

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Figure 28. DFN6 (3x3) footprint recommended data

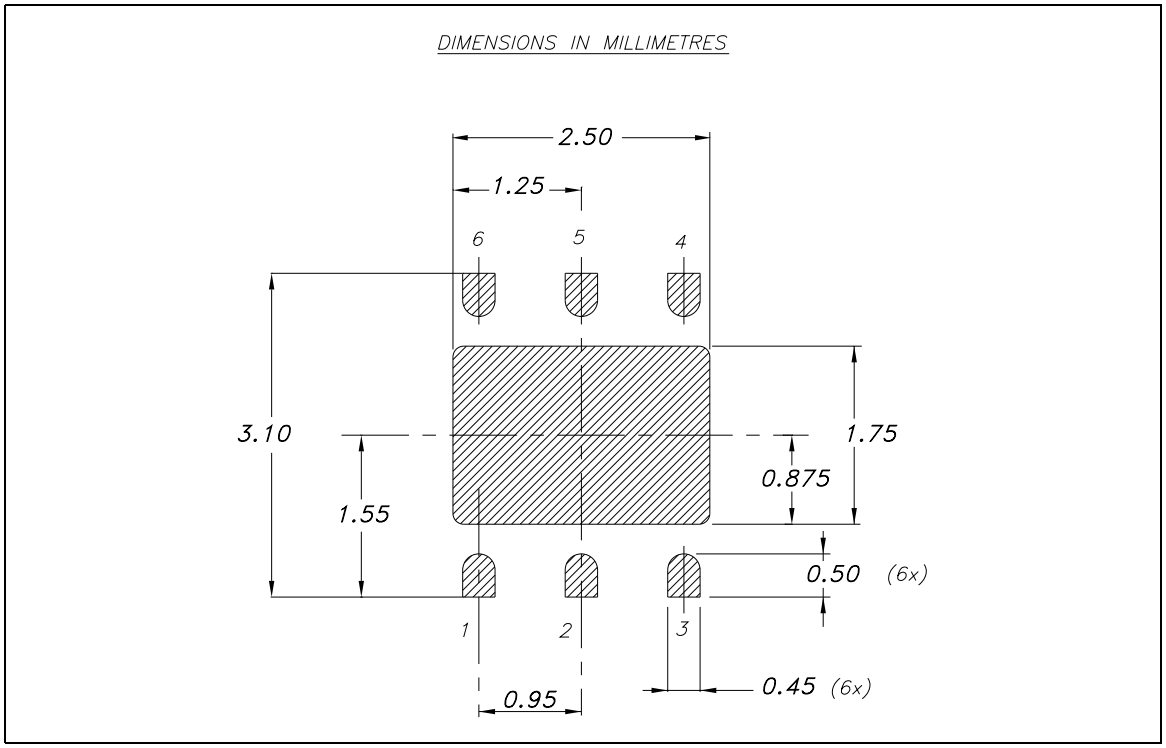
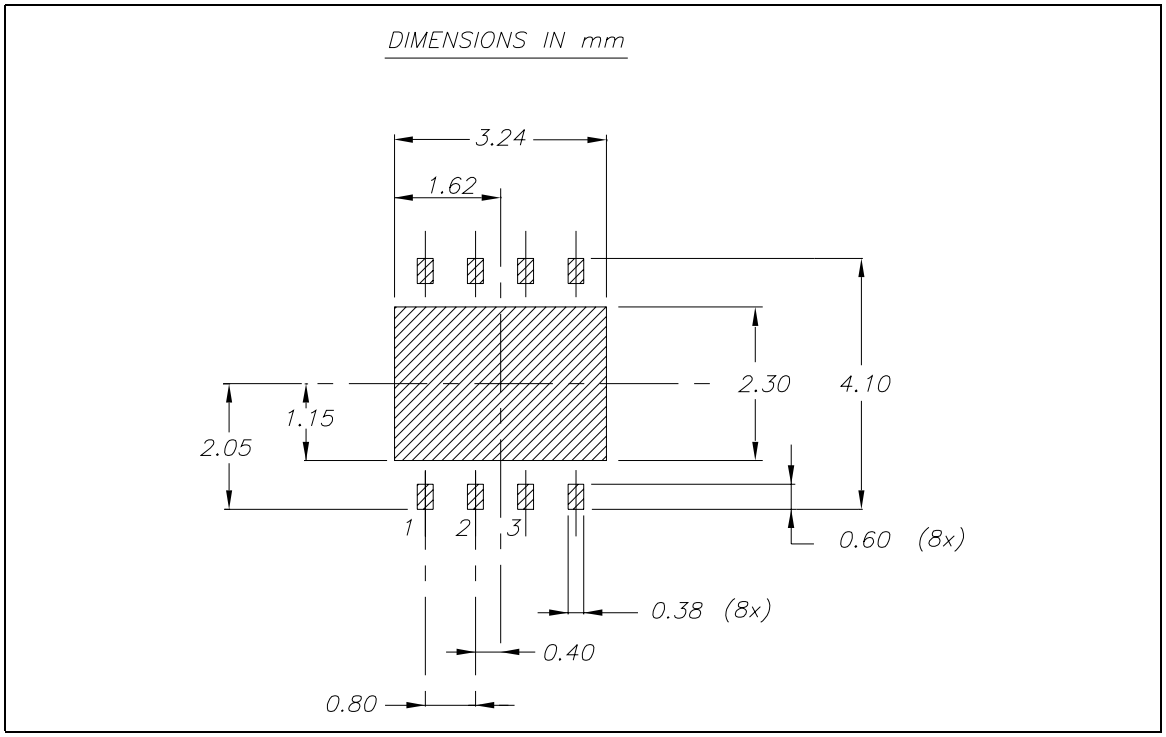


Figure 29. DFN8 (4 x 4) footprint recommended data



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8 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Feb-2008	1	First release.
08-Sep-2009	2	Modified *Table 1 on page 1*.

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