STSR30

SYNCHRONOUS RECTIFIER SMART DRIVER FOR FLYBACK

- SUPPLY VOLTAGE RANGE: 4V TO 5.5V
- TYPICAL PEAK OUTPUT CURRENT: (SOURCE-SINK: 1.5A)
- OPERATING FREQUENCY: 20 TO 500 KHz
- INHIBIT BLANKING TIME: 700 ns
- AUTOMATIC TURN OFF FOR DUTY-CYCLE LESS THAN 14%
- POSSIBILITY TO OPERATE IN DISCONTINUOUS MODE

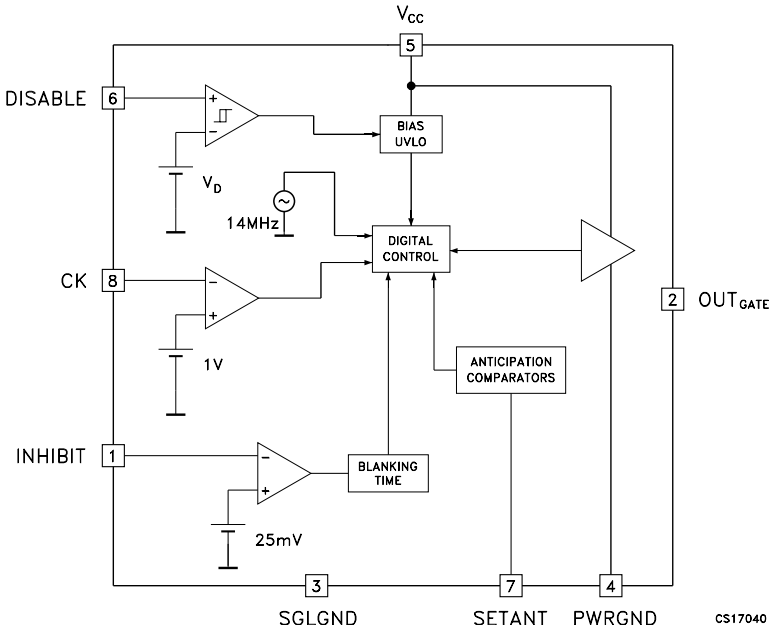
SO-8

DESCRIPTION

STSR30 Smart Driver IC provides a high current outputs to properly drive secondary Power Mosfets used as Synchronous Rectifier in low output voltage, high efficiency Flyback Converters. From a synchronizing clock input, withdrawn on the secondary side of the isolation transformer, the IC generates a driving signal with set dead times with respect to the primary side PWM signal.

The IC operation prevents secondary side shoot-through conditions at turn-on of the primary switch providing anticipation in turn-off the output. This smart function is implemented by a fast cycle-after-cycle logic control mechanism, based on a high frequency oscillator synchronized by the clock signal. This anticipation is externally set through external component. A special Inhibit function, detecting the voltage across the Synchronous FET, allows to shut-off the drive output during discontinuous mode condition. A Disable pin allows turning off the device during no-load condition reducing overall current consumption.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	DC Input Voltage to SGLGND	-0.3 to 6	V
OUT_{GATE}	Max Gate Drive Output Voltage	-0.3 to V_{CC}	V
DISABLE	Max DISABLE Voltage	-0.3 to V_{CC}	V
INHIBIT	Max INHIBIT Voltage (*)	-0.6 to V_{CC}	V
CK	Clock Input Voltage Range (*)	-0.3 to V_{CC}	V
ESD	Human Body Model	±2	KV
P_{TOT}	Continuous Power Dissipation at T_A=105°C SO-8 (No heatsink)	275	mW
T_{STG}	Storage Temperature Range	-40 to +150	°C
T_{OP}	Operating Junction Temperature Range	-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) A higher positive voltage level can be applied to the pin with a resistor which limits the current flowing into the pin to 10mA maximum

THERMAL DATA

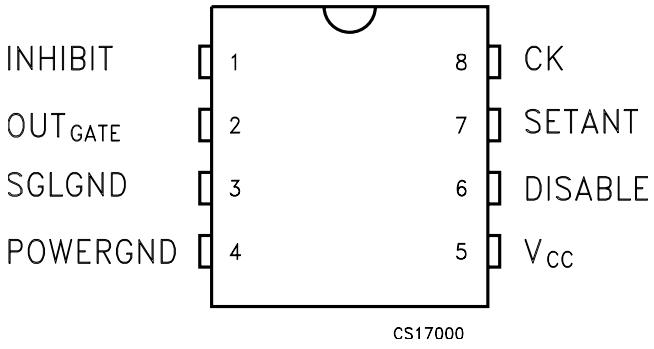
Symbol	Parameter	SO-8	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	40	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (*)	160 (*)	°C/W

(*) This value is referred to one layer pcb board with minimum copper connections for the leads. A minimum value of 120 °C/W can be obtained improving thermal conductivity of the board

ORDERING CODES

TYPE	SO-8	SO-8 (T&R)
STSR30	STSR30D	STSR30D-TR

CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

Pin N°	Symbol	Name and Function
1	INHIBIT	This input enables OUT_{GATE} to work when its voltage is lower than the negative threshold voltage ($V_{INHIBIT}<V_H$). If $V_{INHIBIT}>V_H$ the OUT_{GATE} will be high for a minimum conduction time ($t_{ON(GATE)}$). In typical flyback converter application, it is possible to turn off the synchronous MOSFET when the current through it tends to reverse, allowing discontinuous conduction mode and providing protection to the converter from eventual sinking current from the load. A blanking time of 700ns allows operation when some voltage ringing is present during turn-off of primary switch. Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
2	OUT_{GATE}	Gate Drive signal for Synchronous MOSFET. Anticipation [t_{ANT}] in turning off OUT_{GATE} is provided when the clock input goes to low level.
3	SGLGND	Reference for all the control logic signals. This pin is completely separated from the PWRGND to prevent eventual disturbances to affect the control logic.
4	PWRGND	Reference for power signals, this pin carries the full peak currents for the output.
5	V_{CC}	The supply voltage range from 4.5V to 5.5V allows applications with logic gate threshold mosfets. UVLO feature guarantees proper start-up while it avoids undesirable driving during eventual dropping of the supply voltage.
6	DISABLE	This pin allows turning off the device completely when kept to low level. In this condition the IC power consumption is strongly reduced. When this pin goes to high value, OUT_{GATE} turns to switching again according to the CK signal.
7	SETANT	The voltage on this pin sets the anticipation in turning off the OUTGATE. It is possible to choose among three different anticipation times by discrete partitioning of the supply voltage [ANT].
8	CK	This input provides synchronization for IC's operations, being the transitions between the two output conditions based on a positive threshold, equal for the two slopes. A smart internal control logic mechanism using a 15MHz internal oscillator generates proper anticipation timing at the turn-off of each output. This feature allows safe turn-off of Synchronous Rectifiers avoiding any eventual shoot-through situation on secondary side at both transitions. Clock revelation mechanism makes the operation of STSR30 particularly suitable for flyback adaptors application allowing correct operation during discontinuous mode. Absolute maximum positive voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, CK = 100kHz, duty-cycle = 50%, $V_{INHIBIT}$ = -200mV, T_J = -40 to 125°C, C_1 = C_2 = 100nF ceramic, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT AND UNDER VOLTAGE LOCK OUT						
V_{CC}	Start Threshold			3.7	4	V
	Turn OFF Threshold After Start		3.3	3.6		
I_{CC}	Unloaded Supply Current	OUT_{GATE} = no load		3.2	4.5	mA
		DISABLE = 0V		15	50	µA
GATE DRIVER OUTPUT						
OUT_{GATE}	Output Low Voltage	$I_{OUTGATE}$ = -200mA		0.20	0.45	V
	Output High Voltage	$I_{OUTGATE}$ = 200mA	4.30	4.65		
I_{OUT}	Output Source Peak Current	T_J = 25°C		1.5		A
	Output Sink Peak Current	T_J = 25°C		1.5		
$R_{DS(ON)}$	Output Series Source Resistance			1.75	3.5	Ω
	Output Series Sink Resistance			1	2.25	
t_R	Rise Time	C_{LOAD} = 5nF (Note 1)		40		ns
t_F	Fall Time	C_{LOAD} = 5nF (Note 1)		40		ns
t_P	Clock Propagation Delay to Turn ON of OUT_{GATE}	No Load (Fig. 4)		25		ns
TURN-OFF ANTICIPATION TIME						
t_{ANT}	OUT_{GATE} Turn-off Anticipation Time (Fig. 1)	V_{ANT} = 0 to 1/3V_{CC}; no load		150		ns
		V_{ANT} = 1/3V_{CC} to 2/3V_{CC}; no load		225		
		V_{ANT} = 2/3V_{CC} to V_{CC}; no load		300		
I_{SETANT}	Leakage Current (Note 2)		-0.1		0.1	µA
DISABLE						
V_{DP}	Positive Threshold Voltage	$V_{DISABLE}$ > V_{DP} : ON		1.7	2.4	V
V_{DN}	Negative Threshold Voltage	$V_{DISABLE}$ < V_{DN} : OFF	0.8	1.5		V
V_{HY}	Hysteresis Voltage			0.2		V
I_I	Input Current		-0.1		0.1	µA
INHIBIT (OUT_{GATE} ENABLE)						
V_H	Threshold Voltage	T_J = 25°C	-30	-25		mV
I_H	Leakage Current	$V_{INHIBIT}$ = +200mV		-100		nA
		$V_{INHIBIT}$ = -200mV			1.5	µA
t_{BL}	Blanking Time	$V_{INHIBIT}$ = +200mV		700		ns
SYNCHRONIZATION INPUT						
V_{CK}	Rise Threshold Voltage			1	1.2	V
	Fall Threshold Voltage		0.6	0.8		
D_{OFF}	Duty Cycle Shut Down		12	14		%
	Duty Cycle Turn ON after Shut Down			19	20	

Note1: t_R is measured between 10% and 90% of the final voltage; t_F is measured between 90% and 10% on the initial voltage
Note2: Parameter guaranteed by design

Figure 1 : TIMING DIAGRAM

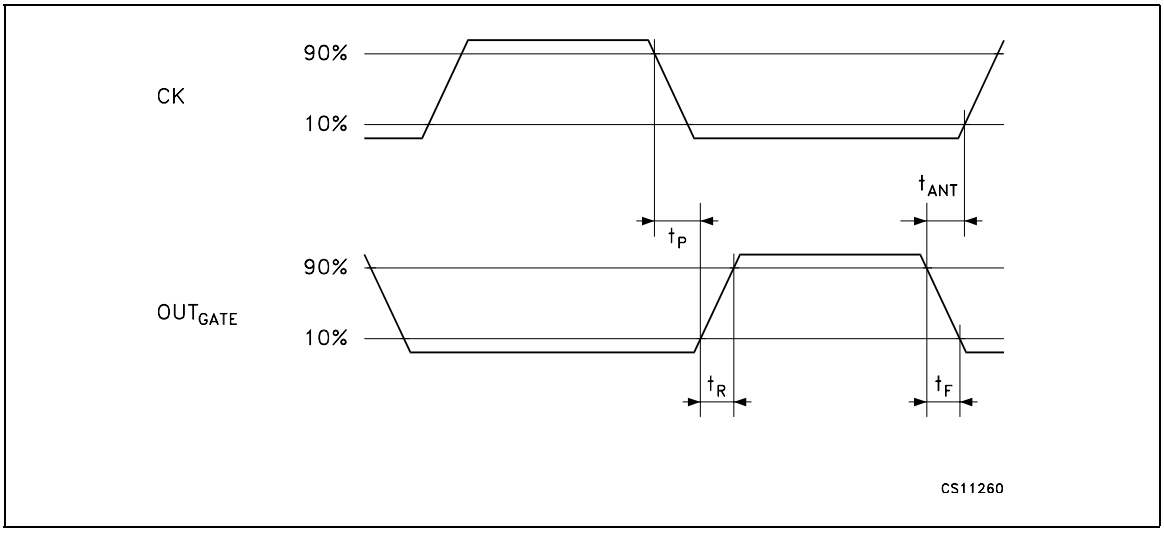
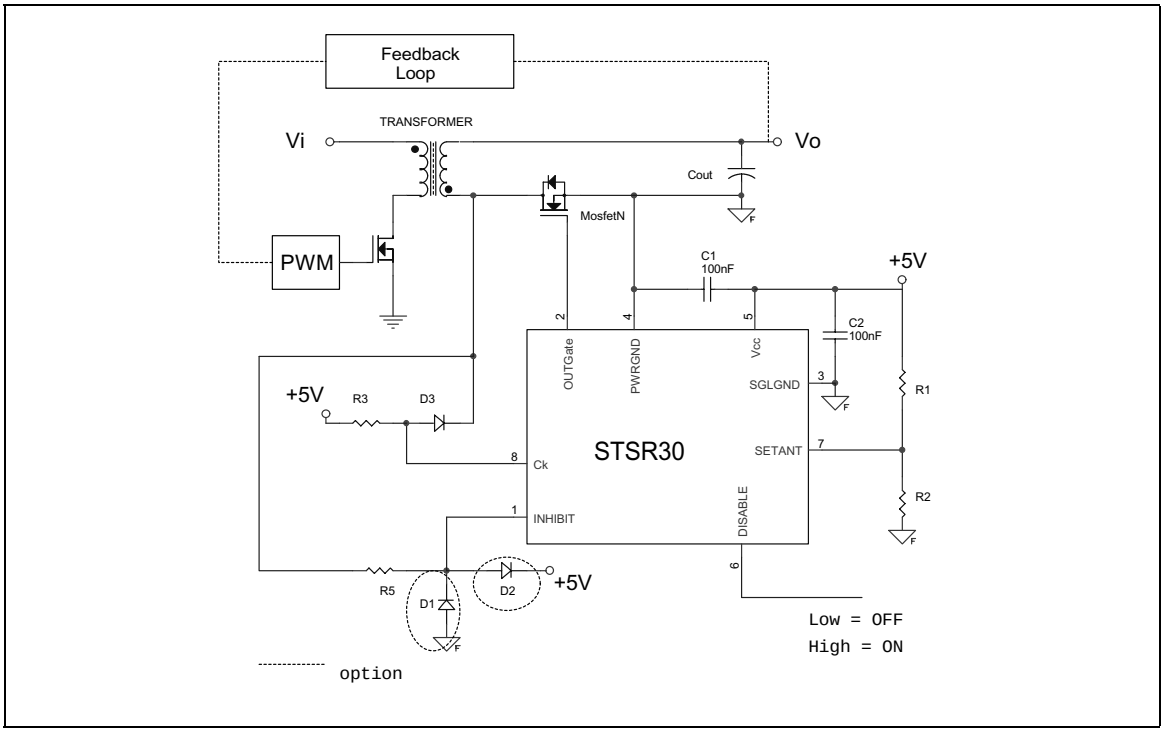
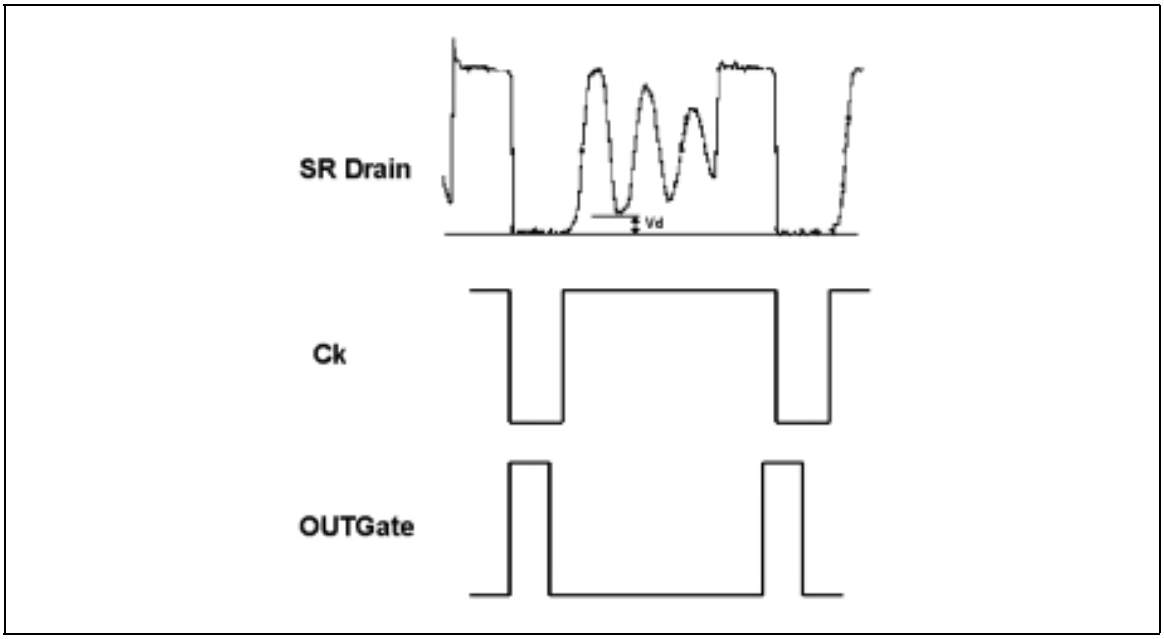


Figure 2 : STSR30 IN FLYBACK CONVERTER SECONDARY SIDE



NOTES
1) Ceramic Capacitors C1 and C2 must be placed very close to the IC;
2) R1 and R2 set the anticipation time by partitioning the V_{CC} voltage;
3) R3 is a pull-up resistor;
4) R5 limits the current flowing through diode D2 when Freewheeling drain voltage is high;
5) D1 could be necessary to protect INHIBIT pin from negative voltages.
6) D2 could be necessary to protect INHIBIT pin from voltages higher than V_{CC}
7) SGLGND layout trace must not include OUTGATE current paths.

Figure 3 : STSR30 SYNCHRONIZATION TECHNIQUE



The synchronization is based on the revelation of the low level of the drain voltage of the synchronous rectifier. To avoid false triggering of the device during discontinuous mode, it is important that the lowest level of the ringing must be higher than the Ck threshold. Diode D3 and resistor R3 keep the Ck signal to high level even during the ringing. OUTGate is the complementary signal of the Ck with proper dead time setting to avoid cross-conduction.

Figure 4 : INHIBIT OPERATION OF OUT_{GATE} IN DISCONTINUOUS CONDUCTION MODE

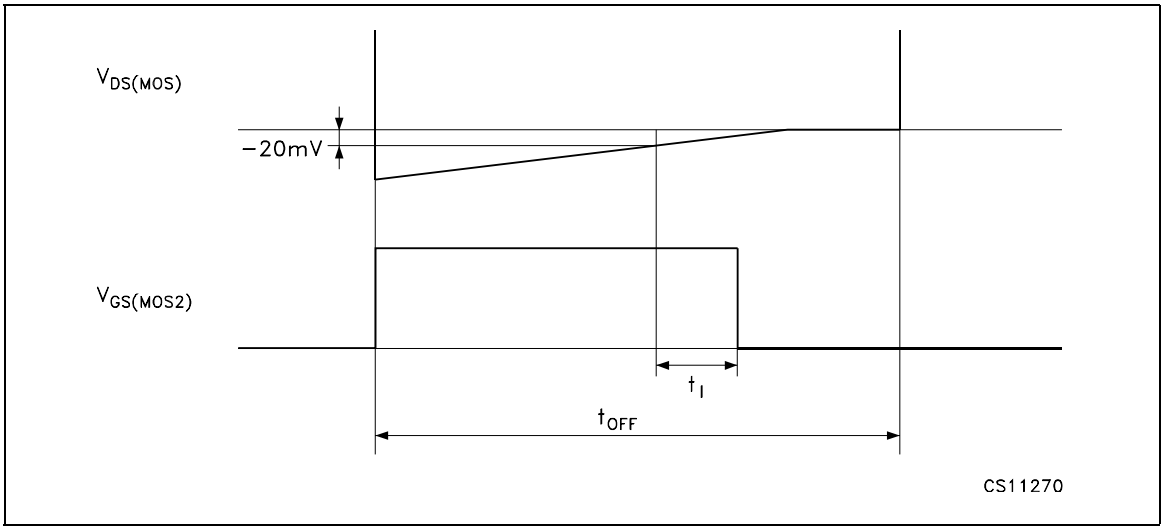


Figure 5 : INHIBIT Threshold Voltage vs Temperature

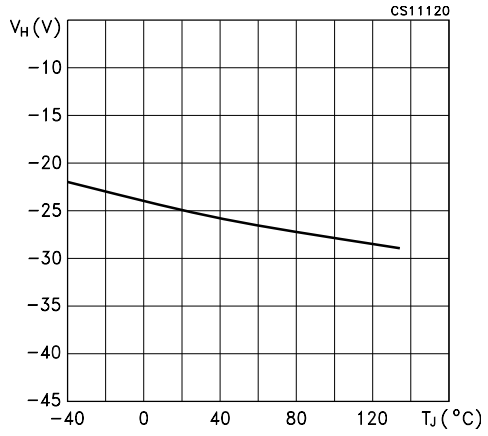


Figure 6 : I_{CC} vs CK Frequency

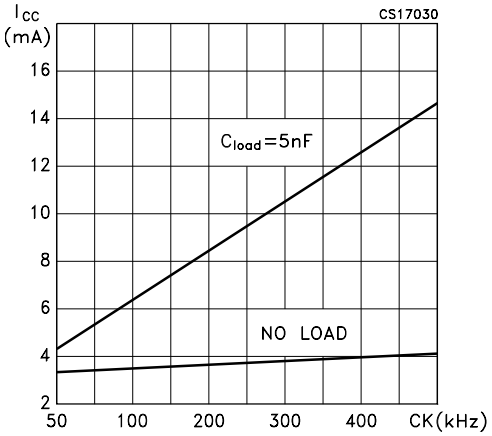


Figure 7 : Rise and Fall Time vs Load Capacitor

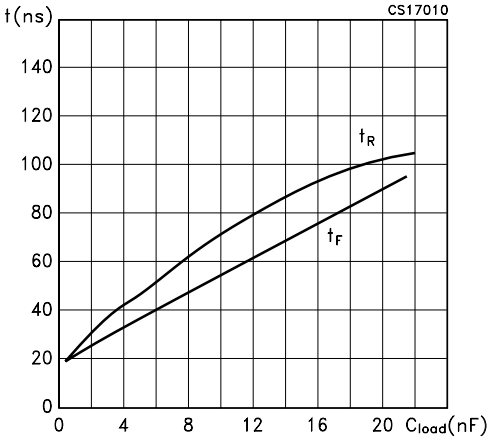


Figure 8 : $R_{DS(ON)}$ vs Temperature

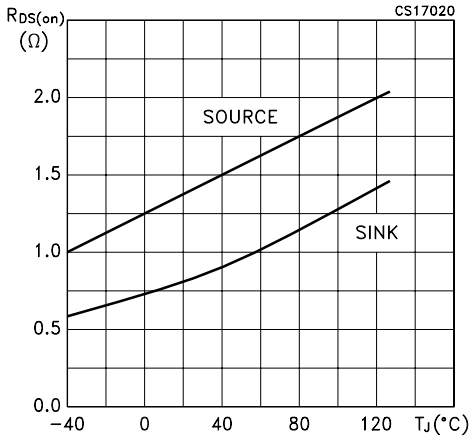


Figure 9 : Minimum $T_{ON(GATE)}$

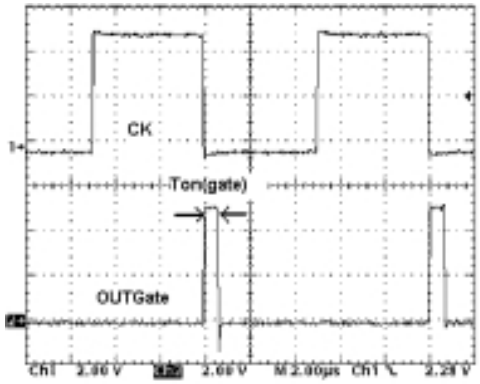
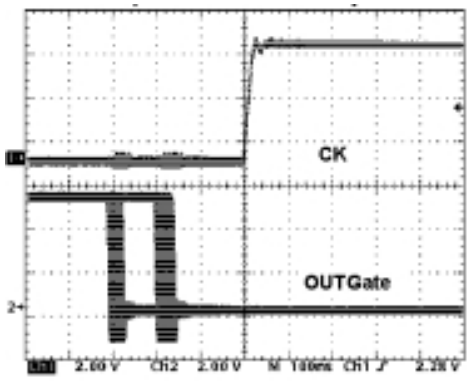
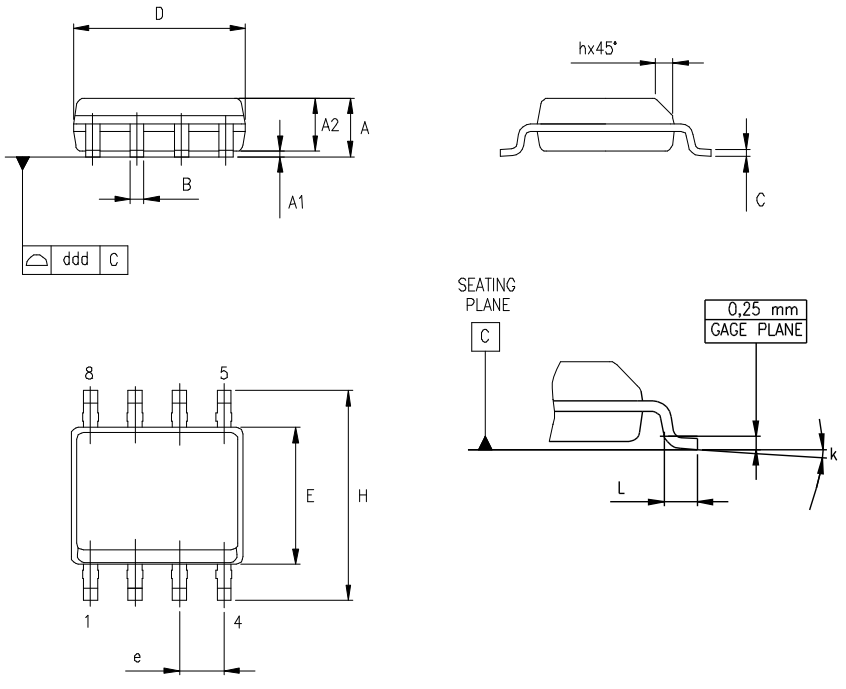


Figure 10 : OUT_{GATE} Turn-off Jitter with Minimum Anticipation Time



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



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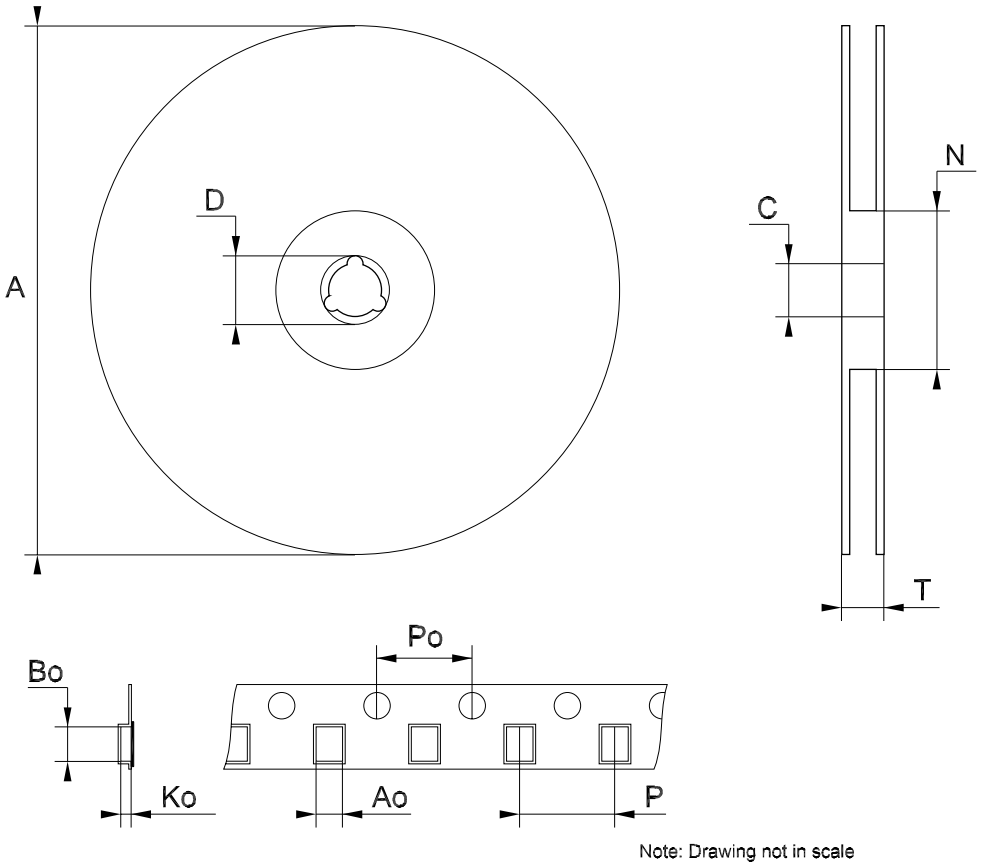
Tape & Reel SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale