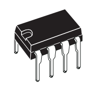
LM2904W

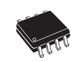
Low power dual operational amplifier

Features

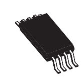
- Internally frequency compensated
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current/op (500 µA)
- Low input bias current: 20 nA (temperature compensated)
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rail
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to (V_{CC}^{+} - 1.5 V)
- ESD internal protection: 2 kV



N
DIP8
(Plastic package)

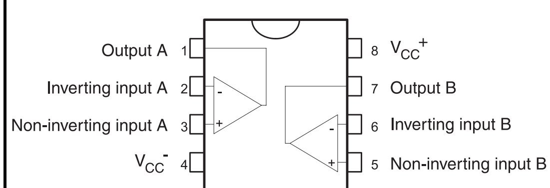


D
SO-8
(Plastic micropackage)



P
TSSOP8
(Thin shrink small outline package)

Pin connections (top view)



Description

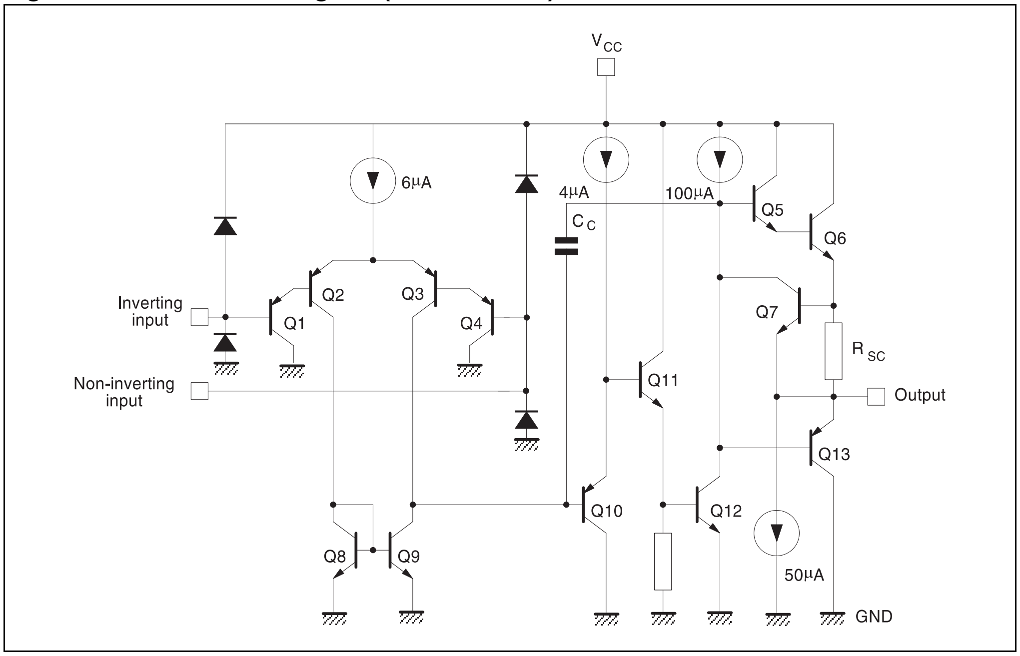
This circuit consists of two independent, high gain, internally frequency compensated operational amplifiers, designed specifically for automotive and industrial control system. It operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied from standard +5 V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from a single power supply.

1 Schematic diagram

Figure 1. Schematic diagram (1/2 LM2904W)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	+32	V
V_{id}	Differential input voltage(2)	-0.3V to V_{CC} + 0.3	V
V_{in}	Input voltage	-0.3V to V_{CC} + 0.3	V
	Output short-circuit duration(3)	Infinite	s
I_{in}	Input current (4)	50	mA
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient(5) SO-8 TSSOP8 DIP8	 125 120 85	°C/W
R_{thjc}	Thermal resistance junction to case(5) SO-8 TSSOP8 DIP8	 40 37 41	°C/W
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	HBM: human body model(6) MM: machine model(7) CDM: charged device model(8)	2000 200 1500	V

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC}^+ > 15$ V. The maximum output current is approximately 40 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
4. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
5. Short-circuits can cause excessive heating and destructive dissipation. R_{th} are typical values.
6. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common mode input voltage range $T_{min} \leq T_{amb} \leq T_{max}$	V_{CC}^{+} - 1.5 V_{CC}^{+} - 2	V
T_{oper}	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. V_{CC}^+ = 5V, V_{CC}^- = Ground, V_O = 1.4V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) $T_{min} \leq T_{amb} \leq T_{max}$		2	7 9	mV
DV_{io}	Input offset voltage drift		7	30	µV/°C
I_{io}	Input offset current $T_{min} \leq T_{amb} \leq T_{max}$		2	30 40	nA
DI_{io}	Input offset current drift		10	300	pA/°C
I_{ib}	Input bias current (2) $T_{min} \leq T_{amb} \leq T_{max}$		20	150 200	nA
A_{vd}	Large signal voltage gain V_{CC}^+= +15V, R_L=2kΩ, V_o=1.4V to 11.4V $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio $R_S \leq$10kΩ $T_{min} \leq T_{amb} \leq T_{max}$	65 65	100		dB
I_{CC}	Supply current, all Amp, no load V_{CC} = +5V $T_{min} \leq T_{amb} \leq T_{max}$, V_{CC} = +30V		0.7	1.2 2	mA
CMR	Common-mode rejection ratio R_S = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$	70 60	85		dB
I_{source}	Output short-circuit current V_{CC}^+ = +15V, V_o = +2V, V_{id} = +1V	20	40	60	mA
I_{sink}	Output sink current V_O = 2V, V_{CC}^+ = +5V V_O = +0.2V, V_{CC}^+ = +15V	10 12	20 50		mA µA
V_{OH}	High level output voltage V_{CC}^+ = + 30V R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$	26 26 27 27	27 28		V
V_{OL}	Low level output voltage R_L = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew rate V_{CC}^+ = 15V, V_{in} = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain $T_{min} \leq T_{amb} \leq T_{max}$	0.3 0.2	0.6		V/µs

Table 3. $V_{CC}^+ = 5V$, $V_{CC}^- =$ Ground, $V_O = 1.4V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product $f = 100kHz$, $V_{CC}^+ = 30V$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$	0.7	1.1		MHz
THD	Total harmonic distortion $f = 1kHz$, $A_V = 20dB$, $R_L = 2k\Omega$, $V_o = 2V_{pp}$, $C_L = 100pF$, $V_{CC}^+ = 30V$		0.02		%
e_n	Equivalent input noise voltage $f = 1kHz$, $R_S = 100\Omega$, $V_{CC}^+ = 30V$		55		nV/√Hz
V_{O1}/V_{O2}	Channel separation (3) $1kHz \leq f \leq 20kHz$		120		dB

1. $V_O = 1.4$ V, $R_S = 0\ \Omega$, 5 V < V_{CC}^+ < 30 V, 0 V < V_{ic} < V_{CC}^+ - 1.5 V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.
3. Due to the proximity of external components, ensure that stray capacitance does not cause coupling between these external parts. Typically, this can be detected because this type of capacitance increases at higher frequencies.

Figure 2. Open loop frequency response

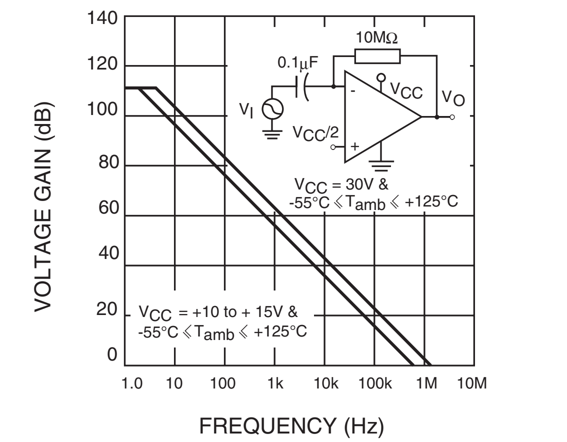


Figure 3. Large signal frequency response

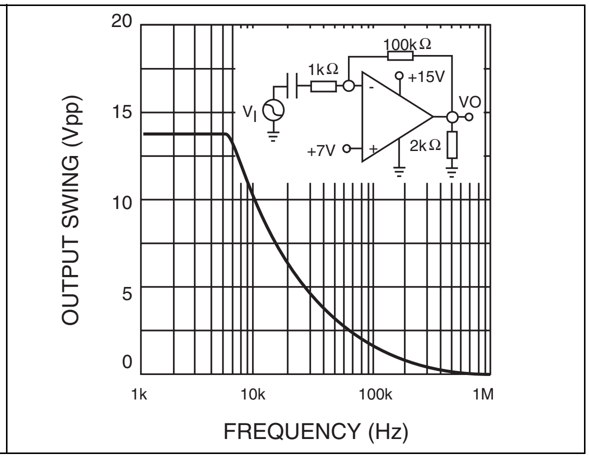


Figure 4. Voltage follower pulse response

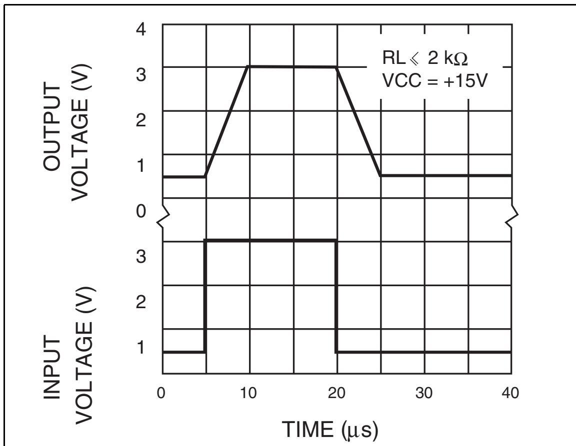


Figure 5. Output characteristics

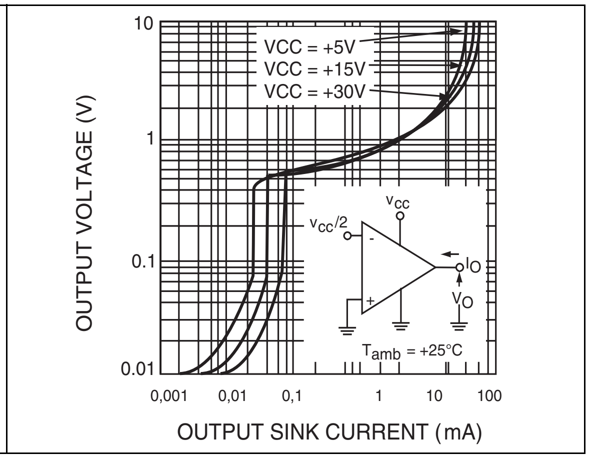


Figure 6. Voltage follower pulse response

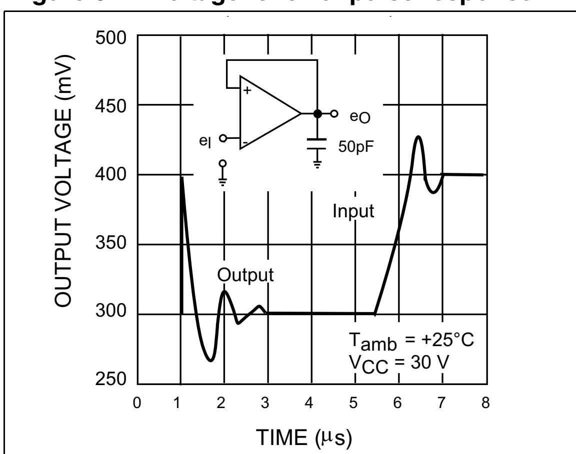


Figure 7. Output characteristics

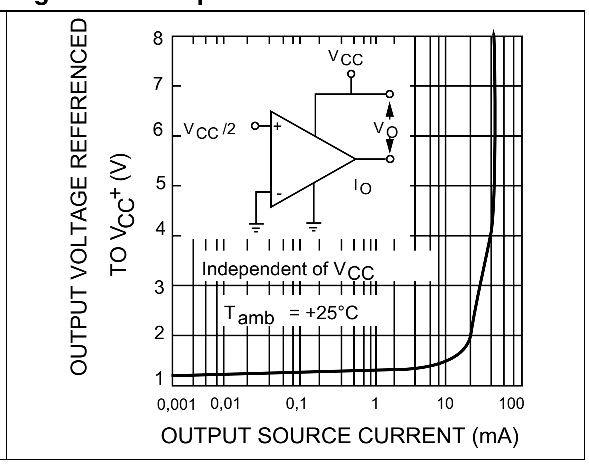


Figure 8. Input current versus temperature

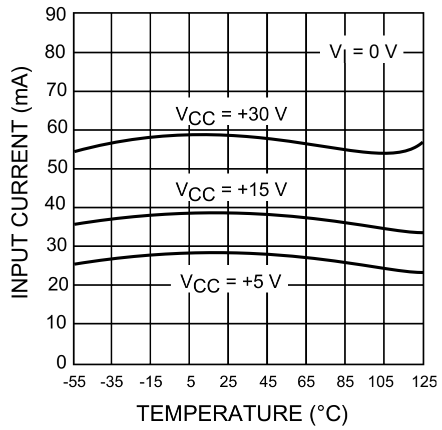


Figure 9. Current limiting

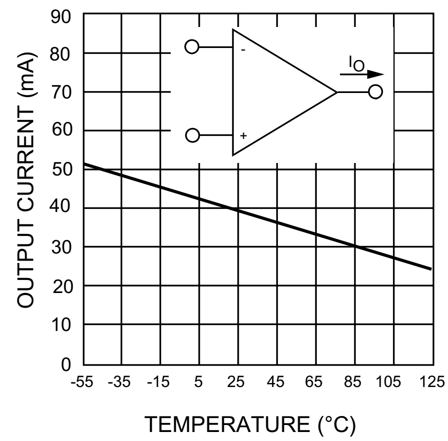


Figure 10. Input voltage range

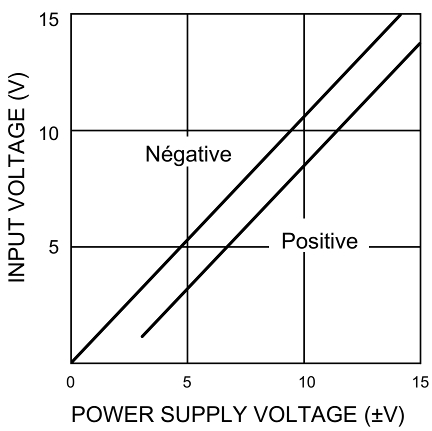


Figure 11. Supply current

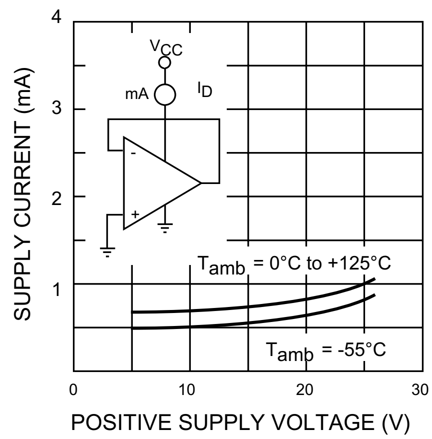


Figure 12. Voltage gain

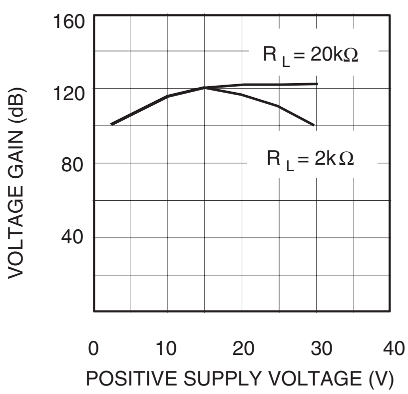


Figure 13. Input current versus supply voltage

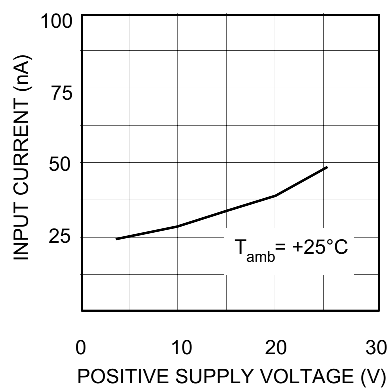


Figure 14. Gain bandwidth product

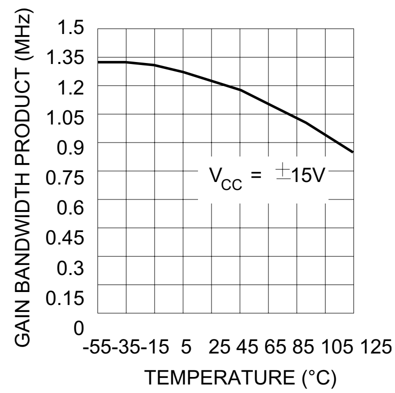


Figure 15. Power supply rejection ratio

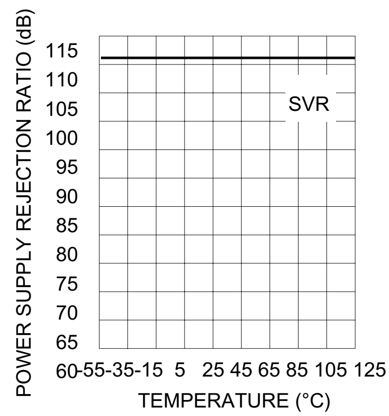


Figure 16. Common mode rejection ratio

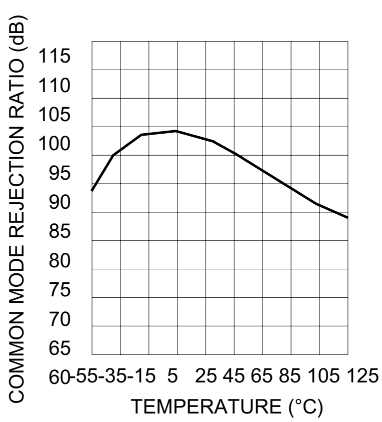
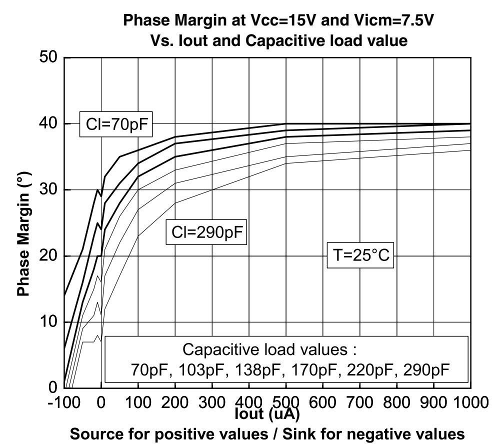


Figure 17. Phase margin vs capacitive load



Typical single-supply applications

Figure 18. AC coupled inverting amplifier

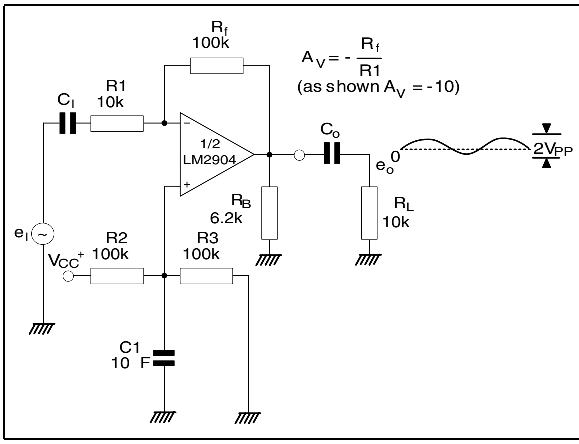


Figure 19. AC coupled non-inverting amplifier

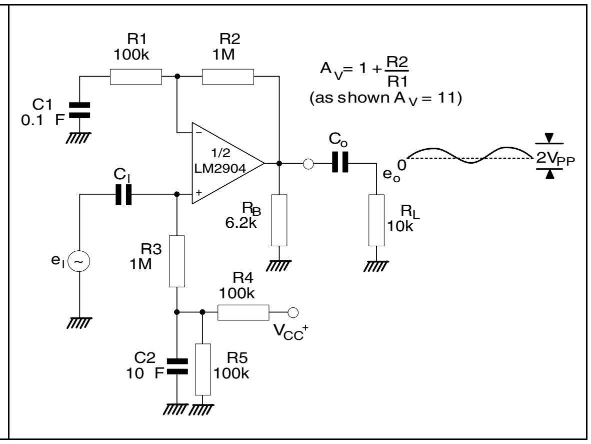


Figure 20. Non-inverting DC gain

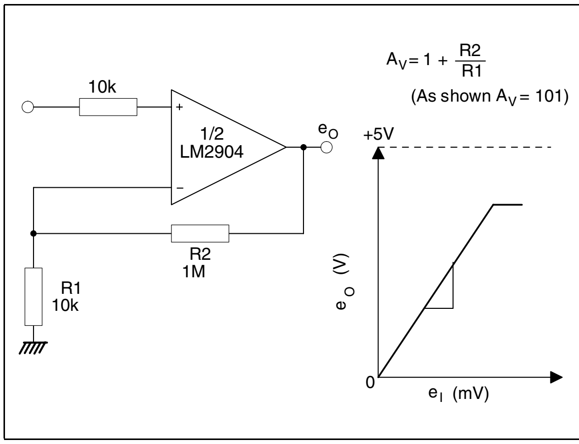


Figure 21. DC summing amplifier

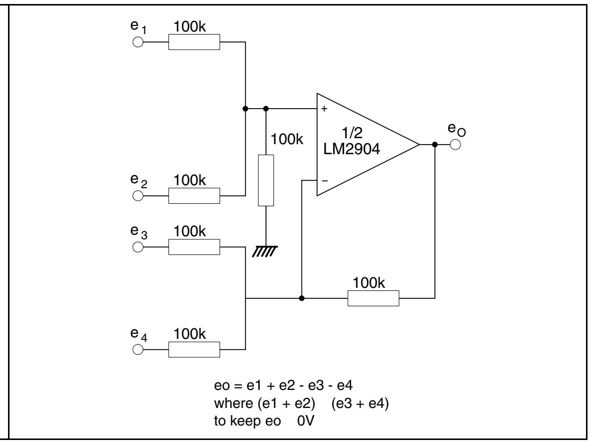


Figure 22. High input Z, DC differential amplifier

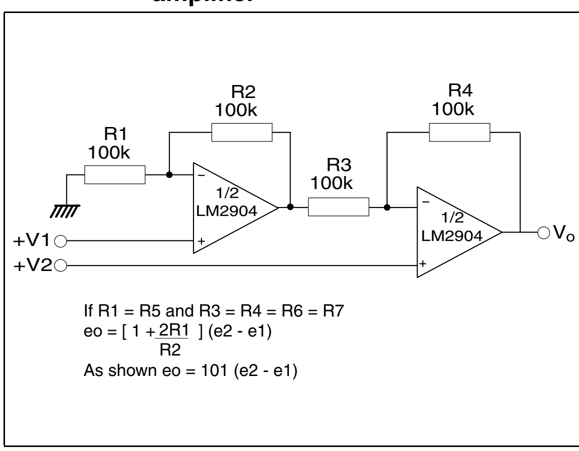


Figure 23. Using symmetrical amplifiers to reduce input current

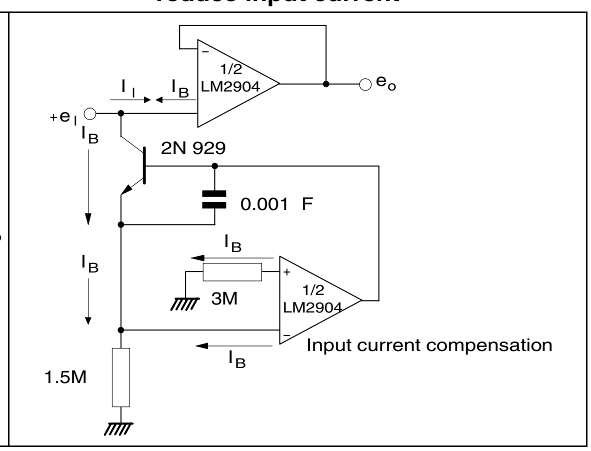


Figure 24. Low drift peak detector

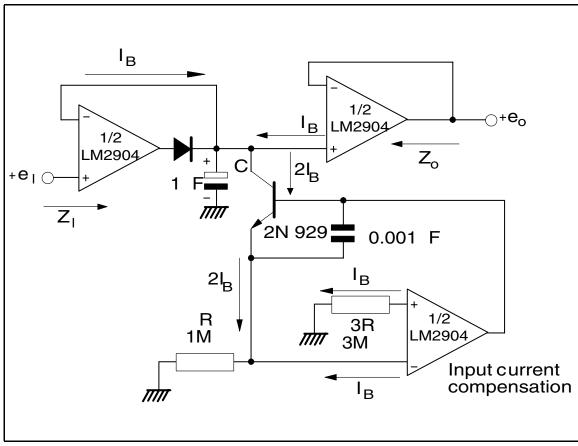
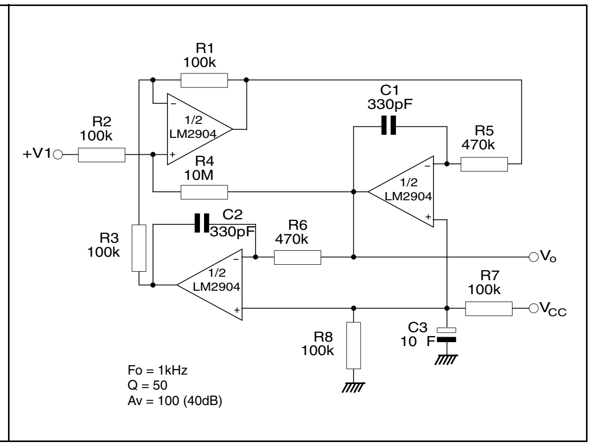


Figure 25. Active bandpass filter



4 Macromodel

4.1 Important note concerning this macromodel

Please consider the following remarks before using this macromodel.

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (temperature, supply voltage, for example). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.

Data derived from macromodels used outside of the specified conditions (V_{CC}, temperature, for example) or even worse, outside of the device operating conditions (V_{CC}, V_{icm}, for example), is not reliable in any way.

4.2 Macromodel code

```
** Standard Linear Ics Macromodels, 1993.
** ESD diodes added to the initial macromodel (2007).
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT LM2904W 1 2 3 4 5
***************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
D1A 1 4 MDTH 400E-12
D1B 5 1 MDTH 400E-12
D2A 2 4 MDTH 400E-12
D2B 5 2 MDTH 400E-12
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
```

```
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 SO-8 package information

Figure 26. SO-8 package mechanical drawing

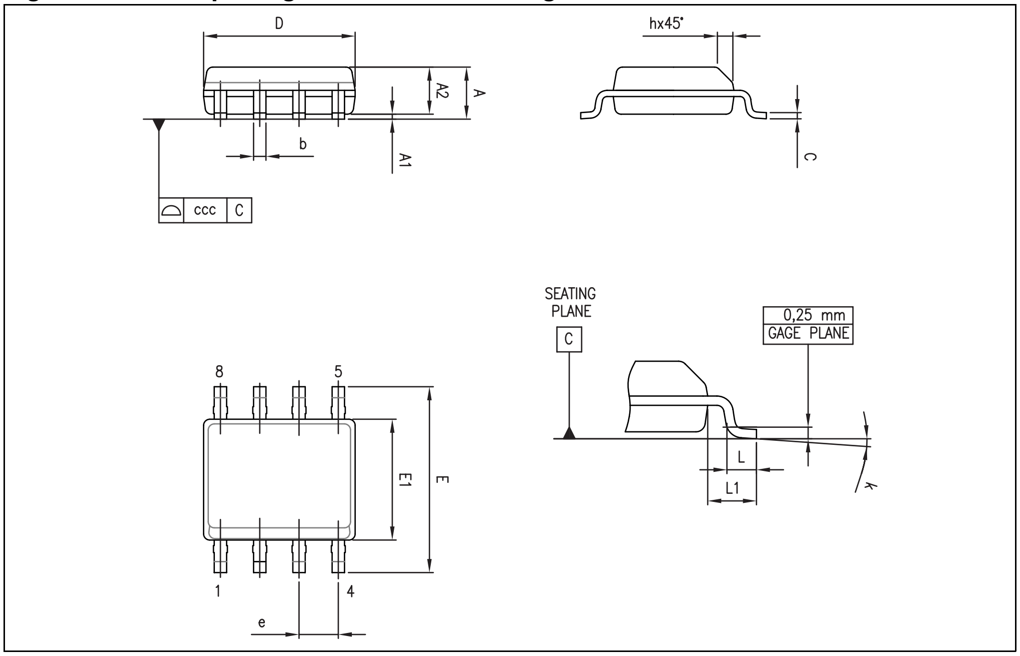


Table 4. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

5.2 DIP8 package information

Figure 27. DIP8 package mechanical drawing

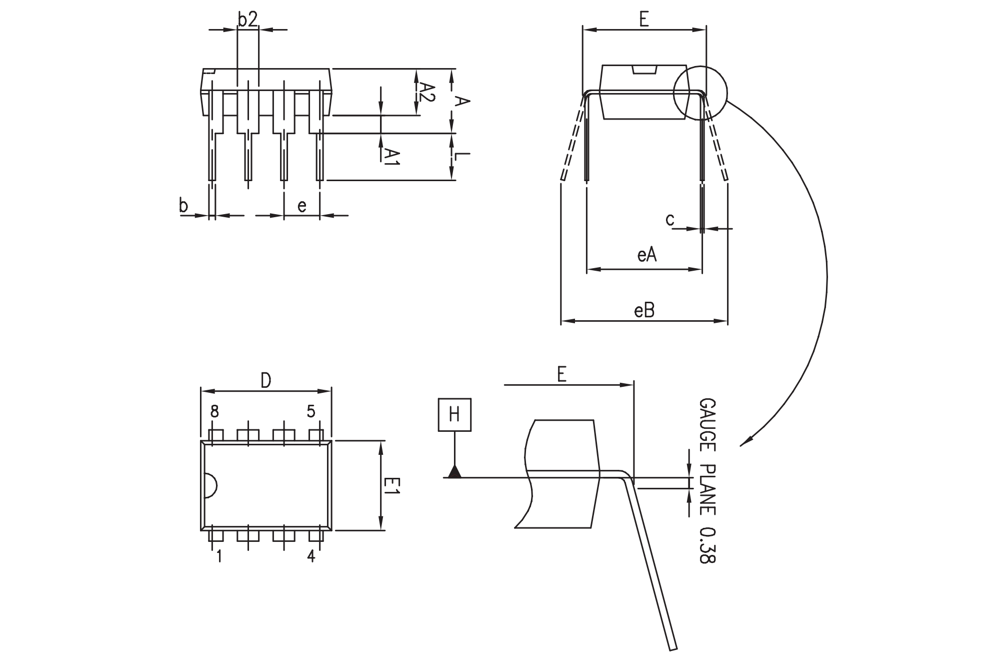


Table 5. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

5.3 TSSOP8 package information

Figure 28. TSSOP8 package mechanical drawing

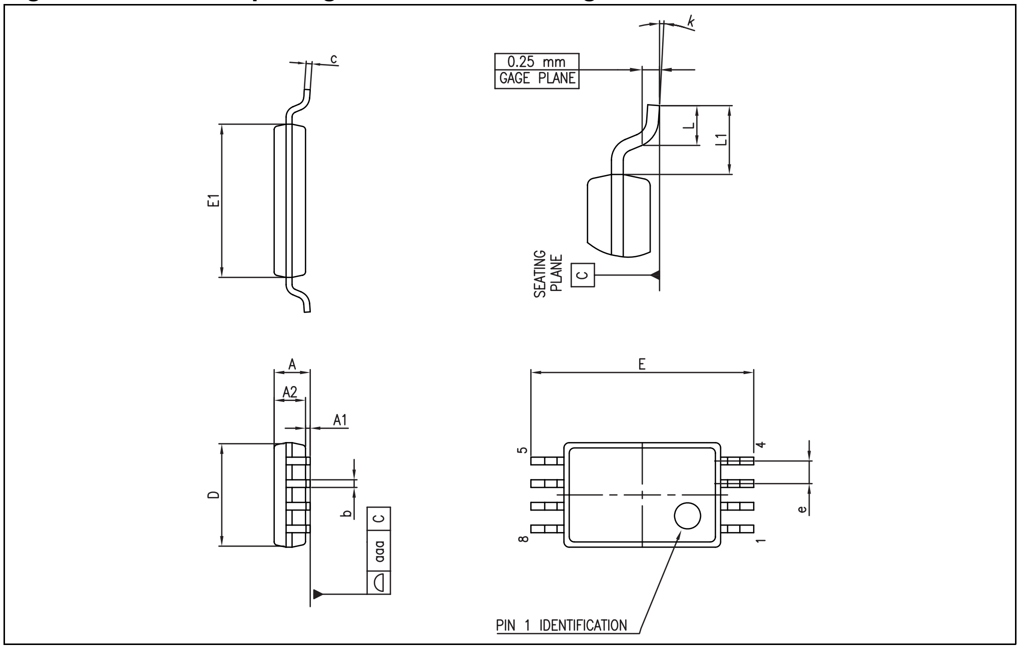


Table 6. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

6 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Packing	Marking
LM2904WN	-40°C, +125°C	DIP8	Tube	LM2904W
LM2904WD LM2904WDT		SO-8	Tube or tape & reel	2904W
LM2904WPT		TSSOP8	Tape & reel	2904W
LM2904WYD(1) LM2904WYDT(1)		SO-8 (Automotive grade level)	Tube or tape & reel	2904WY
LM2904WYPT(2)		TSSOP8 (Automotive grade level)	Tape & reel	K04WY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.
2. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
1-Sep-2003	1	Initial release.
1-Jul-2005	2	PPAP references inserted in the datasheet see *Section 6: Ordering information on page 18*. ESD protection inserted in *Table 1: Absolute maximum ratings (AMR) on page 3*.
1-Oct-2005	3	Correction of error in AVD min. value see *Table 3 on page 5*.
1-Dec-2005	4	LM2904WYPT PPAP reference added in *Section 6: Ordering information on page 18*. Information added in *Table 1: Absolute maximum ratings (AMR) on page 3*.
2-May-2006	5	Minimum value of slew rate at 25°C and in temperature added in *Table 3 on page 5*.
20-Jul-2007	6	Power dissipation value corrected in *Table 1: Absolute maximum ratings (AMR)*. ESD tolerance for HBM model improved to 2kV in *Table 3 on page 5*. Equivalent input noise voltage parameter added in *Table 3*. Electrical characteristics curves updated. Added *Figure 17: Phase margin vs capacitive load on page 9*. *Section 5: Package information* updated. *Section 4: Macromodel* added.
18-Dec-2007	7	Reformatted electrical characteristics table, *Table 3*. Deleted V_{opp} parameter in *Table 3*. Corrected footnotes for automotive grade order codes in *Table 7*.
21-Feb-2008	8	Corrected SO-8 package mechanical data. Dimension E in drawing was marked H in table. Corrected revision history.
24-Feb-2011	9	Corrected x-axis in *Figure 5*.

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