

## Precision quad operational amplifier

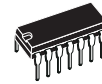
### Features

- Low input offset voltage: 500  $\mu$ V max.
- Low power consumption.
- Short circuit protection.
- Low distortion, low noise.
- High gain-bandwidth product.
- High channel separation.
- ESD protection 2 kV.
- Macromodel included in this specification.

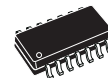
### Description

The TS514 is a high-performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as a voltage follower in spite of its high gain bandwidth.

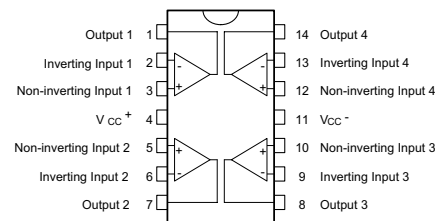
The circuit presents very stable electrical characteristics over the entire supply voltage range, and is particularly intended for professional and telecom applications (such as active filters, for example).



**N**  
**DIP14**  
(Plastic package)



**D**  
**SO-14**  
(Plastic micropackage)



**Pin connections**  
(Top view)

# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	$\pm 18$	V
$V_i$	Input voltage	$V_{DD}-0.2$ to $V_{CC}+0.2$	V
$V_{id}^{(1)}$	Differential input voltage	$\pm V_{CC}$	V
$T_{stg}$	Storage temperature range	-65 to +150	$^{\circ}\text{C}$
$R_{thja}$	Thermal resistance junction to ambient		$^{\circ}\text{C}/\text{W}$
	SO-14 DIP14	103 80	
$R_{thjc}$	Thermal resistance junction to case		$^{\circ}\text{C}/\text{W}$
	SO-14 DIP14	31 33	
ESD	HBM: human body model <sup>(2)</sup>	2	kV
	MM: machine model <sup>(3)</sup>	200	V
	CDM: charged device model <sup>(4)</sup>	1.5	kV

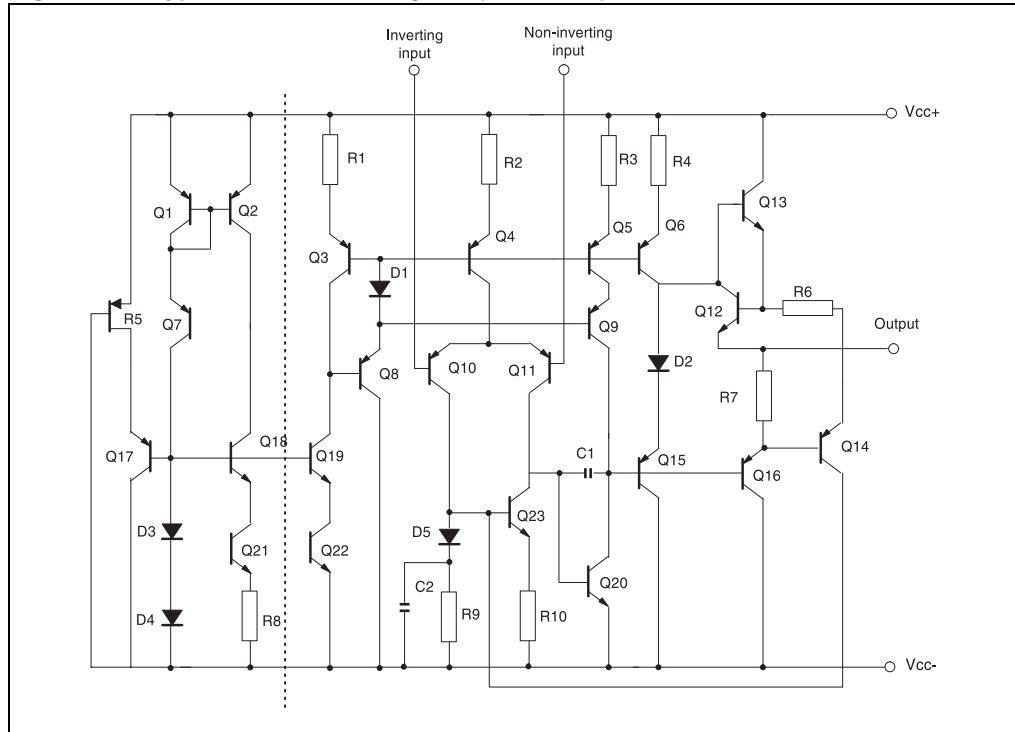
1. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5k $\Omega$  resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5  $\Omega$ ). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	6 to 30	V
$V_{icm}$	Common mode input voltage range	$V_{DD} + 0.8$ to $V_{CC} - 1.5$	V
$T_{oper}$	Operating free air temperature range	-40 to +125	$^{\circ}\text{C}$

## 2 Schematic diagram

Figure 1. Typical schematic diagram (1/4 TS514)



### 3 Electrical characteristics

**Table 3.**  $V_{CC} = \pm 15\text{ V}$ ,  $T_{amb} = 25^\circ\text{ C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current (per operator) at $T_{min} \leq T_{op} \leq T_{max}$		0.5	0.6 0.75	mA
$I_{ib}$	Input bias current – at $25^\circ\text{ C}$ – at $T_{min} \leq T_{op} \leq T_{max}$		50	150 300	nA
$R_i$	Input resistance, $F = 1\text{ kHz}$		1		$M\Omega$
$V_{io}$	Input offset voltage – at $25^\circ\text{ C}$ : TS514 TS514A – at $T_{min} \leq T_{op} \leq T_{max}$ TS514 TS514A		0.5	2.5 0.5  4 1.5	mV
$\Delta V_{io}$	Input offset voltage drift at $T_{min} \leq T_{op} \leq T_{max}$		5		$\mu\text{V}/^\circ\text{C}$
$I_{io}$	Input offset current at $25^\circ\text{ C}$ at $T_{min} \leq T_{op} \leq T_{max}$		5	20 40	nA
$\Delta I_{io}$	Input offset current drift $T_{min} \leq T_{op} \leq T_{max}$		0.08		$\frac{\text{nA}}{^\circ\text{C}}$
$I_{os}$	Output short circuit current		23		mA
$A_{vd}$	Large signal voltage gain, $R_L = 2\text{ k}\Omega$ $V_{CC} = \pm 15\text{ V}$ , at $T_{min} \leq T_{op} \leq T_{max}$ $V_{CC} = \pm 4\text{ V}$	90	100 95		dB
GBP	Gain bandwidth product, $F = 100\text{ kHz}$	1.8	3		MHz
$e_n$	Equivalent input noise voltage, $F = 1\text{ kHz}$ $R_s = 50\ \Omega$ $R_s = 1\text{ k}\Omega$ $R_s = 10\text{ k}\Omega$		8 10 18	15	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
THD	Total harmonic distortion $A_v = 20\text{ dB}$ , $R_L = 2\text{ k}\Omega$ , $V_o = 2\text{ V}_{pp}$ , $f = 1\text{ kHz}$		0.03	0.1	%
$\pm V_{opp}$	Output voltage swing, $R_L = 2\text{ k}\Omega$ $V_{CC} = \pm 15\text{ V}$ , at $T_{min} \leq T_{op} \leq T_{max}$ $V_{CC} = \pm 4\text{ V}$	$\pm 13$	$\pm 3$		V
$V_{opp}$	Large signal voltage swing, $R_L = 10\text{ k}\Omega$ , $F = 10\text{ kHz}$		28		$V_{pp}$
SR	Slew rate, unity gain, $R_L = 2\text{ k}\Omega$	0.8	1.5		$\text{V}/\mu\text{s}$
CMR	Common mode rejection ratio, $V_{ic} = 10\text{ V}$	90			dB

**Table 3.**  $V_{CC} = \pm 15\text{ V}$ ,  $T_{amb} = 25^\circ\text{ C}$  (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection ratio, $dV_{ic} = 10\text{ V}$ , $F = 100\text{ Hz}$	90			dB
$V_{o1}/V_{o2}$	Channel separation, $F = 1\text{ kHz}$		120		dB

Figure 2.  $V_{io}$  distribution at  $V_{cc} = \pm 15$  V and  $T = 25^\circ\text{C}$

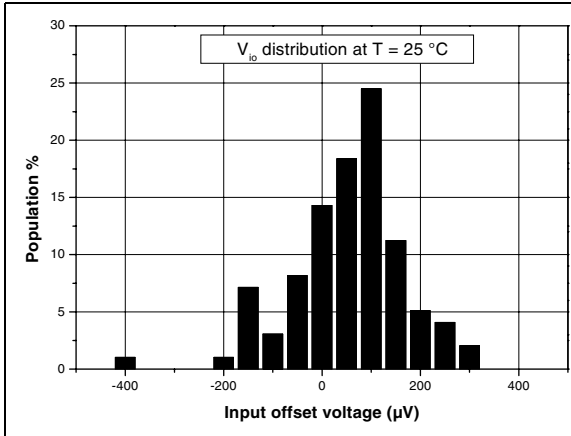


Figure 3.  $V_{io}$  distribution at  $V_{cc} = \pm 15$  V and  $T = 125^\circ\text{C}$

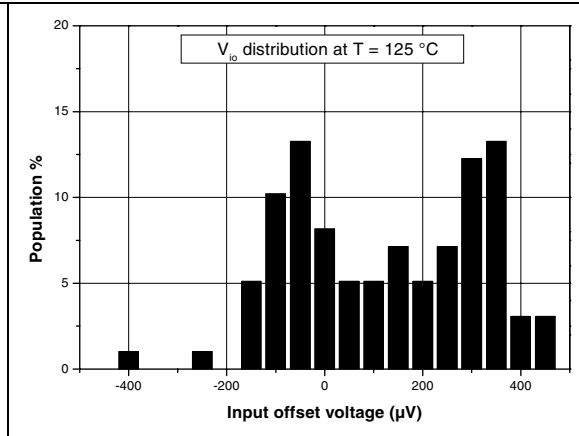


Figure 4. Input offset voltage vs. supply voltage at  $V_{icm} = V_{cc}/2$

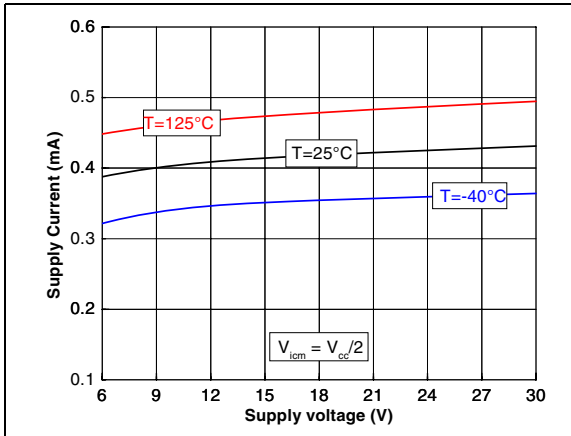


Figure 5. Input offset voltage vs. input common mode voltage at  $V_{cc} = 6$  V

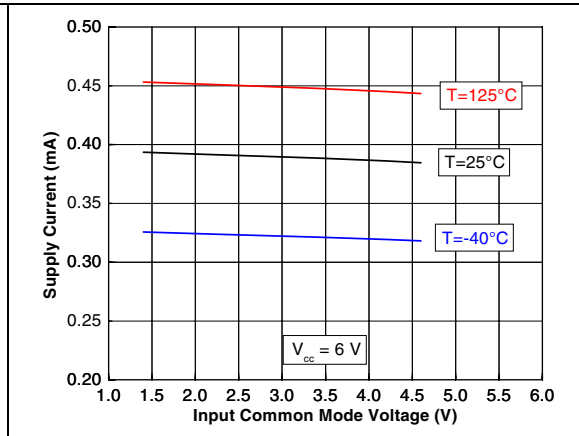


Figure 6. Input offset voltage vs. input common mode voltage at  $V_{cc} = 10$  V

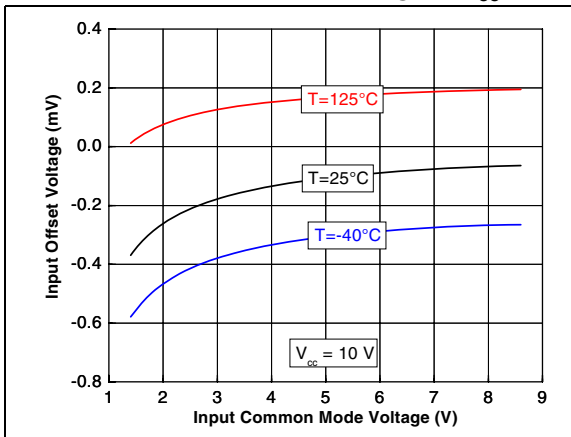


Figure 7. Input offset voltage vs. input common mode voltage at  $V_{cc} = 30$  V

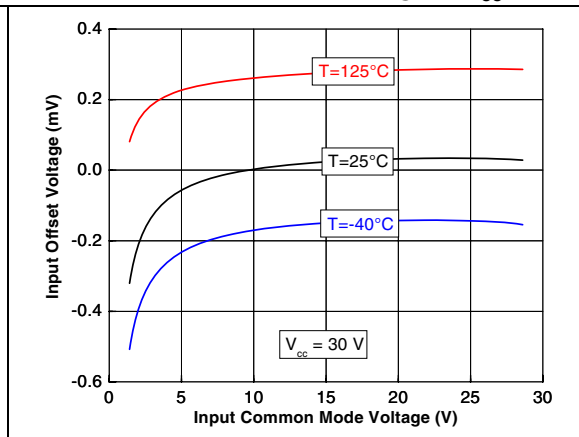


Figure 8. Supply current (per operator) vs. supply voltage at  $V_{icm}=V_{cc}/2$

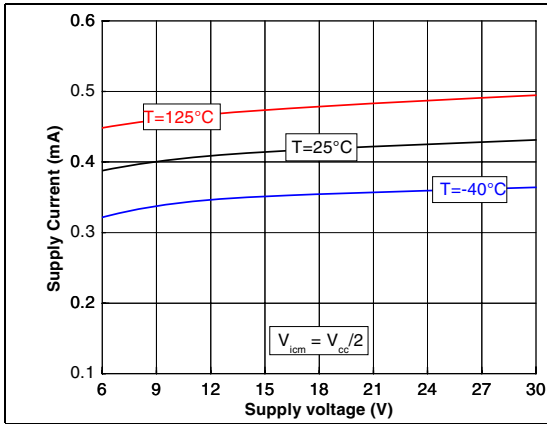


Figure 9. Supply current (per operator) vs. input common mode voltage at  $V_{cc}=6\text{ V}$

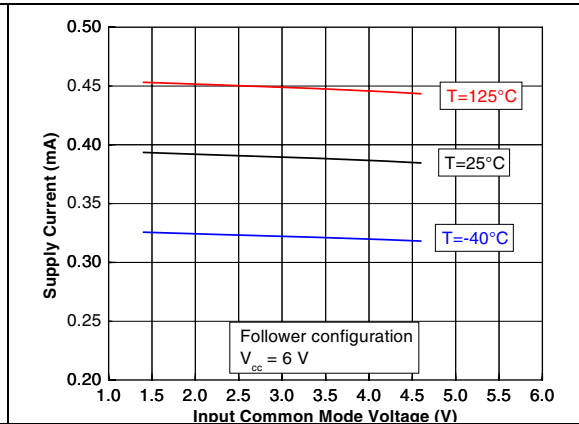


Figure 10. Supply current (per operator) vs. input common mode voltage at  $V_{cc}=10\text{ V}$

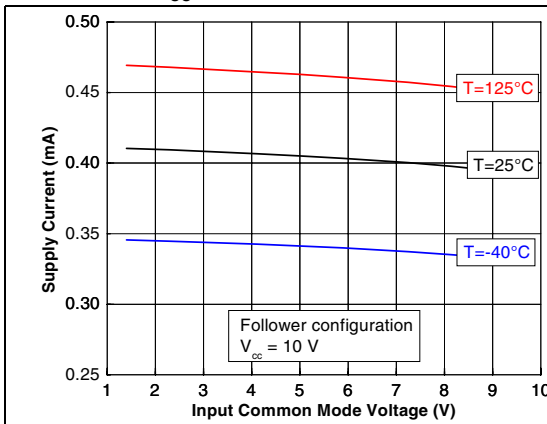


Figure 11. Supply current (per operator) vs. input common mode voltage at  $V_{cc}=30\text{ V}$

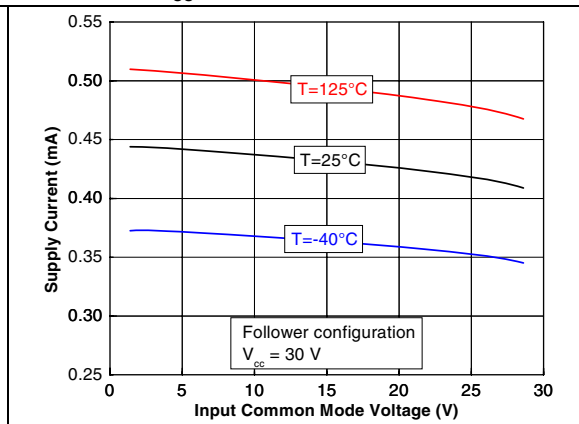


Figure 12. Output current vs. supply voltage at  $V_{icm}=V_{cc}/2$

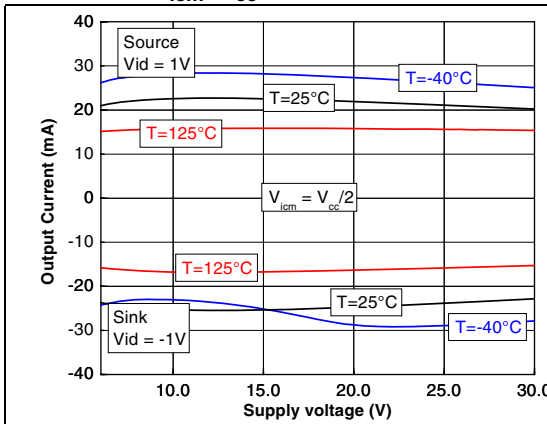


Figure 13. Output current vs. output voltage at  $V_{cc} = 6\text{ V}$

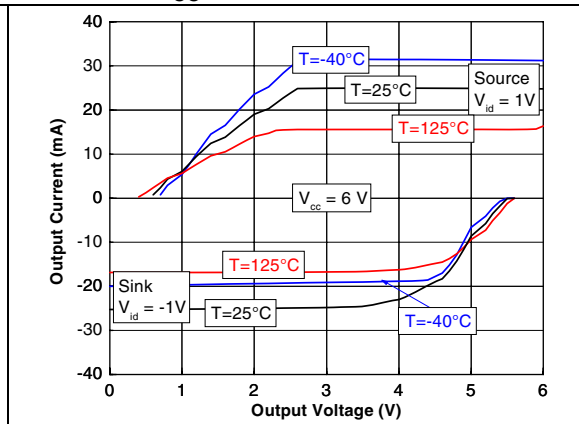


Figure 14. Output current vs. output voltage at  $V_{CC} = 10\text{ V}$

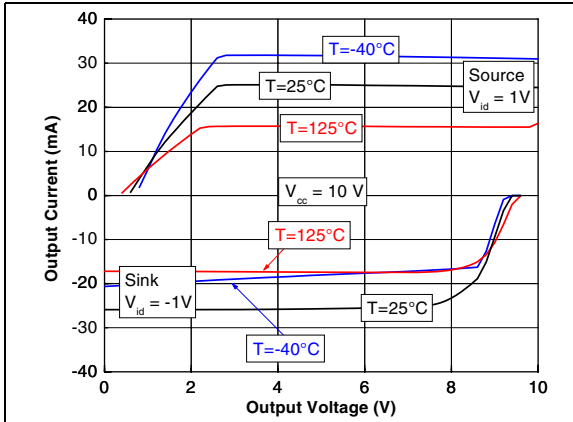


Figure 15. Output current vs. output voltage at  $V_{CC} = 30\text{ V}$

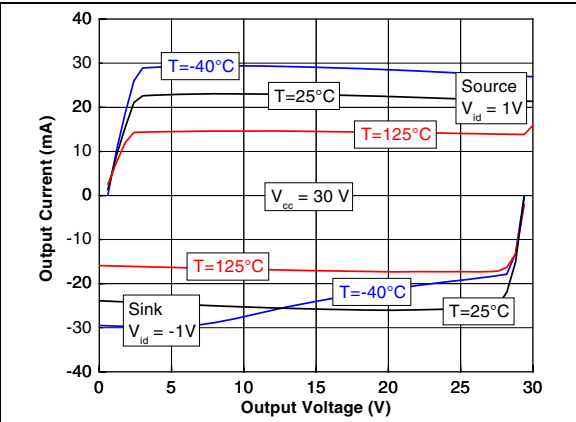


Figure 16. Voltage gain and phase for different capacitive load at  $V_{CC}=6\text{ V}$ ,  $V_{icm}=3\text{ V}$  and  $T=25^\circ\text{ C}$

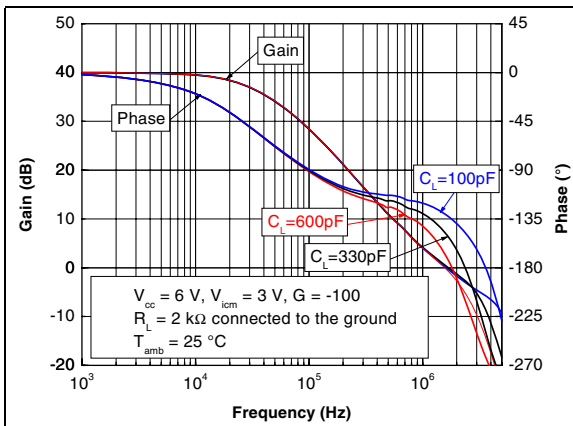


Figure 17. Voltage gain and phase for different capacitive load at  $V_{CC}=10\text{ V}$ ,  $V_{icm}=5\text{ V}$  and  $T=25^\circ\text{ C}$

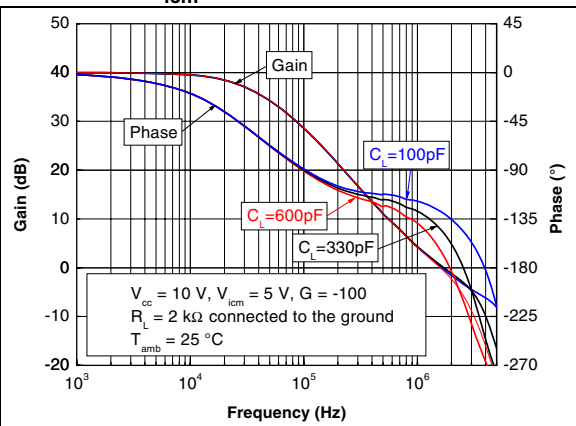


Figure 18. Voltage gain and phase for different capacitive load at  $V_{CC}=30\text{ V}$ ,  $V_{icm}=15\text{ V}$  and  $T=25^\circ\text{ C}$

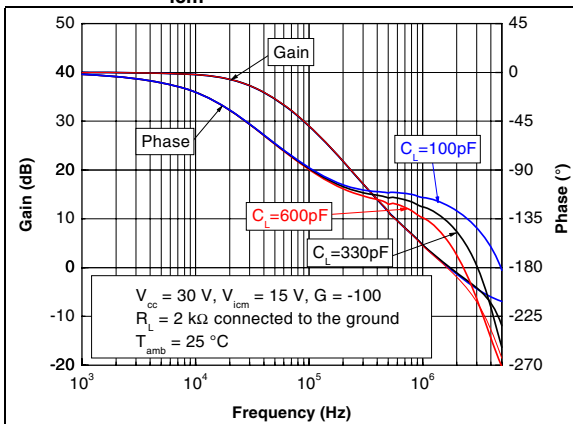


Figure 19. Frequency response for different capacitive load at  $V_{CC}=6\text{ V}$ ,  $V_{icm}=3\text{ V}$  and  $T=25^\circ\text{ C}$

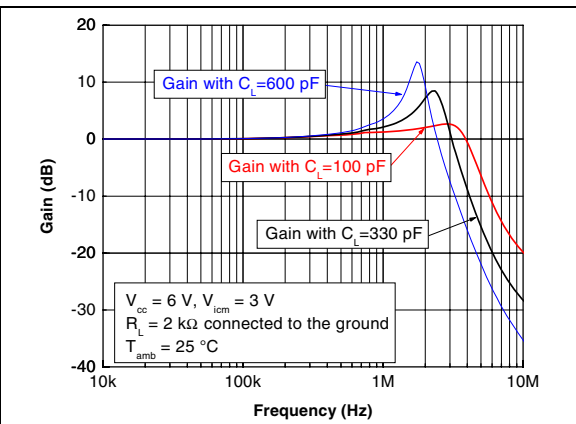




Figure 20. Frequency response for different capacitive load at  $V_{CC}=10\text{ V}$ ,  $V_{icm}=5\text{ V}$  and  $T=25^\circ\text{ C}$

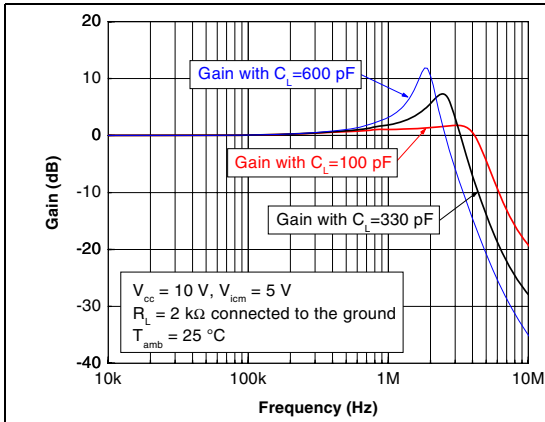


Figure 21. Frequency response for different capacitive load at  $V_{CC}=30\text{ V}$ ,  $V_{icm}=15\text{ V}$  and  $T=25^\circ\text{ C}$

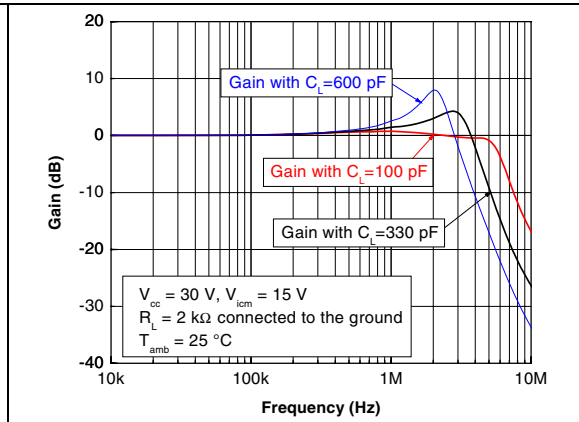


Figure 22. Gain margin vs. output current, at  $V_{CC}=6\text{ V}$ ,  $V_{icm}=3\text{ V}$  and  $T=25^\circ\text{ C}$

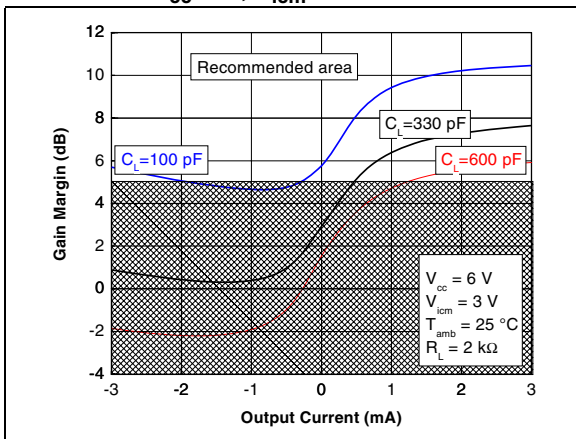


Figure 23. Gain margin vs. output current, at  $V_{CC}=10\text{ V}$ ,  $V_{icm}=5\text{ V}$  and  $T=25^\circ\text{ C}$

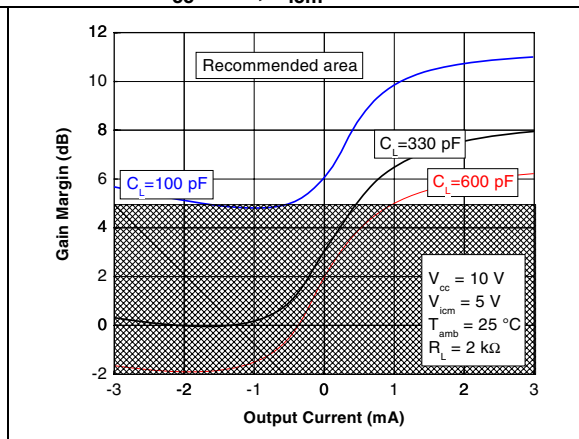


Figure 24. Gain margin vs. output current, at  $V_{CC}=30\text{ V}$ ,  $V_{icm}=15\text{ V}$  and  $T=25^\circ\text{ C}$

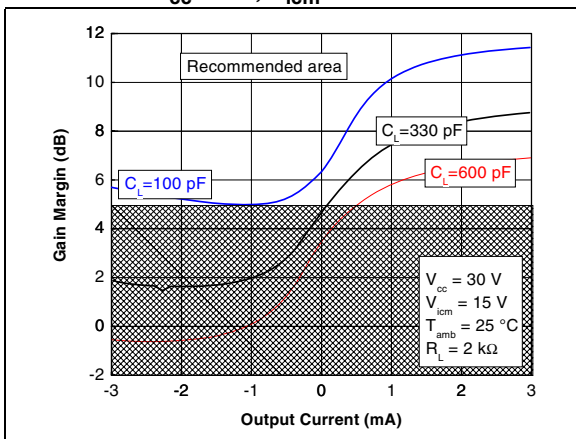


Figure 25. Phase margin vs. output current, at  $V_{CC}=6\text{ V}$ ,  $V_{icm}=3\text{ V}$  and  $T=25^\circ\text{ C}$

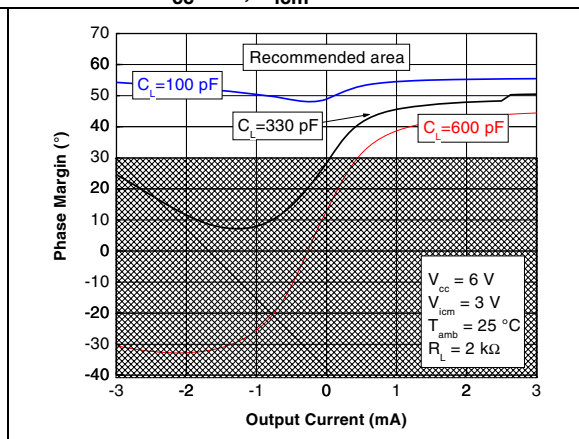
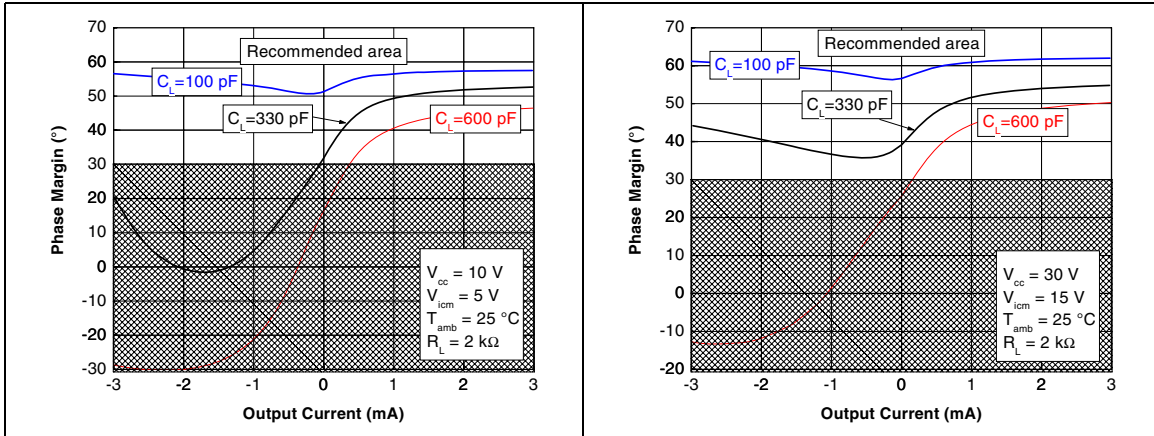


Figure 26. Phase margin vs. output current, at  $V_{cc}=10\text{ V}$ ,  $V_{icm}=5\text{ V}$  and  $T=25^\circ\text{ C}$       Figure 27. Phase margin vs. output current, at  $V_{cc}=30\text{ V}$ ,  $V_{icm}=15\text{ V}$  and  $T=25^\circ\text{ C}$



## 4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 4.1 DIP14 package information

Figure 28. DIP14 package mechanical drawing

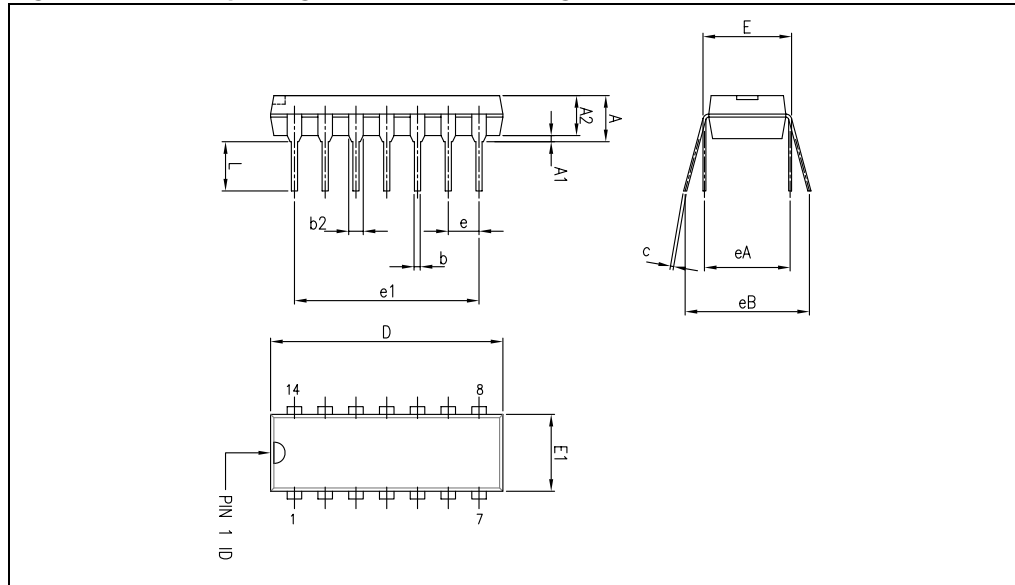


Table 4. DIP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.21
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.11	0.13	0.19
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.04	0.06	0.07
c	0.20	0.25	0.36	0.007	0.009	0.01
D	18.67	19.05	19.69	0.73	0.75	0.77
E	7.62	7.87	8.26	0.30	0.31	0.32
E1	6.10	6.35	7.11	0.24	0.25	0.28
e		2.54			0.10	
e1		15.24			0.60	
eA		7.62			0.30	
eB			10.92			0.43
L	2.92	3.30	3.81	0.11	0.13	0.15

Note: D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm.

## 4.2 SO-14 package information

Figure 29. SO-14 package mechanical drawing

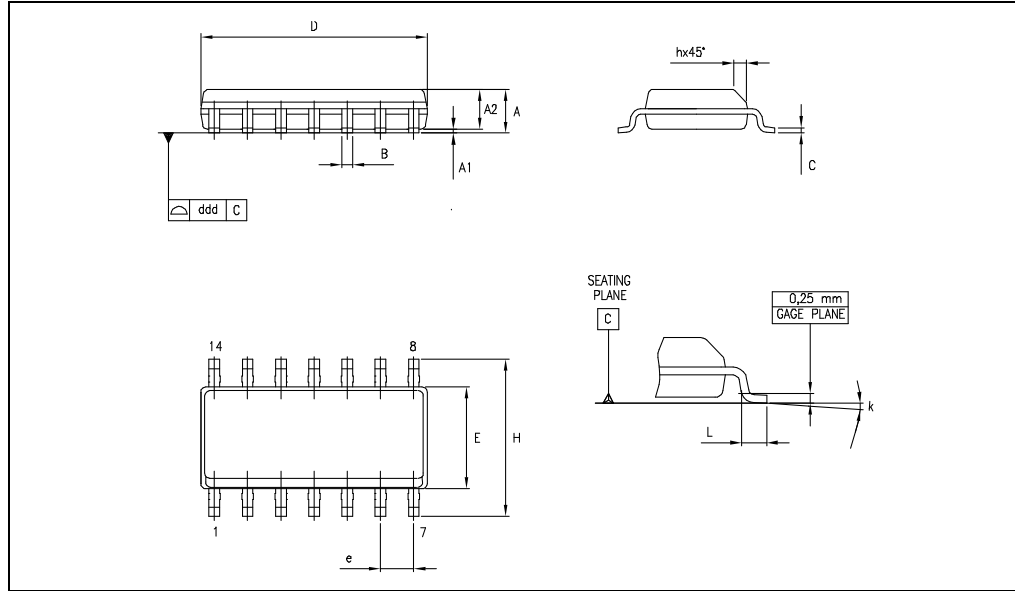


Table 5. SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

Note: D and F dimensions do not include mold flash or protrusions. Mold flash or protrusions must not exceed 0.15 mm.

## 5 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packaging	Marking	
TS514IN	-40, + 125°C	DIP14	Tube	TS514IN	
TS514AIN				TS514AIN	
TS514ID		SO-14	Tube or tape & reel	514I	
TS514IDT				514AI	
TS514AID		SO-14 (automotive grade)		514IY	
TS514AIDT				514AIY	
TS514IYD <sup>(1)</sup>					
TS514IYDT <sup>(1)</sup>					
TS514AIYD <sup>(1)</sup>					
TS514AIYDT <sup>(1)</sup>					

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are ongoing.

## 6 Revision history

Table 7. Document revision history

Date	Revision	Changes
09-Mar-2001	1	Initial release.
23-Jun-2005	2	Automotive grade part references inserted in the datasheet (see <a href="#">Chapter 5: Ordering information on page 14</a> ).
30-Sep-2005	3	The following changes were made in this revision. <ul style="list-style-type: none"> <li>– An error in the device description was corrected on page 1.</li> <li>– <a href="#">Chapter 5: Ordering information on page 14</a> updated with complete list of markings.</li> <li>– Addition of supplementary data in <a href="#">Table 1: Absolute maximum ratings on page 2</a>.</li> <li>– Addition of <a href="#">Table 2: Operating conditions on page 2</a>.</li> <li>– Reorganization of <a href="#">Chapter 4: Package information on page 11</a>.</li> <li>– Minor grammatical and formatting changes throughout.</li> </ul>
24-Oct-2008	4	Added performance AC and DC characteristic curves for $V_{CC}=6$ V, $V_{CC}=10$ V and $V_{CC}=30$ V in <a href="#">Chapter 3: Electrical characteristics</a> . Modified $I_{CC}$ typ, added parameters over temperature in <a href="#">Table 3</a> . Deleted old macromodel. Added $R_{thjc}$ , $R_{thja}$ in <a href="#">Table 1</a> . Corrected $V_i$ and $V_{id}$ AMR values in <a href="#">Table 1</a> . Added input common mode range $V_{icm}$ in <a href="#">Table 2: Operating conditions</a> . Updated <a href="#">Section 4.1: DIP14 package information</a> and <a href="#">Section 4.2: SO-14 package information</a> .

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