

Wide bandwidth dual bipolar operational amplifier

Features

- Operating from $V_{CC} = 2.5\text{ V}$ to 5.5 V
- 200 mA output current on each amplifier
- High dissipation package
- Rail-to-rail input and output
- Unity-gain stable

Applications

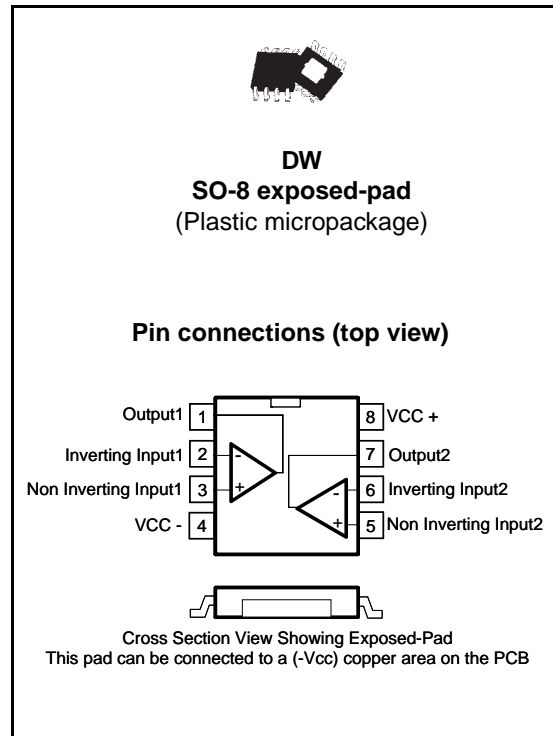
- Hall sensor compensation coil
- Servo amplifier
- Motor driver
- Industrial
- Automotive

Description

The TS982 is a dual operational amplifier able to drive 200 mA down to voltages as low as 2.7 V.

The SO-8 exposed-pad package allows high current output at high ambient temperatures making it a reliable solution for automotive and industrial applications.

The TS982 is stable with a unity gain.



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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

| Symbol | Parameter | Value | Unit |
|------------|---|----------------------------|------|
| V_{CC} | Supply voltage ⁽¹⁾ | 6 | V |
| V_{in} | Input voltage | -0.3 V to $V_{CC} + 0.3$ V | V |
| T_{oper} | Operating free-air temperature range | -40 to + 125 | °C |
| T_{stg} | Storage temperature | -65 to +150 | °C |
| T_j | Maximum junction temperature | 150 | °C |
| R_{thja} | Thermal resistance junction to ambient ⁽²⁾ | 45 | °C/W |
| R_{thjc} | Thermal resistance junction to case | 10 | °C/W |
| ESD | Human body model (HBM) ⁽³⁾ | 2 | kV |
| | Charged device model (CDM) ⁽⁴⁾ | 1.5 | kV |
| | Machine model (MM) ⁽⁵⁾ | 200 | V |
| Latch-up | Latch-up immunity (all pins) | 200 | mA |
| | Lead temperature (soldering, 10sec) | 250 | °C |
| | Output short-circuit duration | see note ⁽⁶⁾ | |

- All voltage values are measured with respect to the ground pin.
- With two sides, two-plane PCB following the EIA/JEDEC JESD51-7 standard.
- Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 k Ω resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
- Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- Short-circuits can cause excessive heating. Destructive dissipation can result from a short-circuit on one or two amplifiers simultaneously.

Table 2. Operating conditions

| Symbol | Parameter | Value | Unit |
|-----------|--|-----------------|------|
| V_{CC} | Supply voltage | 2.5 to 5.5 | V |
| V_{icm} | Common mode input voltage range | GND to V_{CC} | V |
| C_L | Load capacitor | | |
| | $R_L < 100 \Omega$ $R_L > 100 \Omega$ | 400 100 | pF |

2 Electrical characteristics

Table 3. Electrical characteristics for $V_{CC+} = +5\text{ V}$, $V_{CC-} = 0\text{ V}$, and $T_{\text{amb}} = 25^\circ\text{ C}$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--|----------|-----------|--------------|--------------------------------------|
| I_{CC} | Supply current - No input signal, no load $T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$ | | 5.5 | 7.2 7.2 | mA |
| V_{IO} | Input offset voltage ($V_{\text{icm}} = V_{CC}/2$) $T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$ | | 1 | 5 7 | mV |
| ΔV_{IO} | Input offset voltage drift | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IB} | Input bias current - $V_{\text{icm}} = V_{CC}/2$ $T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$ | | 200 | 500 500 | nA |
| I_{IO} | Input offset current $V_{\text{icm}} = V_{CC}/2$ | | 10 | | nA |
| V_{OH} | High level output voltage $R_L = 16\Omega$ $R_L = 16\Omega$, $T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$ $I_{\text{out}} = 200\text{mA}$ | 4.2 4 | 4.4 4 | | V |
| | $V_{CC} = 4.75\text{V}$, $T = 125^\circ\text{C}$, $I_{\text{out}} = 25\text{mA}$ | 4.3 | | | V |
| V_{OL} | Low level output voltage $R_L = 16\Omega$ $R_L = 16\Omega$, $T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$ $I_{\text{out}} = 200\text{mA}$ | | 0.55 1 | 0.65 0.95 | V |
| | $V_{CC} = 4.75\text{V}$, $T = 125^\circ\text{C}$, $I_{\text{out}} = 25\text{mA}$ | | | 0.45 | V |
| A_{VD} | Large signal voltage gain $R_L = 16\Omega$ | | 95 | | dB |
| GBP | Gain bandwidth product $R_L = 32\Omega$ | 1.35 | 2.2 | | MHz |
| CMR | Common mode rejection ratio | | 80 | | dB |
| SVR | Supply voltage rejection ratio | | 95 | | dB |
| SR | Slew rate, unity gain inverting $R_L = 16\Omega$ | 0.45 | 0.7 | | V/ μs |
| Φ_m | Phase margin at unit gain $R_L = 16\Omega$, $C_L = 400\text{pF}$ | | 56 | | degrees |
| G_m | Gain margin $R_L = 16\Omega$, $C_L = 400\text{pF}$ | | 18 | | dB |
| e_n | Equivalent input noise voltage $F = 1\text{kHz}$ | | 17 | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| Crosstalk | Channel separation $R_L = 16\Omega$, $F = 1\text{kHz}$ | | 100 | | dB |

Table 4. Electrical characteristics for $V_{CC+} = +3.3\text{ V}$, $V_{CC-} = 0\text{ V}$, and $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)⁽¹⁾

| Symbol | Table 5. Parameter | Min. | Typ. | Max. | Unit |
|-----------------|---|--------------|-----------------|--------------|--------------------------------------|
| I_{CC} | Supply current - No input signal, no load $T_{min} < T_{op} < T_{max}$ | | 5.3 | 7.2 7.2 | mA |
| V_{IO} | Input offset voltage ($V_{icm} = V_{CC}/2$) $T_{min} < T_{op} < T_{max}$ | | 1 | 5 7 | mV |
| ΔV_{IO} | Input offset voltage drift | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IB} | Input bias current - $V_{icm} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ | | 200 | 500 500 | nA |
| I_{IO} | Input offset current $V_{icm} = V_{CC}/2$ | | 10 | | nA |
| V_{OH} | High level output voltage $R_L = 16\Omega$ $R_L = 16\Omega$, $T_{min} < T_{op} < T_{max}$ $I_{out} = 200\text{ mA}$ | 2.68 2.64 | 2.85 2.3 | | V |
| V_{OL} | Low level output voltage $R_L = 16\Omega$ $R_L = 16\Omega$, $T_{min} < T_{op} < T_{max}$ $I_{out} = 200\text{mA}$ | | 0.45 1 | 0.52 0.65 | V |
| A_{VD} | Large signal voltage gain $R_L = 16\Omega$ | | 92 | | dB |
| GBP | Gain bandwidth product $R_L = 32\Omega$ | 1.2 | 2 | | MHz |
| CMR | Common mode rejection ratio | | 75 | | dB |
| SVR | Supply voltage rejection ratio | | 95 | | dB |
| SR | Slew rate, unity gain inverting $R_L = 16\Omega$ | 0.45 | 0.7 | | V/ μs |
| Φ_m | Phase margin at unit gain $R_L = 16\Omega$, $C_L = 400\text{pF}$ | | 57 | | degrees |
| G_m | Gain margin $R_L = 16\Omega$, $C_L = 400\text{pF}$ | | 16 | | dB |
| e_n | Equivalent input noise voltage $F = 1\text{kHz}$ | | 17 | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| Crosstalk | Channel separation $R_L = 16\Omega$, $F = 1\text{kHz}$ | | 100 | | dB |

1. All electrical values are guaranteed by correlation with measurements at 2.7 V and 5 V.

Table 6. Electrical characteristics for $V_{CC} = +2.7\text{ V}$, $V_{CC-} = 0\text{ V}$, and $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|---|-------------|-----------------|--------------|--------------------------------------|
| I_{CC} | Supply current - No input signal, no load $T_{min} < T_{op} < T_{ma}$ | | 5.3 | 6.4 6.4 | mA |
| V_{IO} | Input offset voltage ($V_{icm} = V_{CC}/2$) $T_{min} < T_{op} < T_{max}$ | | 1 | 5 7 | mV |
| ΔV_{IO} | Input offset voltage drift | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IB} | Input bias current - $V_{icm} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ | | 200 | 500 500 | nA |
| I_{IO} | Input offset current $V_{icm} = V_{CC}/2$ | | 10 | | nA |
| V_{OH} | High level output voltage $R_L = 16\Omega$ $R_L = 16\Omega, T_{min} < T_{op} < T_{max}$ $I_{out} = 20\text{ mA}$ | 2.3 2.25 | 2.85 2.3 | | V |
| V_{OL} | Low level output voltage $R_L = 16\Omega$ $R_L = 16\Omega, T_{min} < T_{op} < T_{max}$ $I_{out} = 200\text{mA}$ | | 0.45 1 | 0.37 0.42 | V |
| A_{VD} | Large signal voltage gain $R_L = 16\Omega$ | | 92 | | dB |
| GBP | Gain bandwidth product $R_L = 32\Omega$ | 1.2 | 2 | | MHz |
| CMR | Common mode rejection ratio | | 75 | | dB |
| SVR | Supply voltage rejection ratio | | 95 | | dB |
| SR | Slew rate, unity gain inverting $R_L = 16\Omega$ | 0.45 | 0.7 | | V/ μs |
| Φ_m | Phase margin at unit gain $R_L = 16\Omega, C_L = 400\text{pF}$ | | 57 | | degrees |
| G_m | Gain margin $R_L = 16\Omega, C_L = 400\text{pF}$ | | 16 | | dB |
| e_n | Equivalent input noise voltage $F = 1\text{kHz}$ | | 17 | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| Crosstalk | Channel separation $R_L = 16\Omega, F = 1\text{kHz}$ | | 100 | | dB |

Figure 1. Current consumption vs. supply voltage

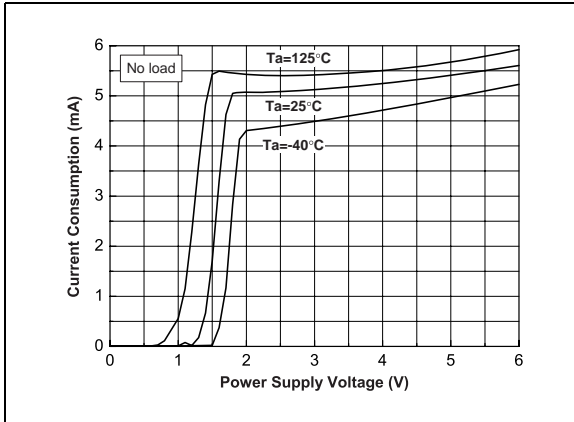


Figure 2. Voltage drop vs. output sourcing current

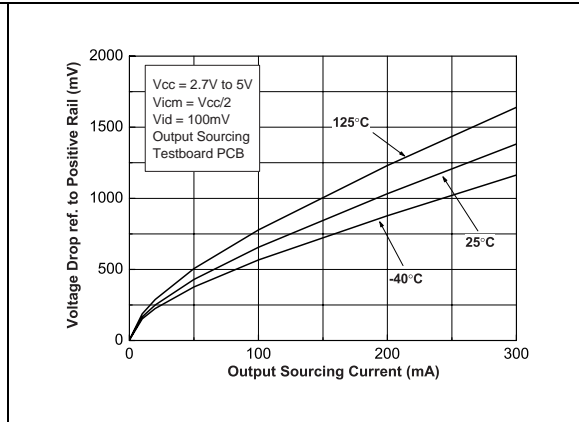


Figure 3. Voltage drop vs. output sinking current

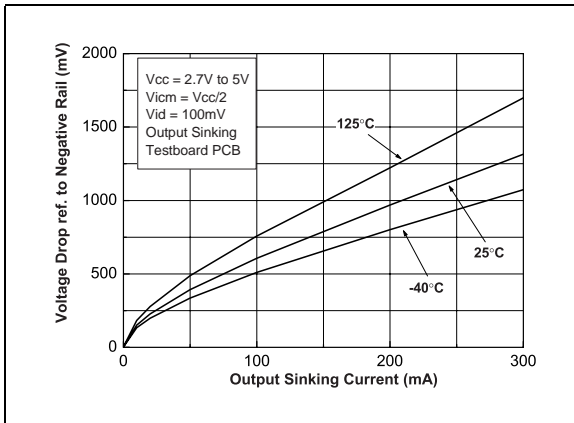


Figure 4. Voltage drop vs. supply voltage (sourcing)

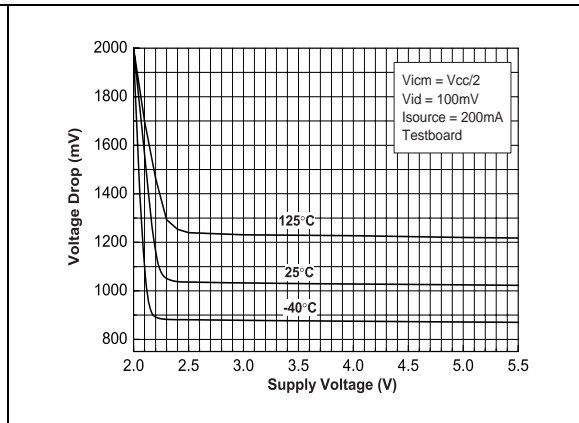


Figure 5. Voltage drop vs. supply voltage (sinking)

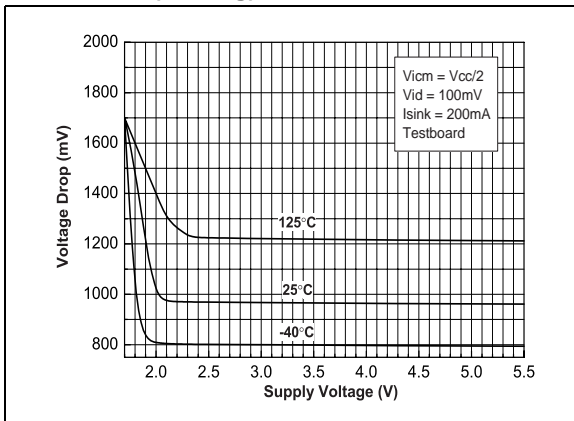


Figure 6. Voltage drop vs. temperature (I_{out} = 50 mA)

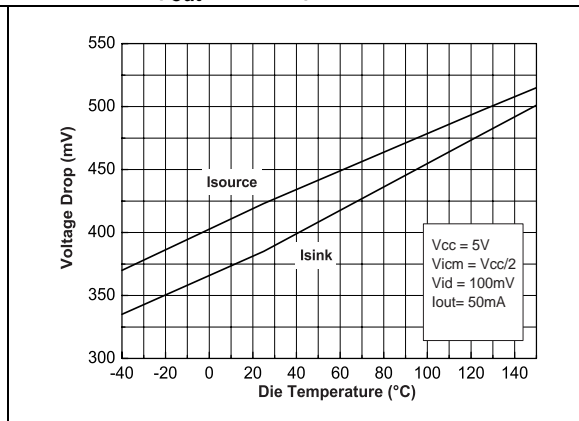


Figure 7. Voltage drop vs. temperature ($I_{out} = 100\text{ mA}$)

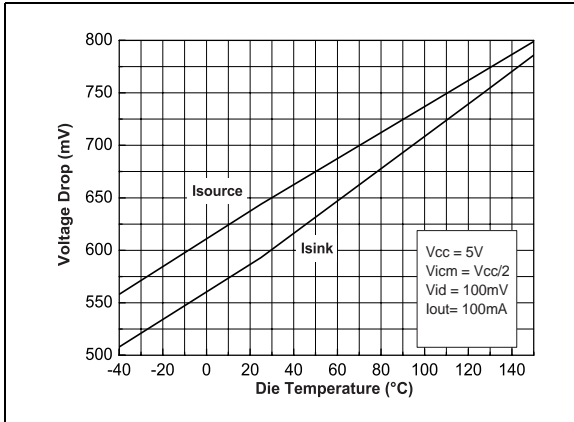


Figure 8. Voltage drop vs. temperature ($I_{out} = 200\text{ mA}$)

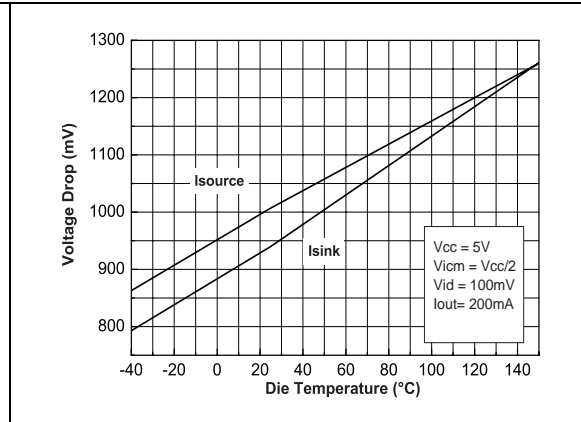


Figure 9. Open loop gain and phase vs. frequency

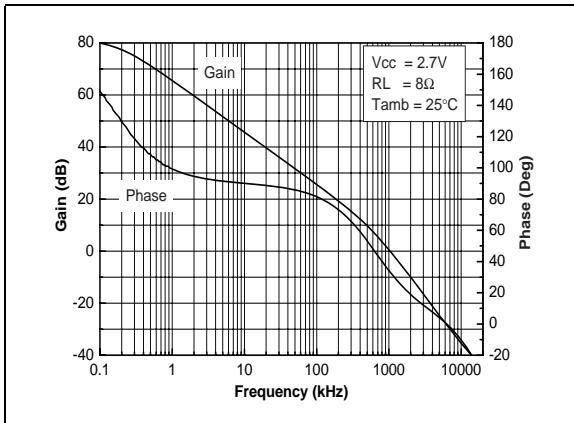


Figure 10. Open loop gain and phase vs. frequency

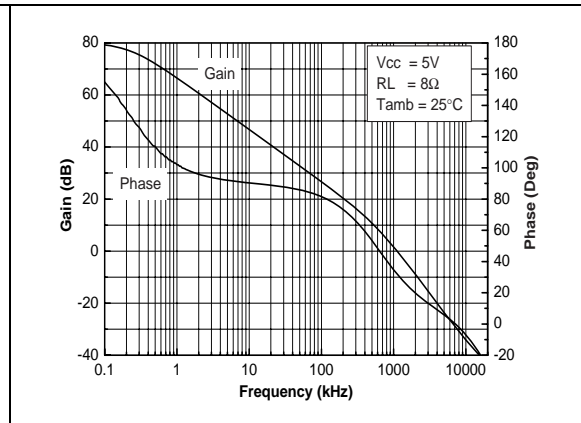


Figure 11. Open loop gain and phase vs. frequency

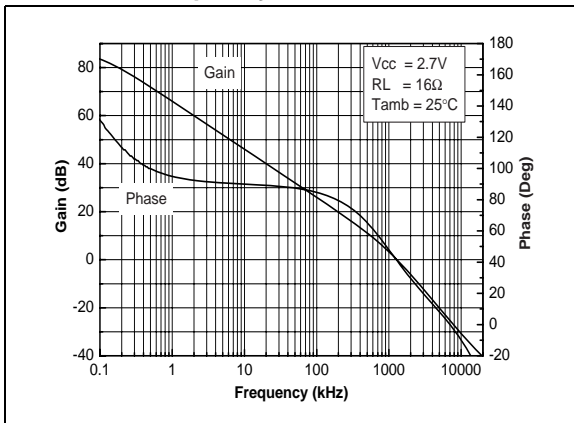


Figure 12. Open loop gain and phase vs. frequency

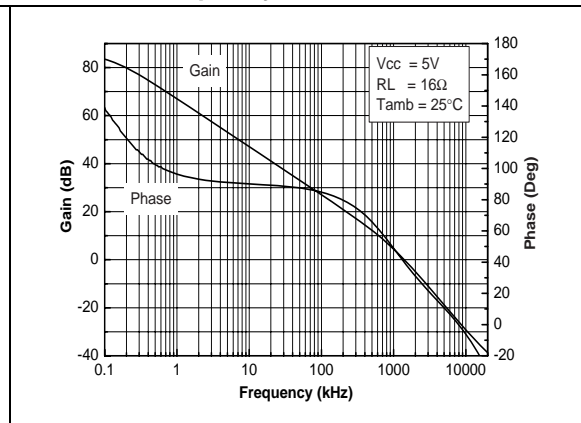


Figure 13. Open loop gain and phase vs. frequency

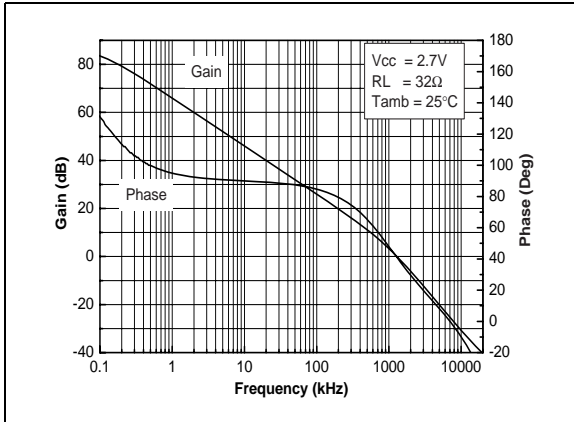


Figure 14. Open loop gain and phase vs. frequency

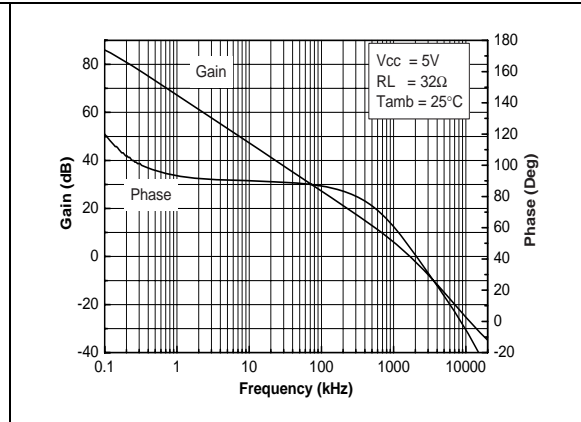


Figure 15. Open loop gain and phase vs. frequency

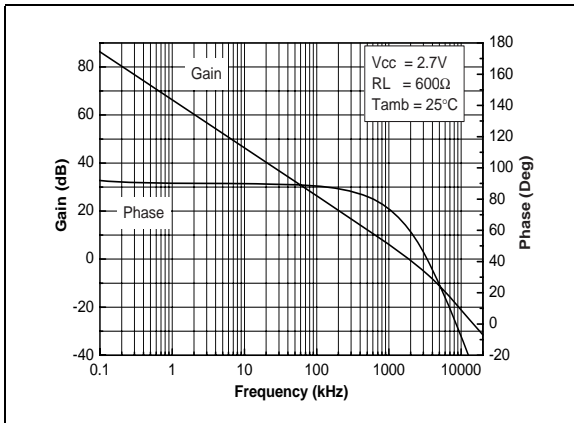


Figure 16. Open loop gain and phase vs. frequency

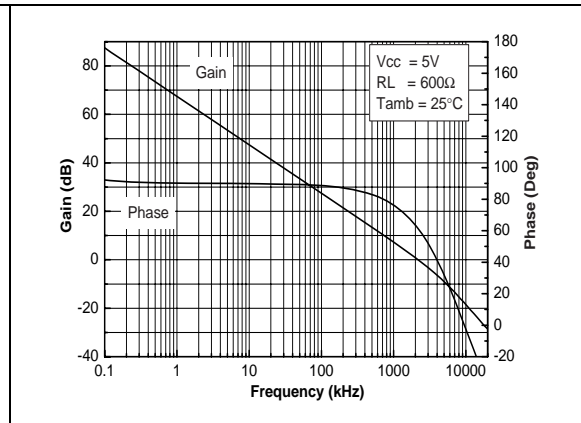


Figure 17. Open loop gain and phase vs. frequency

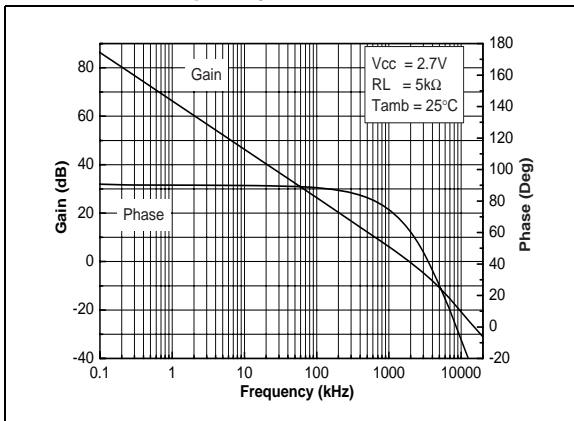


Figure 18. Open loop gain and phase vs. frequency

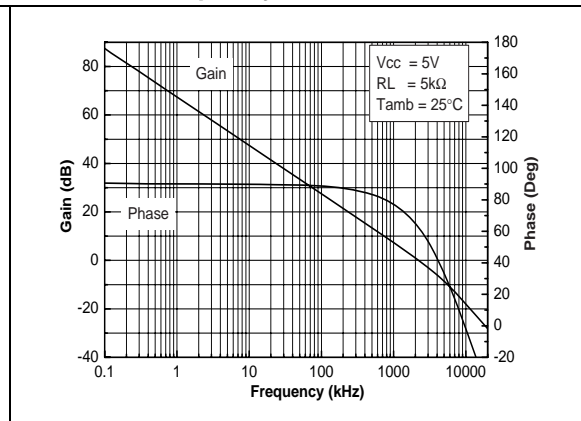


Figure 19. Phase margin vs. supply voltage

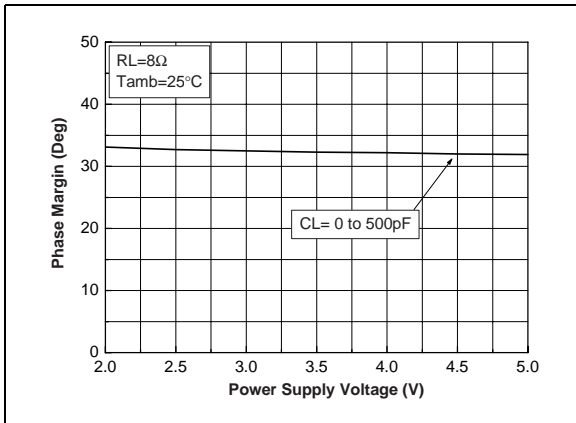


Figure 20. Gain margin vs. supply voltage

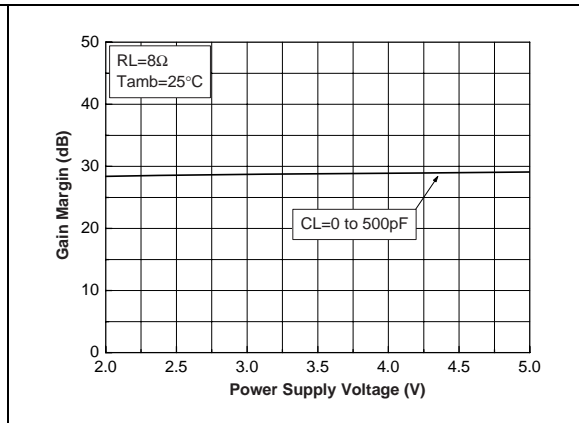


Figure 21. Phase margin vs. supply voltage

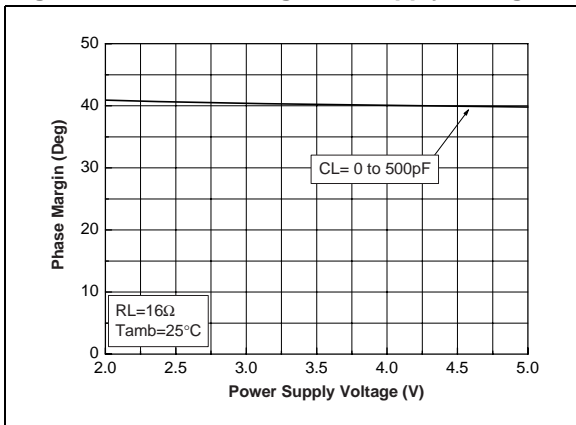


Figure 22. Gain margin vs. supply voltage

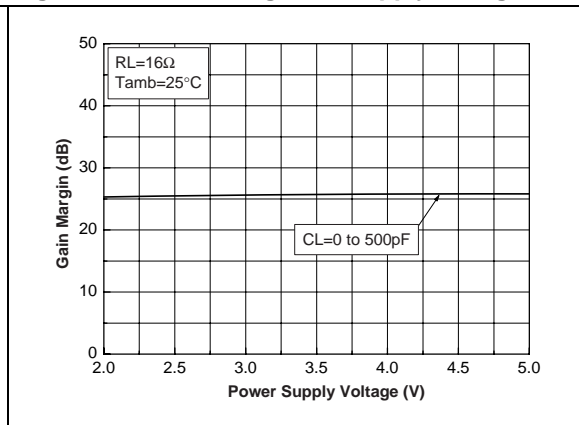


Figure 23. Phase margin vs. supply voltage

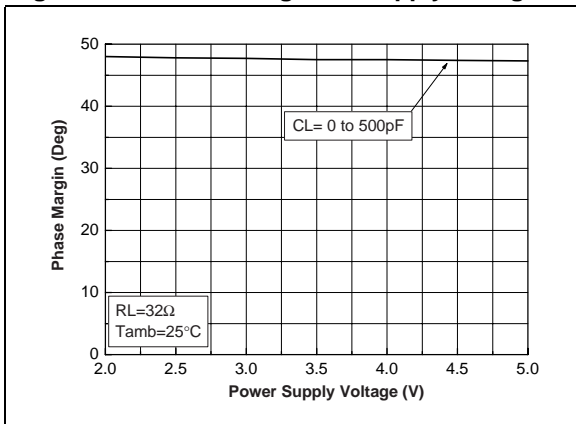


Figure 24. Gain margin vs. supply voltage

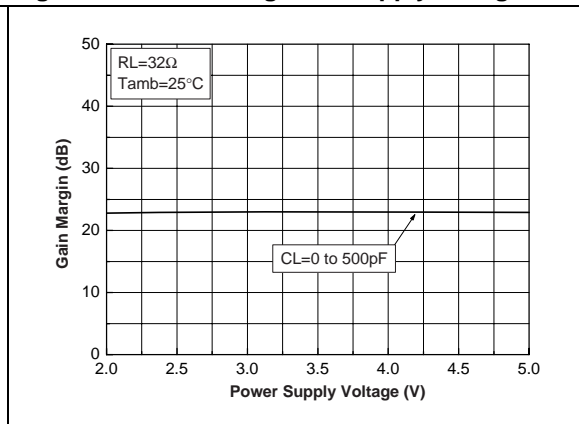


Figure 25. Phase margin vs. supply voltage

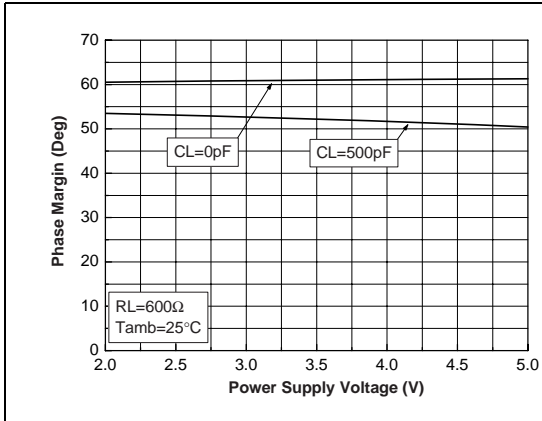


Figure 26. Gain margin vs. supply voltage

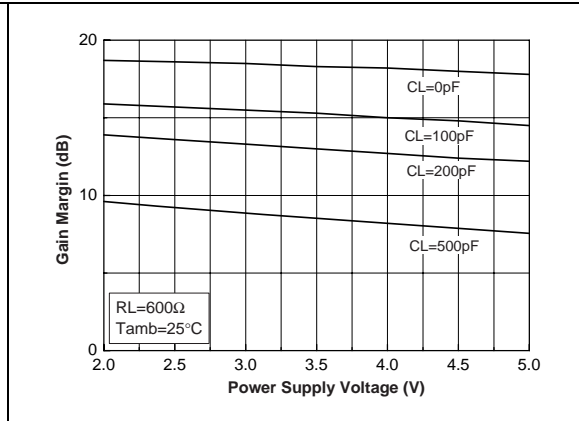


Figure 27. Phase margin vs. supply voltage

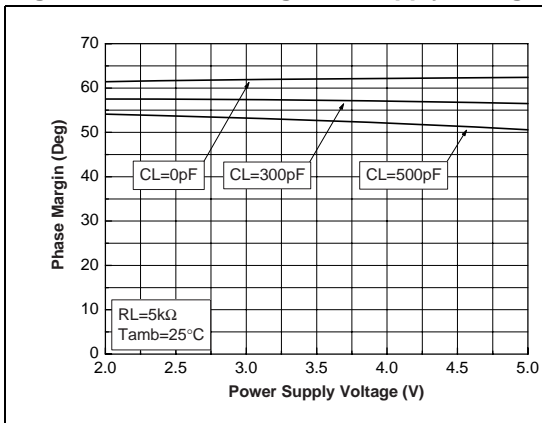


Figure 28. Gain margin vs. supply voltage

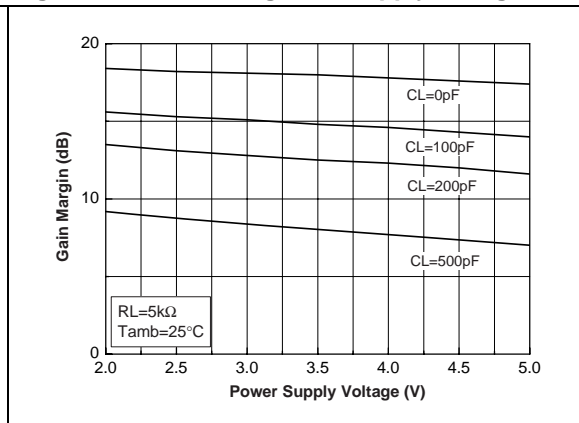


Figure 29. Distortion vs. output voltage

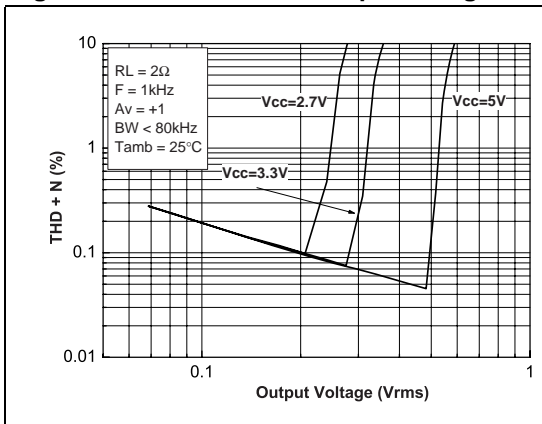


Figure 30. Distortion vs. output voltage

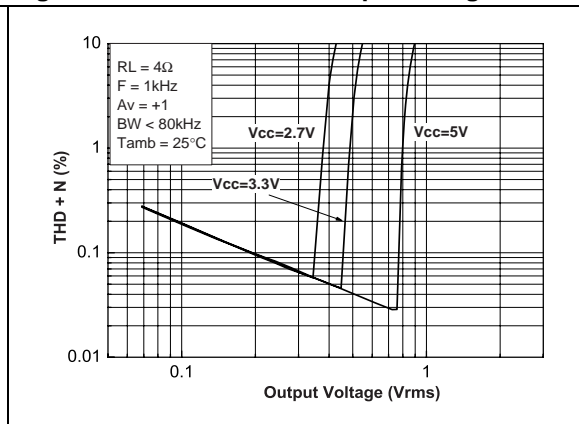


Figure 31. Distortion vs. output voltage

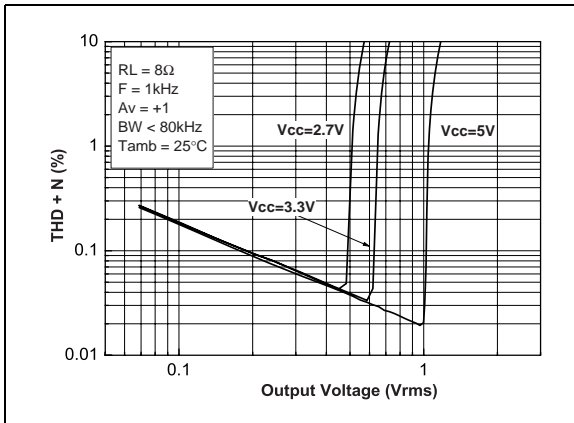


Figure 32. Distortion vs. output voltage

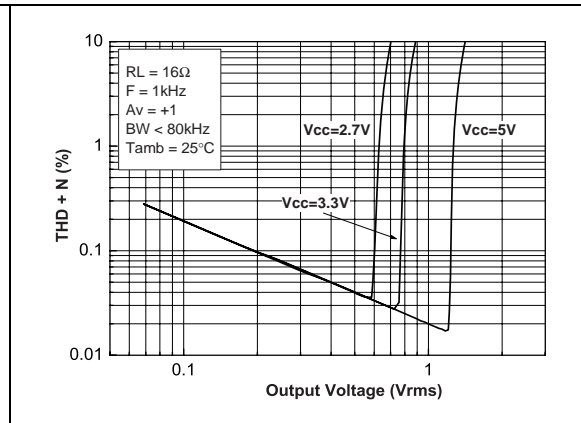


Figure 33. Crosstalk vs. frequency

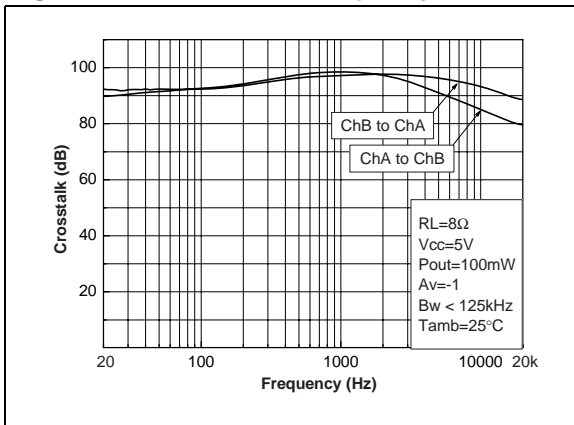


Figure 34. Crosstalk vs. frequency

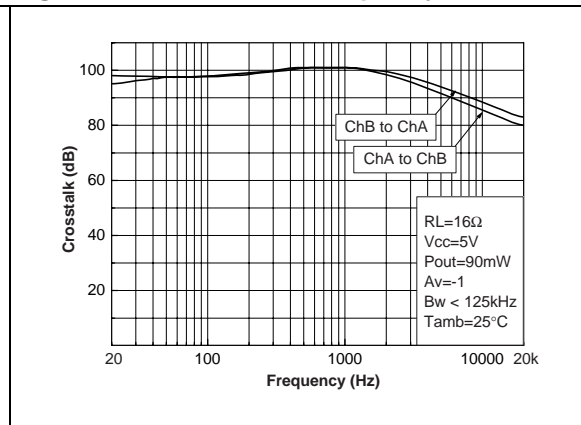


Figure 35. Crosstalk vs. frequency

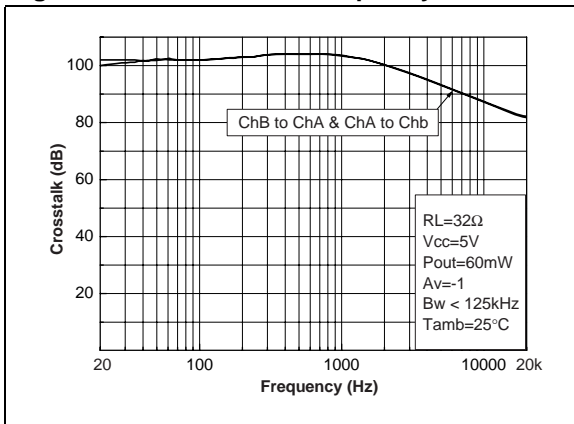


Figure 36. Crosstalk vs. frequency

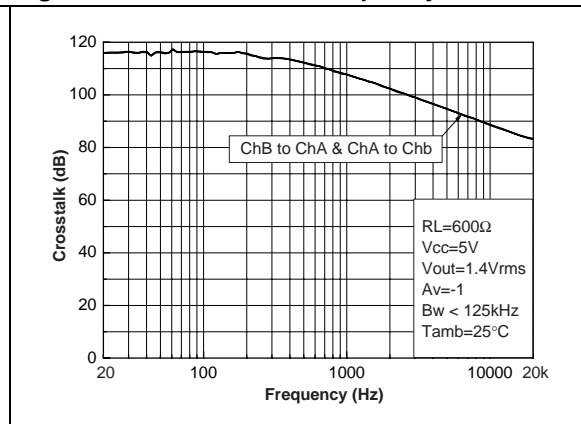


Figure 37. Crosstalk vs. frequency

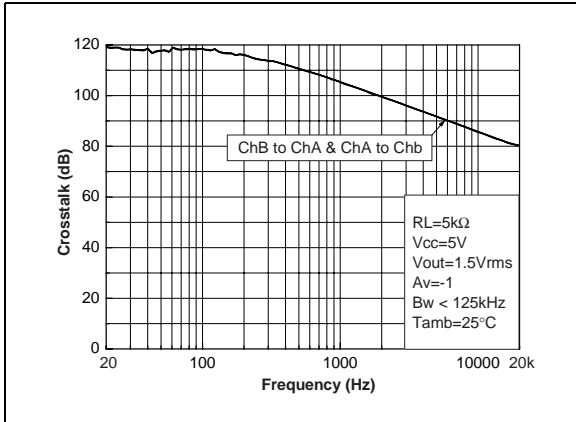


Figure 38. Equivalent input noise voltage vs. frequency

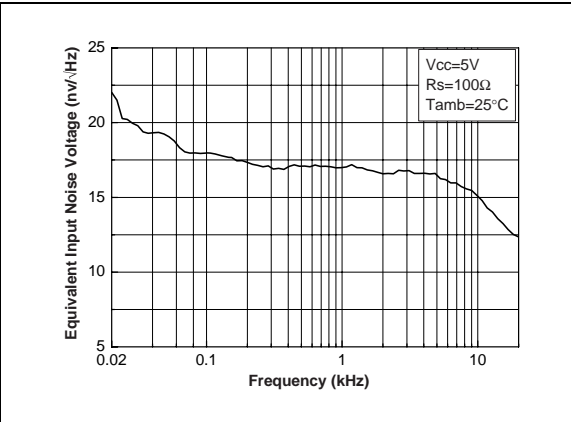
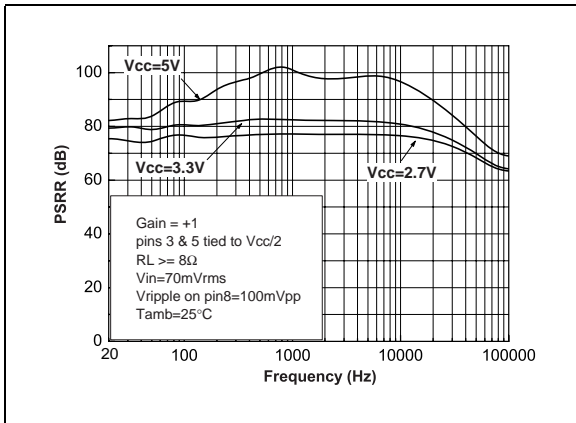


Figure 39. Power supply rejection ratio vs. frequency

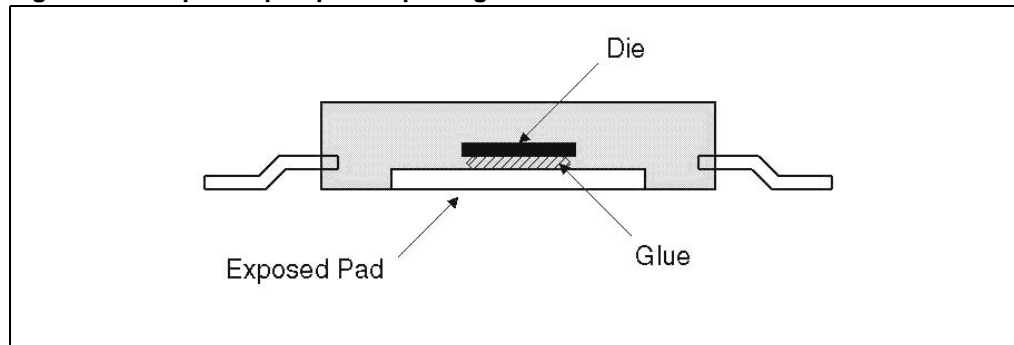


3 Application information

3.1 Exposed-pad package description

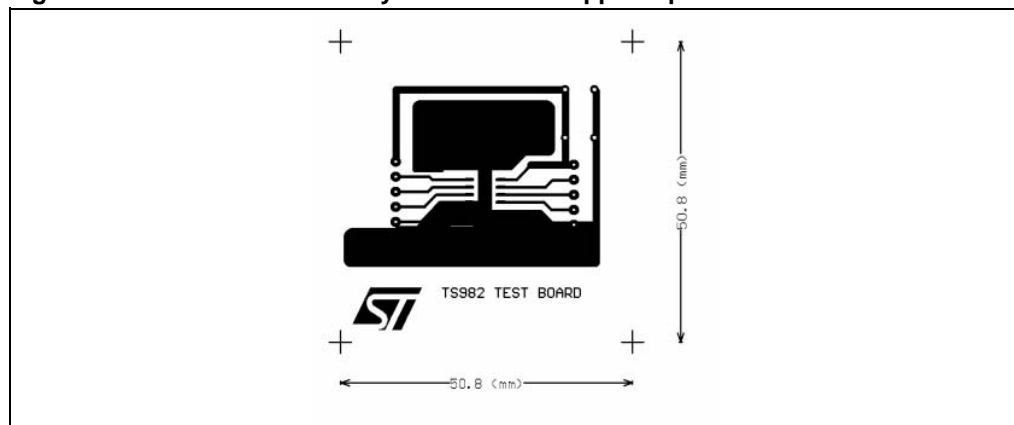
The dual operational amplifier TS982 is housed in an SO-8 exposed-pad plastic package. As shown in [Figure 40](#), the die is mounted and glued on a lead frame. This lead frame is exposed as a thermal pad on the underside of the package. The thermal contact is direct with the die and therefore, offers an excellent thermal performance in comparison with the common SO packages. The thermal contact between the die and the exposed-pad is characterized using the parameter R_{thjc} .

Figure 40. Exposed-pad plastic package



As 90% of the heat is removed through the pad, the thermal dissipation of the circuit is directly linked to the copper area soldered to the pad. In other words, the R_{thja} depends on the copper area and the number of layers of the printed circuit board under the pad.

Figure 41. TS982 test board layout: 6 cm² of copper topside



3.2 Exposed-pad electrical connection

In the SO-8 exposed-pad package, the silicon die is mounted on the thermal pad (see [Figure 40](#)). The silicon substrate is not directly connected to the pad because of the glue. Therefore, the copper area of the exposed-pad must be connected to the substrate voltage (V_{CC^-}) pin 4.

3.3 Thermal management benefits

A good thermal design is important to maintain the temperature of the silicon junction below $T_j = 150^\circ\text{C}$ as given in the absolute maximum ratings and also to maintain the operating power level.

Another effect of temperature is that the life expectancy of an integrated circuit decreases exponentially when operating at high temperature over an extended period of time. It is estimated that, the chip failure rate doubles for every 10° to 20°C . This demonstrates that reducing the junction temperature is also important to improve the reliability of the amplifier.

Because of the high dissipation capability of the SO-8 exposed-pad package, the dual op-amp TS982 has a lower junction temperature for high current applications in high ambient temperatures.

3.4 Thermal management guidelines

The following guidelines are a simple procedure to determine the PCB you should use in order to get the best from the SO-8 exposed-pad package:

1. Determine the total power P_{total} to be dissipated by the IC.

$$P_{\text{total}} = I_{\text{CC}} \times V_{\text{CC}} + V_{\text{drop1}} \times I_{\text{out1}} + V_{\text{drop2}} \times I_{\text{out2}}$$

$I_{\text{CC}} \times V_{\text{CC}}$ is the DC power needed by the TS982 to operate with no load. Refer to [Figure 1: Current consumption vs. supply voltage on page 7](#) to determine I_{CC} versus V_{CC} and versus temperature.

The other terms are the power dissipated by the two operators to source the load. If the output signal can be assimilated to a DC signal, you can calculate the dissipated power using the voltage drop curves versus output current, supply voltage, and temperature ([Figure 2 on page 7](#) to [Figure 8 on page 8](#)).

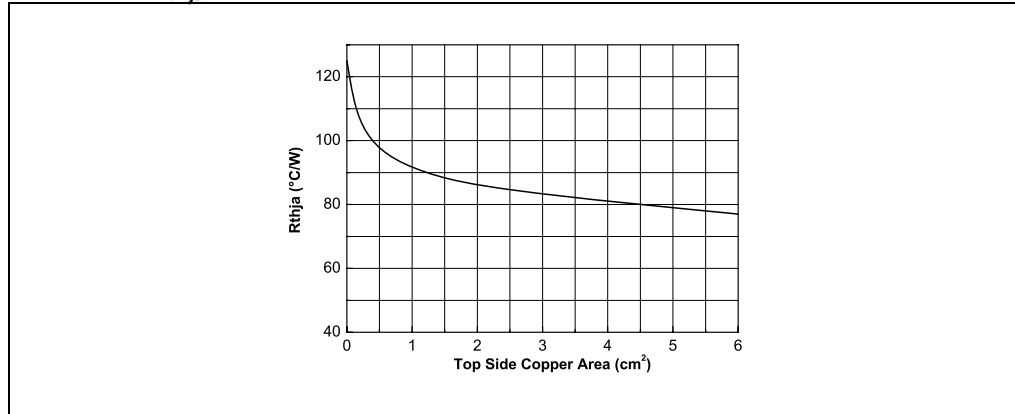
2. Specify the maximum operating temperature, (T_a) of the TS982.
3. Specify the maximum junction temperature (T_j) at the maximum output power. As discussed above, T_j must be below 150°C and as low as possible for reliability considerations.

Therefore, the maximum thermal resistance between junction and ambient R_{thja} is:

$$R_{\text{thja}} = (T_j - T_a) / P_{\text{total}}$$

Different PCBs can give the right R_{thja} for a given application. [Figure 42](#) gives the R_{thja} of the SO-8 exposed pad versus the copper area of a top side PCB.

Figure 42. R_{thja} of the TS982 vs. top side copper area

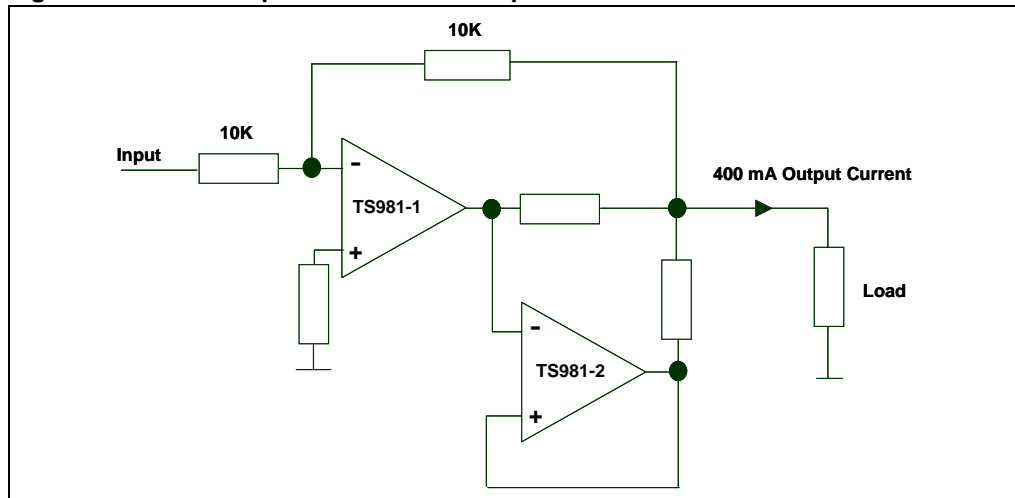


The ultimate R_{thja} of the package on a 4-layer PCB under natural convection conditions, is 45° C/W by using two power planes and metallized holes.

3.5 Parallel operation

Using the two amplifiers of the TS982 in parallel mode provides a higher output current: 400 mA.

Figure 43. Parallel operation: 400 mA output current



4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 44. SO-8 exposed pad package mechanical drawing

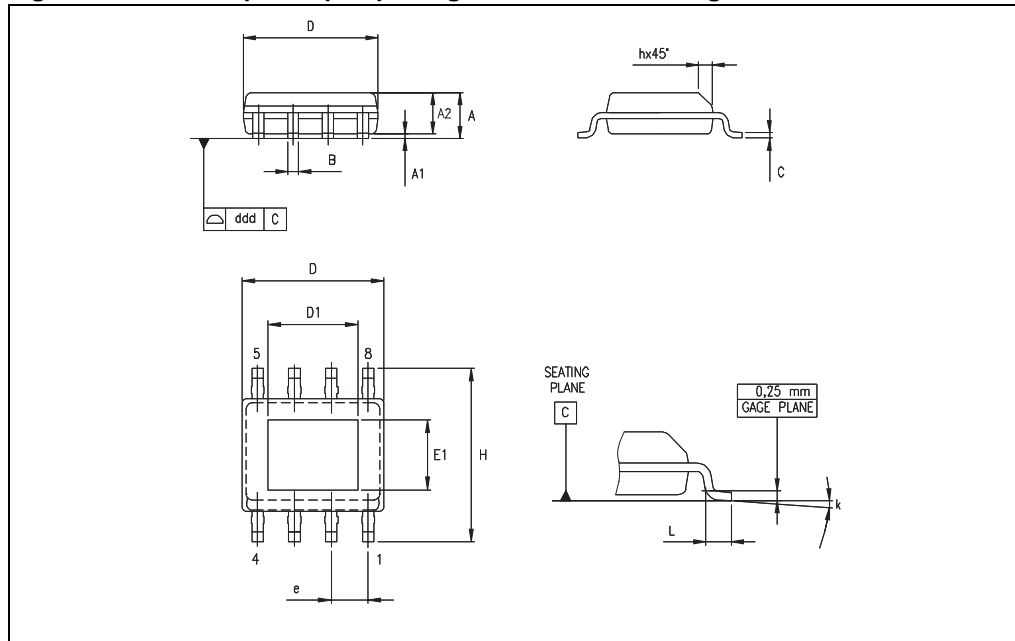


Table 7. SO-8 exposed pad package mechanical data

| Ref. | Dimensions | | | | | |
|------|-------------|------|------|--------|-------|-------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.15 | 0.04 | | 0.059 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D | 4.80 | | 5.00 | 0.189 | | 0.197 |
| D1 | 3.1 | | | 0.122 | | |
| E | 3.80 | | 4.00 | 0.150 | | 0.157 |
| E1 | 2.41 | | | 0.095 | | |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 8° (max.) | | | | | |
| ddd | | | 0.1 | | | 0.04 |

5 Ordering information

Table 8. Order codes

| Order code | Temperature range | Package | Packing | Marking |
|---------------------------|-------------------|--|-------------|---------|
| TS982IDW | -40° C to +125° C | SO-8 exposed-pad | Tube | TS982I |
| TS982IDWT | | | Tape & reel | |
| TS982IYDW ⁽¹⁾ | | SO-8 exposed-pad (Automotive grade) | Tube | TS982IY |
| TS982IYDWT ⁽¹⁾ | | | Tape & reel | |

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|--------------|----------|---|
| 02-Jan-2004 | 1 | First release. |
| 01-Feb- 2004 | 2 | Order codes modified on cover page. |
| 01-Dec-2005 | 3 | PPAP references inserted in the datasheet see Table 5: Ordering information on page 19 . |
| 02-Apr-2006 | 4 | V_{OH} and V_{OL} limits (at $V_{CC} = 4.75$ V, $T_{amb} = 125^{\circ}$ C) added in Table 3. on page 4 . |
| 24-Oct-2006 | 5 | Corrections to Section 3.3: Thermal management benefits and Section 3.4: Thermal management guidelines on page 15 . Pad size added to package mechanical data table under SO-8 exposed pad package mechanical drawing on page 18 , and stand-off value corrected. Corrected value of V_{OH} for $V_{CC} = 2.7$ V. |
| 5-Jun-2008 | 6 | Moved ordering information from cover page to end of document. Added footnotes for ESD parameters in Table 1: Absolute maximum ratings (AMR) . Added footnote for automotive grade parts in Table 8: Order codes . |

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