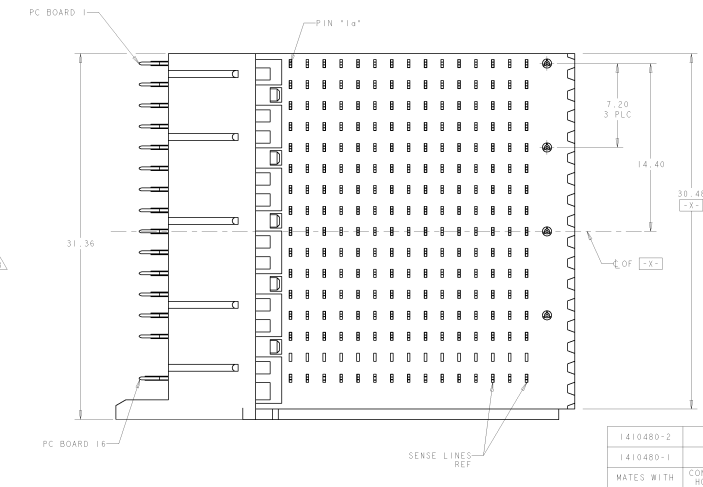
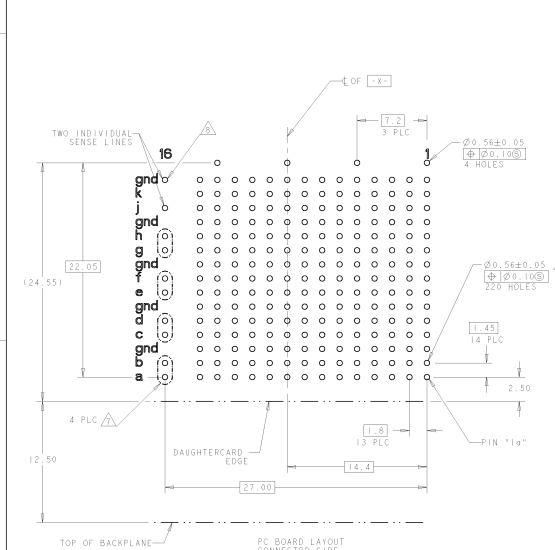
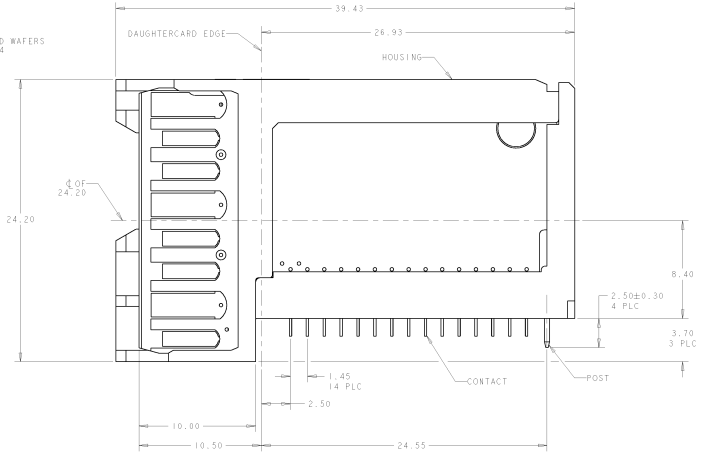
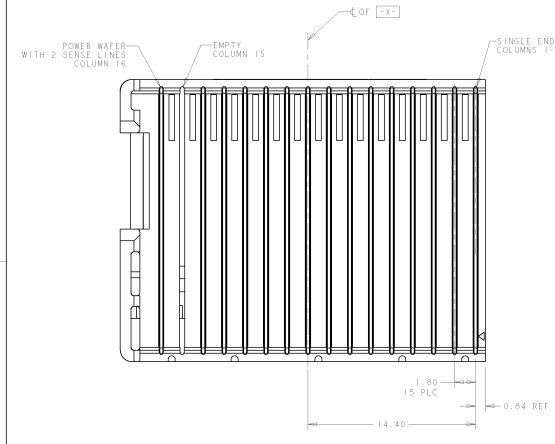


DATE: 08/11/2005	DESIGNED BY: J. J. J.
BY: T. J. J.	BY: T. J. J.

REV	DATE	DESCRIPTION	BY	CHKD	APP'D
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- △ HOUSING: LOP, UL94V-0, BLACK. CONTACT: PHOSPHOR BRONZE. POST: BRASS WIRE.
- △ CONTACT: 0.76µm GOLD PER ASTM B 488 IN CONTACT AREA. 1.27µm MIN TIN-LEAD ON COMPLIANT PORTION OF PCB TAIL. BOTH OVER 1.27µm MIN NICKEL PER SAE AMS-QQ-N-290 ALL OVER.
- POST: 1.27µm MIN NICKEL.
- △ MANUFACTURING TOLERANCE FOR A Ø0.56±0.02 FINISHED HOLE: DRILLED HOLE: Ø0.65±0.02 COPPER PLATING: 0.025 - 0.050 TIN/LEAD PLATE: 0.0038 - 0.0124
- △ CONTACT: 0.76µm GOLD PER ASTM B 488 IN CONTACT AREA. 0.508µm MIN MATTE TIN PER ASTM B 545 ON COMPLIANT PORTION OF PCB TAIL. BOTH OVER 1.27µm MIN NICKEL PER SAE AMS-QQ-N-290 ALL OVER.
- POST: 1.27µm MIN NICKEL.
- △ MANUFACTURING TOLERANCE FOR A Ø0.575±0.045 FINISHED HOLE WITHOUT TIN LEAD PLATING: DRILLED HOLE: Ø0.65 ±0.02 COPPER PLATING: 0.025 - 0.050
- 6. MATING SEQUENCE: POWER & GROUNDS ARE LEVEL 3, SIGNALS ARE LEVEL 2, AND TWO SENSE LINES ARE LEVEL 1.
- △ POWER PIN PAIRS INDICATED ARE COMMONED INSIDE ASSEMBLY.
- △ PIN INDICATED CONNECTS TO PIN K-16 ON BACKPLANE CONNECTOR.

1410480-2	14 SINGLE ENDED WAFERS AND 1 48V POWER WAFER	1410479-2																																										
1410480-1	14 SINGLE ENDED WAFERS AND 1 48V POWER WAFER	1410479-1																																										
MATES WITH	CONTACT TAIL/ HOLE FINISH	DESCRIPTION																																										
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