RJ45 Modular Stacked Jack With Integrated Magnetics and Integrated Power over Ethernet (PoE)

1. SCOPE

1.1. Content

This specification covers the performance, tests and quality requirements for the Tyco Electronics Right Angle Stacked RJ45 with LED's and Power over Ethernet (PoE) capability designed for intra-building use only. The RJ45 Modular Stacked Jack With Integrated Magnetics and Integrated PoE integrates new and existing technologies into a single connector unit that provides power compliant to IEEE Standard 802.3af to devices through a standard RJ45 modular jack by sharing data contacts.

1.2. Qualification

When tests are preformed on the subject product line, procedures specified in Figure 1 shall be used. All inspections shall be performed using the applicable inspection plan and product drawing.

1.3. Qualification Test Results

Successful qualification testing on the subject product line was completed on 10Apr07. The Qualification Test Report number for this testing is 501-653. This documentation is on file at and available from Engineering Practices and Standards (EPS).

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent herein. Unless otherwise specified, the latest edition of the document applies. In the even of conflict between the requirements of this specification and the product drawing, the product drawing shall take precedence. In the event of conflict between the requirements of this specification and the referenced documents, this specification shall take precedence.

2.1. Tyco Electronics Documents

- 109-197: Test Specification (AMP Test Specifications vs EIA and IEC Test Methods)
- 501-653: Qualification Test Report (RJ45 Modular Stacked Jack With Integrated Magnetics and Integrated Power Over Ethernet (PoE))

2.2. Commercial Standards

- EIA-364: Electrical Connector/Socket Test Procedure Including Environmental Classifications
- ANSI X3.263: Information Technology - Fibre Distributed Interface (MDI) - Token Ring Twisted Pair Physical Layer Medium Dependent (TP-PDM)
- IEEE 802.3: Local Area Network; Carrier Sense Multiple Access With Collision Detection (CSMA/CD) Access Method and Physical Layer Specification
- TIA-568-A: Commercial Building Telecommunications Cabling Standards

3. REQUIREMENTS

3.1. Design and Construction

Product shall be of the design, construction and physical dimensions specified on the applicable product drawing.

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3.2. Materials

Materials used in the construction of this product shall be as specified on the applicable product drawing.

3.3. Ratings

- Voltage: 48 volts DC for signal pairs, 2 volts DC for LED signals
- Current:
  - 0.1 ampere maximum per signal contact
  - 0.020 ampere maximum for LED signals
  - 0.275 ampere maximum per contact, PoE contact, RJ45
  - 1.5 ampere maximum per contact, host board connector, 48 volts DC, PoE contacts only Integrated and Enabled PoE connectors only
- Temperature:
  - Storage: -40 to 85˚C
  - Operating: 0 to 70˚C
  - Operating: 0 to 50˚C, Integrated PoE only

3.4. Performance and Test Description

Product is designed to meet the electrical, mechanical, and environmental performance requirements specified in Figure 1. Unless otherwise specified, all tests shall be performed at the ambient environmental conditions per EIA-364.

3.5. Test Requirements and Procedure Summary

Test Description	Requirement	Procedure
Examination of product.	Meets requirements of product drawing.	EIA-364-18. Visual and dimensional (C of C) inspection per product drawing.
ELECTRICAL		
Low-level contact resistance, RJ45 interface, cable and board side.	ΔR 40 milliohms maximum.	EIA-364-23. Subject specimens to 100 milliamperes maximum and 20 millivolts maximum open circuit voltage. Measure the DC resistance across each of the 4 signal pairs on the RJ45 interface (pins 1-2, 3-6, 4-5, 7-8). See Figures 4 and 5.
Open Circuit Inductance (OCL), cable side only.	350 µh minimum.	ANSI X3.263, ref IEEE 802.3. Measure and record OCL across the signal pairs of mated specimens at 100 kHz, 100 millivolts, 8 milliamperes DC bias, and 25˚C at the RJ45 interface.

Figure 1 (continued)

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Test Description	Requirement	Procedure
Insulation resistance.	500 megohms minimum.	EIA-364-21. Test between adjacent contacts of mated specimens that are not electrically connected (pairs 3-4, 4-5 and 6-7). 500 volts DC, 2 minute hold.
Withstanding voltage.	1 minute hold with no breakdown or flashover.	EIA-364-20. For mated plug and jack, all ports: 1500 volts AC RMS between adjacent plug and PCB contacts, including shield that is not electrically connected, 15 milliamperes cutoff current, 500 volts per second maximum ramp. All bridged on either side of magnetics package for RJ45 contacts. 60 second dwell. See Figures 7 and 8.
Crosstalk (NEXT).	33 - 20 X log (F/50) dB minimum from 1 to 100 MHz.	EIA-568-A.
Insertion loss.	1.3 dB maximum from 0.5 to 100 MHz.	EIA-568-A.
Return loss.	18 dB minimum from 0.5 to 40 MHz. 12 - 20 X log (F/80) dB minimum from 40.1 to 100 MHz.	EIA-568-A.
Common Mode Rejection Ratio (CMRR).	30 dB minimum, 1 to 50 MHz. 17 dB minimum, 50.1 to 100 MHz.	Procedure details appear in test report EMEB048380-005.
Functional test: PoE.	All PoE electronics shall function properly.	Verify PoE functions using PowerDsine/Microsemi integrated PoE test equipment.
Functional test: LEDs.	All LEDs shall illuminate.	Using a current limiting power supply, apply 5 volts in both directions to all LEDs.
MECHANICAL		
Vibration, random.	Monitor for discontinuities. See Note.	EIA-364-28, Test Condition VII, Condition D. Subject mated specimens to 3.10 G's rms between 20-500 Hz. Fifteen minutes in each of 3 mutually perpendicular planes. Loopback contacts on plug side. No loopback needed on PCB side. See Figure 4.

Figure 1 (continued)

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Test Description	Requirement	Procedure
Durability.	See Note.	EIA-364-9. Mate and unmate specimens with the plug locking tab inoperable for 500 cycles at a maximum rate of 600 cycles per hour.
Mechanical shock.	Monitor for discontinuities. See Note.	EIA-364-27, Condition H. Subject mated specimens to 30 G's half-sine shock pulses of 11 milliseconds duration. Three shocks in each direction applied along 3 mutually perpendicular planes, 18 total shocks. Loopback contacts on plug side. No loopback needed on PCB side. See Figure 4.
Mating force.	20.02 N [4.5 lbf] maximum. See Note.	EIA-364-13. Measure force necessary to mate specimens at a maximum rate of 12.7 mm [0.5 in] per minute.
Unmating force.	20.02 N [4.5 lbf] maximum. See Note.	EIA-364-13. Measure force necessary to unmate specimens with the plug locking tab inoperable at a maximum rate of 12.7 mm [0.5 in] per minute.
Plug retention in jack.	35.59 N [8 lbf] minimum. Show no evidence of physical damage to the jack, plug shall not disengage from the jack.	EIA-364-98. Subject specimens to specified force applied for 1 minute in 4 directions with plug mated in jack and latch engaged, plus axial pull. See Figure 6.
Press fit insertion force.	6668 N [1500 lbf] maximum.	Measure force necessary to press connector assembly onto printed circuit board into proper seating location. See Figure 6.
Press fit extraction force.	445 N [100 lbf] minimum.	Measure force necessary to extract connector assembly from printed circuit board. See Figure 6.
ENVIRONMENTAL		
Thermal shock.	See Note.	EIA-364-32. Subject mated specimens to 5 cycles between -40 and 85 +3/-0˚C with 60 minute dwell at temperature extremes.
Humidity/temperature cycling.	See Note.	EIA-364-31, Method IV. Subject mated specimens to 10 cycles (10 days) between 25 and 65˚C at 80 to 100% RH.

Figure 1 (continued)

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Test Description	Requirement	Procedure
Temperature life.	See Note.	EIA-364-17, Method A, Test Condition 2, Test Time Condition C. Subject mated specimens to 85˚C for 500 hours.
Mixed flowing gas.	See Note.	EIA-364-65, Class IIA. Subject mated specimens to environmental Class IIA for 14 days.
Electrical performance at temperature extremes.	Meets Insertion Loss (IL) and OCL, requirements for part.	Measure at 0 and 50 ± 5˚C for standard parts.

NOTE *Shall meet visual requirements, show no physical damage, and meet requirements of additional tests as specified in the Product Qualification and Requalification Test Sequence shown in Figure 2.*

Figure 1 (end)

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3.6 Qualification Tests and Sequences

Test or Examination	Test Groups (a)							
	1(g)	2(g)	3(g)	4(b,g)	5(b,g)	6(b,g)	7(f)	8(b,g)
	Test Sequence (c)							
Initial examination of product	1	1	1	1	1	1	1	1
LLCR, RJ45 interface, cable and board side	5,9	3,5	3,5					
OCL, cable side	2,12(e)(f)			3,9				2,5
Insulation resistance				4,7				
Withstanding voltage				8(f)				
NEXT						2		
Insertion loss	13(e)(f)			2,10		3		3,6
Return loss						4		
CMRR						5		
Functional test: PoE			7(h)					
Functional test: LEDs	3,11(I)	2,6(I)	2,6(I)					
Vibration, random	7							
Durability	6				2			
Mechanical shock	8							
Mating force	4							
Unmating force	10							
Plug retention in jack							3	
Press fit insertion force							2	
Press fit extraction force							4	
Thermal shock				5				
Humidity/temperature cycling				6				
Temperature life		4(d)						4(d)
Mixed flowing gas			4(d)					
Electrical performance at temperature extremes					3			
Final examination of product	14	7	8	11	4	6	5	7

NOTE

(a) See paragraph 4.1.A.
(b) Test Groups are performed with parts NOT mounted to qualification test boards for entire test group.
(c) Numbers indicate sequence in which tests are performed.
(d) Precondition specimens with 10 durability cycles.
(e) Parts to be measured before insertion onto PCB and/or after removal from PCB. Vertical header contact to be probed not soldered.
(f) Test Groups to be performed with all 12 ports populated with cable plug. See Figure 3.
(g) Test Groups to be performed with only ports 0, 1, 5, 6, 10 and 11 populated with cable plugs. See Figure 3.
(h) PoE functional test to be performed with PowerDsine/Microsemi Integrated PoE test equipment. Part must be removed from PCB.
(I) LED functional test to be performed with current-limiting power supply. Verify illumination on both LED's, both directions, all ports.

Figure 2

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4 QUALITY ASSURANCE PROVISIONS

4.1. Qualification Testing

A. Specimen Selection

Modular plug and jack test specimens shall be selected at random from current production lots and prepared for testing in accordance with current Application Specifications and Instructions Sheets. Test groups 1, 2, 3, 5, 6 and 8 shall each consist of 4 specimens. Test group 4 shall consist of 3 specimens. Test group 7 shall consist of 1 specimen.

B. Test Sequence

Qualification inspection shall be verified by testing as specified in Figure 2.

4.2. Re-qualification Testing

If changes significantly affecting form, fit, or function are made to the product or manufacturing process, product assurance shall coordinate re-qualification testing, consisting of all or part of the original testing sequences as determined by development/product, quality and reliability engineering.

4.3. Acceptance

Acceptance is based on verification that the product meets the requirements of Figure 1. Failures attributed to equipment, test setup or operator deficiencies shall not disqualify the product. If the product failure occurs, corrective action shall be taken and specimens resubmitted for qualification. Testing to confirm corrective action is required before re-submittal.

4.4. Quality Conformance Inspection

The applicable quality inspection plan shall specify the sampling acceptable quality level to be used. Dimensional and functional requirements shall be in accordance with the applicable product drawing and this specification.

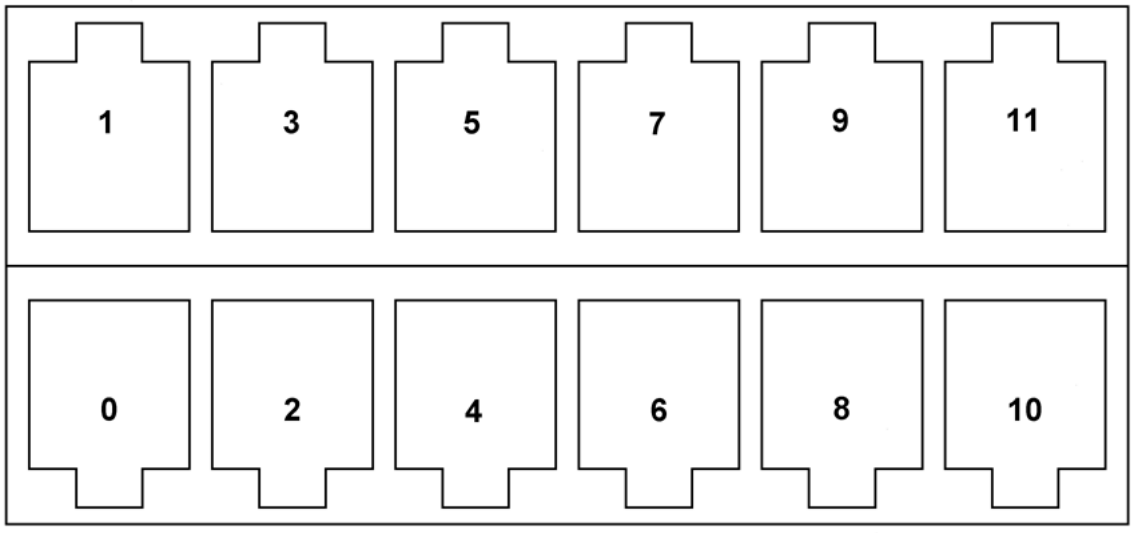

Figure 3
Port Designation
Front View of RJ45 Connector

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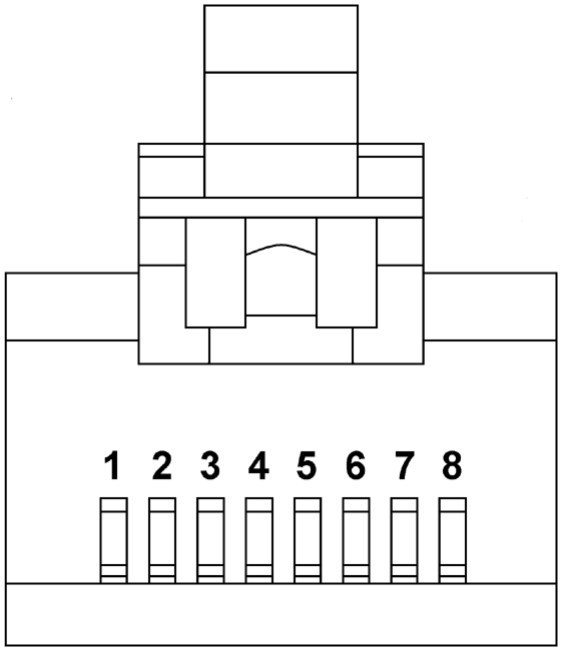
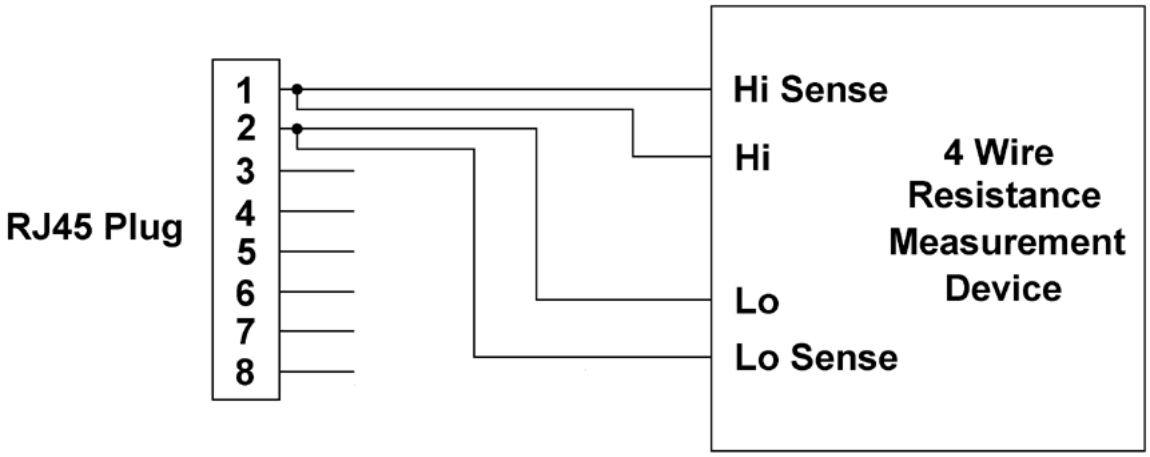


Figure 4
Front View RJ45 Plug
Data Pairs 1-2, 3-6, 4-5 and 7-8
Cable Side LLCR, OCL and Discontinuity



NOTE

1. *Diagram shows connections for Pins 1 and 2.*
2. *Measurement is repeated across the following signal pairs: Pins 1-2, Pins 3-6, Pins 4-5 and Pins 7-8.*

Figure 5
Cable Side LLCR and Discontinuity Measurement Setup

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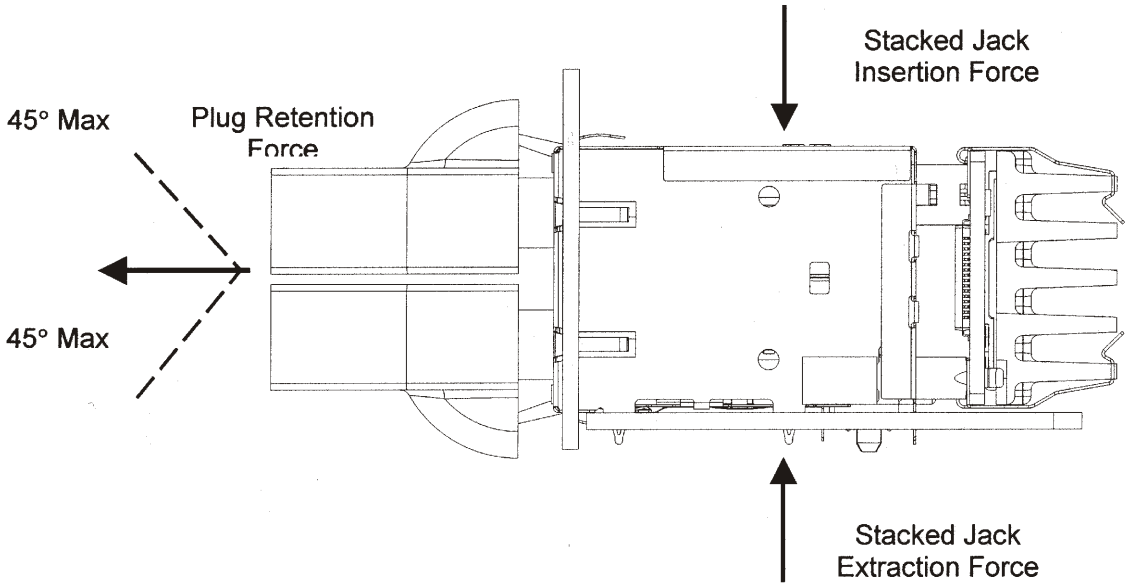

Figure 6
Plug Mating, Unmating and Retention Forces
Jack Insertion and Extraction Forces

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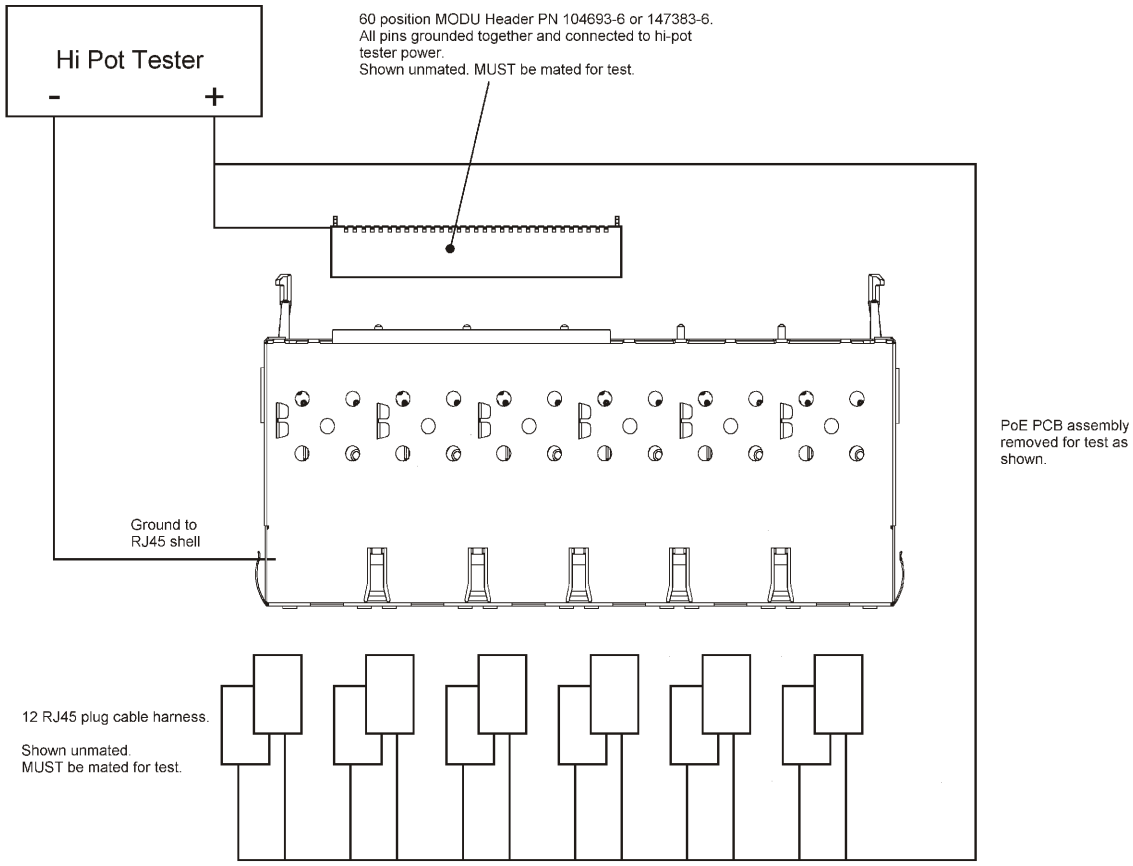

Figure 7
Dielectric Withstanding Voltage Test Setup

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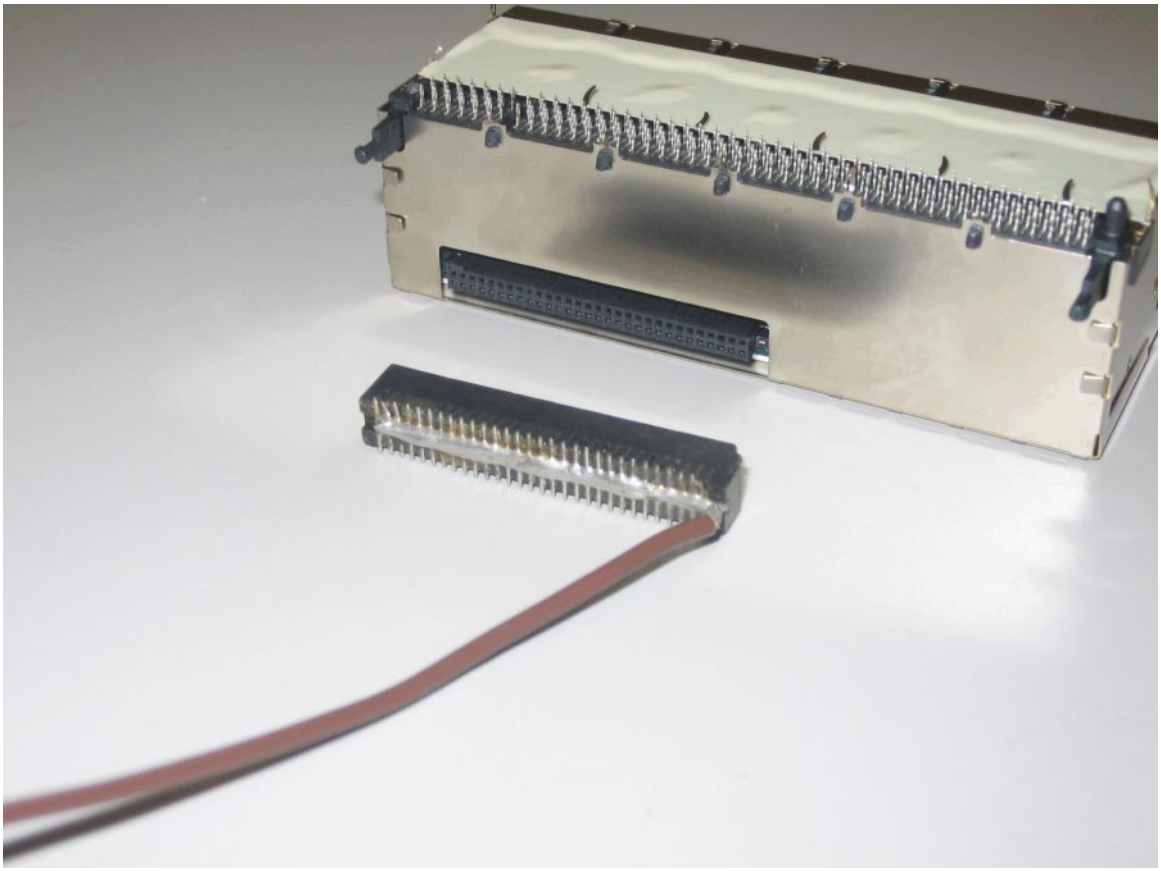

Figure 8
Dielectric Withstanding Voltage Test Setup
PoE Board Header, All Pins Grounded Together

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