

# BLF7G27L-200PB

Power LDMOS transistor

Rev. 2 — 20 February 2012

Product data sheet

## 1. Product profile

### 1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 2600 MHz to 2700 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.

Mode of operation	f (MHz)	$I_{Dq}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR (dBc)
2-carrier W-CDMA	2620 to 2690	1700	32	65	16.5	29	-30 <sup>[1]</sup>

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low  $R_{th}$  providing excellent thermal stability
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

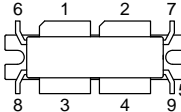
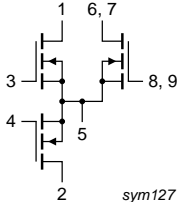
### 1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2600 MHz to 2700 MHz frequency range



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
6, 7	sense drain		
8, 9	sense gate		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLF7G27L-200PB	-	flanged LDMOST ceramic package; 2 mounting holes; 8 leads	SOT1110A

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$ ; $P_L = 65\text{ W}$ ; $V_{DS} = 32\text{ V}$ ; $I_{Dq} = 1700\text{ mA}$	0.22	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ }^\circ\text{C}$  per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.44\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	-	28	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.2\text{ A}$	-	10.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 5.04\text{ A}$	-	0.1	-	$\Omega$
$I_{Dq}$	quiescent drain current	main transistor: $V_{DS} = 32\text{ V}$ sense transistor: $I_{DS} = 31\text{ mA}$ $V_{DS} = 30.1\text{ V}$	1530	1700	1870	mA

## 7. Test information

**Remark:** All testing performed in a class-AB production test circuit.

**Table 7. Functional test information**

Mode of operation: 2-carrier W-CDMA, PAR = 8.4 dB at 0.01 % probability on the CCDF, 3GPP test model 1; 1-64 DPCH;  $f_1 = 2622.5\text{ MHz}; f_2 = 2627.5\text{ MHz}; f_3 = 2682.5\text{ MHz}; f_4 = 2687.5\text{ MHz};$  RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 1700\text{ mA}; T_{case} = 25\text{ }^\circ\text{C};$  unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	65	-	W
$G_p$	power gain		14.8	16.5	17.7	dB
$RL_{in}$	input return loss		-	-15	-5	dB
$\eta_D$	drain efficiency		25.5	29	-	%
ACPR	adjacent channel power ratio		-	-30	-27	dBc

### 7.1 Ruggedness in class-AB operation

The BLF7G27L-200PB is capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 32\text{ V}; I_{Dq} = 1700\text{ mA}; P_L = 200\text{ W (CW)}; f = 2600\text{ MHz}.$

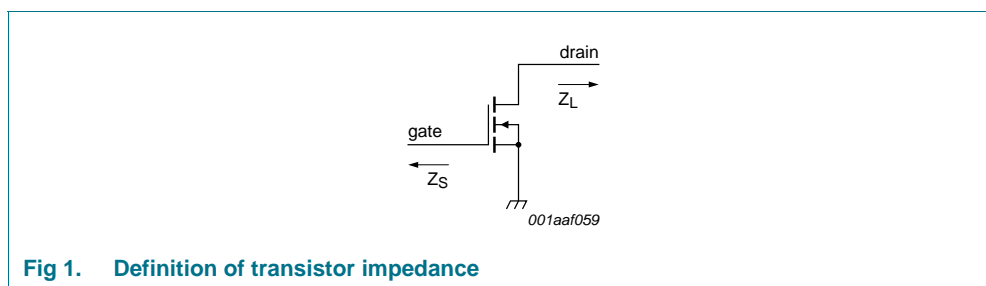
## 7.2 Impedance information

**Table 8. Typical impedance**

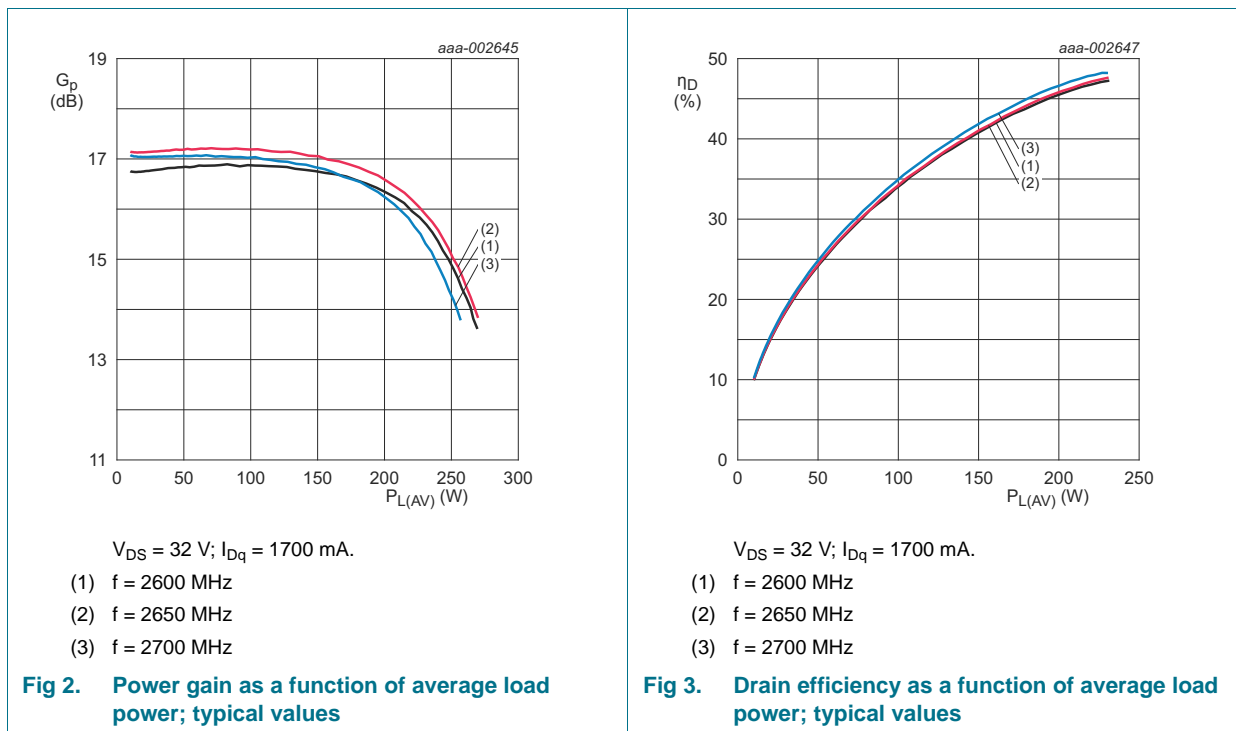
Measured load-pull data half device;  $I_{Dq} = 850 \text{ mA}$ ;  $V_{DS} = 32 \text{ V}$ .

f (MHz)	$Z_S$ <sup>[1]</sup> ( $\Omega$ )	$Z_L$ <sup>[1]</sup> ( $\Omega$ )
2500	3.07 – j3.51	2.79 – j4.86
2600	4.51 – j12.51	2.61 – j4.49
2700	7.56 – j15.0	2.36 – j4.41

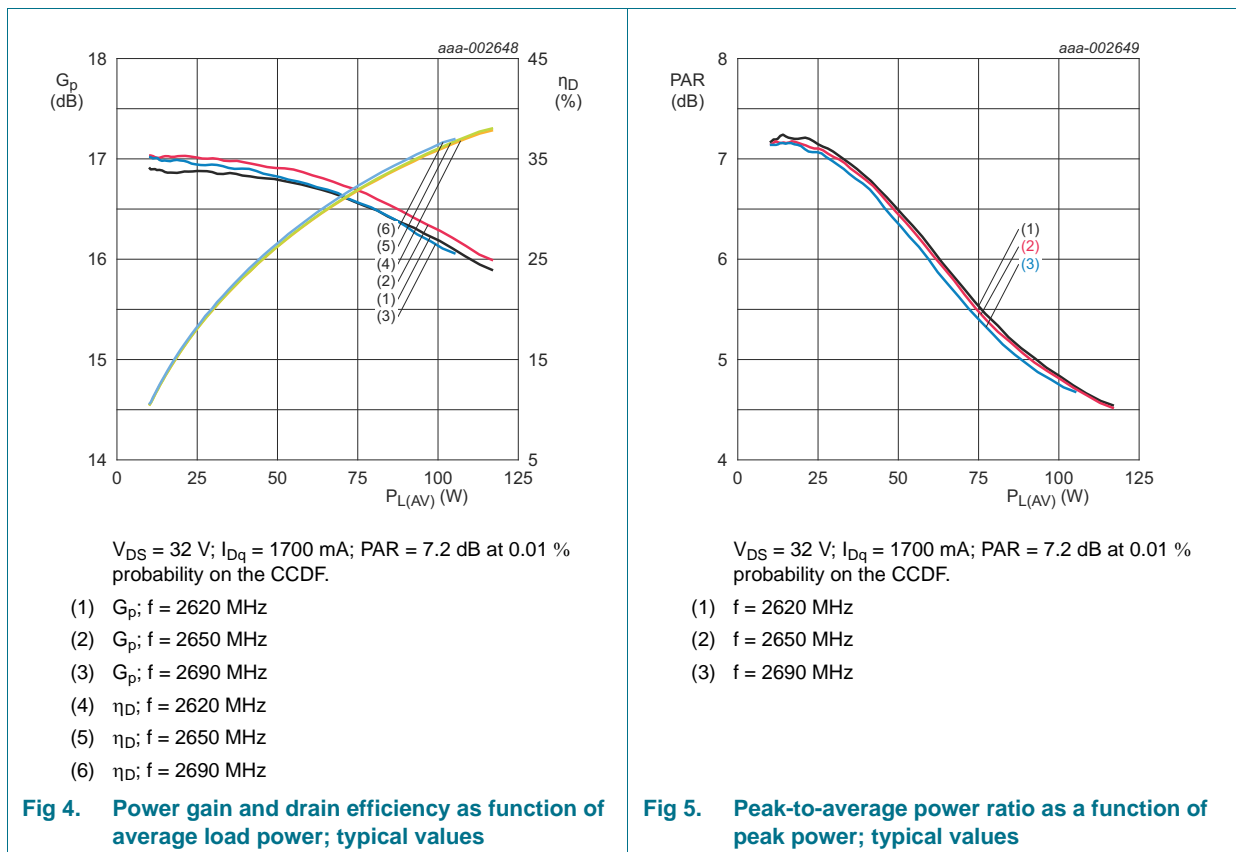
[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).



## 7.3 1 Tone CW



**7.4 1-carrier W-CDMA**

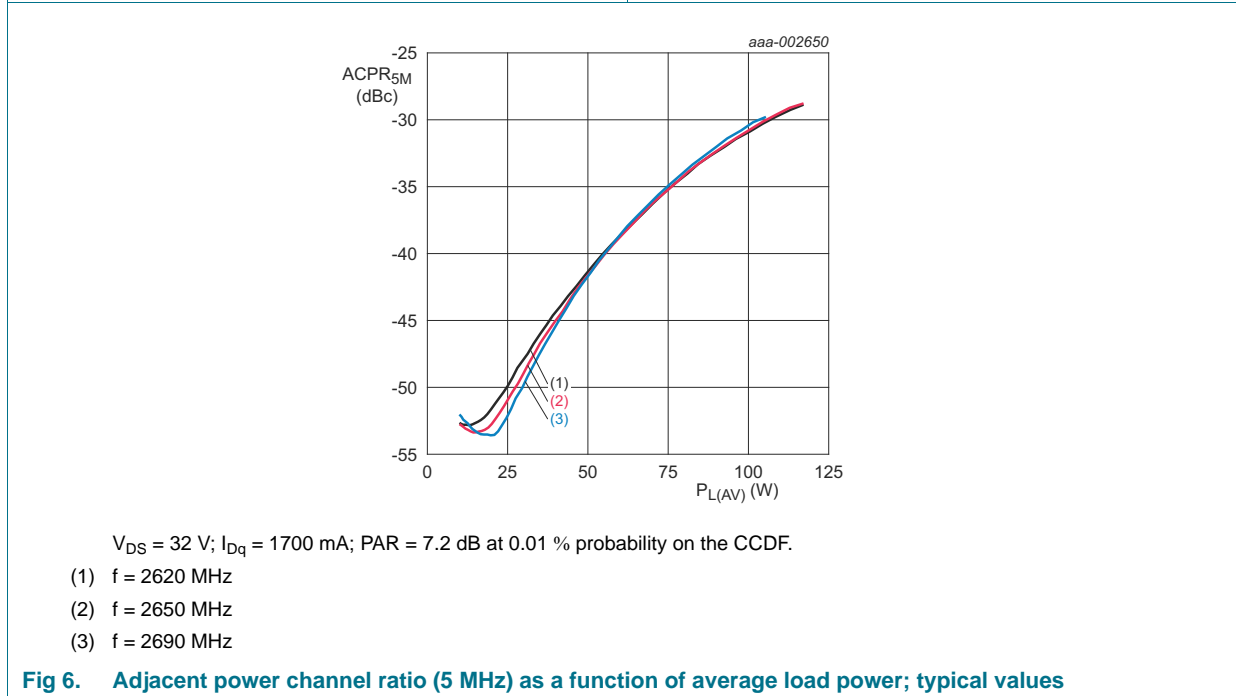


$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1700\text{ mA}$ ; PAR = 7.2 dB at 0.01 % probability on the CCDF.

- (1)  $G_p$ ; f = 2620 MHz
- (2)  $G_p$ ; f = 2650 MHz
- (3)  $G_p$ ; f = 2690 MHz
- (4)  $\eta_D$ ; f = 2620 MHz
- (5)  $\eta_D$ ; f = 2650 MHz
- (6)  $\eta_D$ ; f = 2690 MHz

$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1700\text{ mA}$ ; PAR = 7.2 dB at 0.01 % probability on the CCDF.

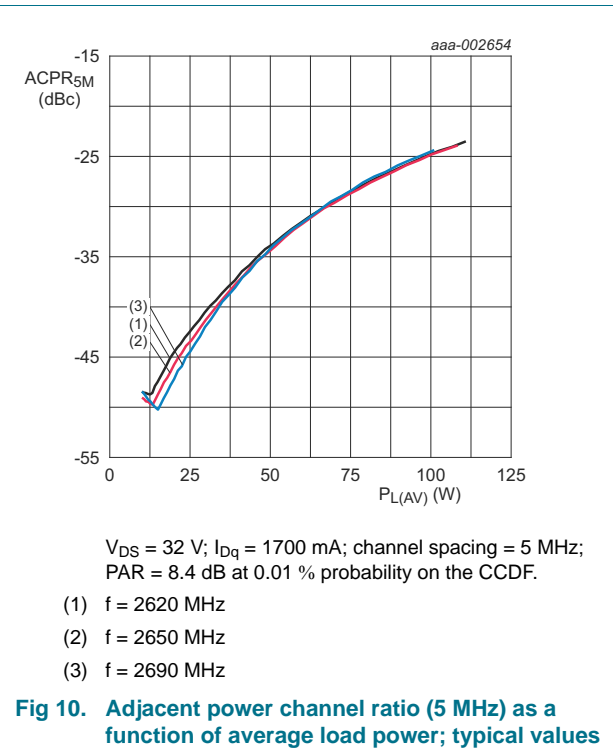
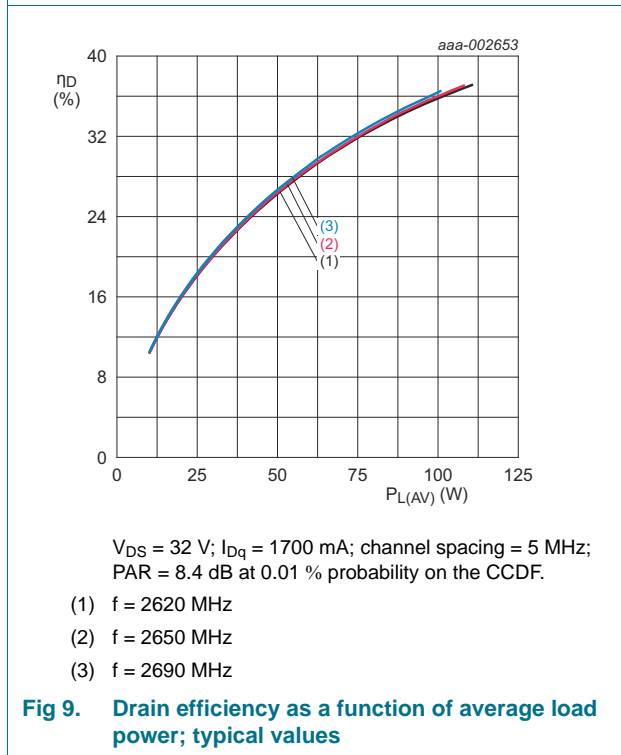
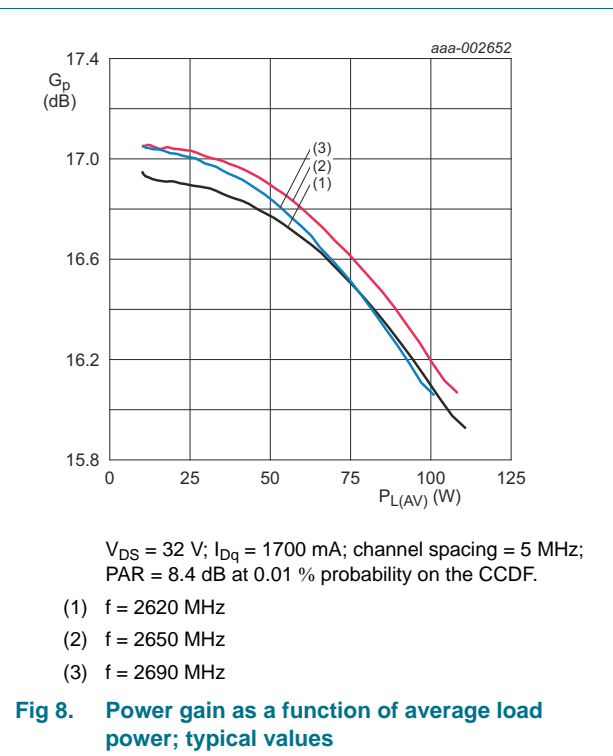
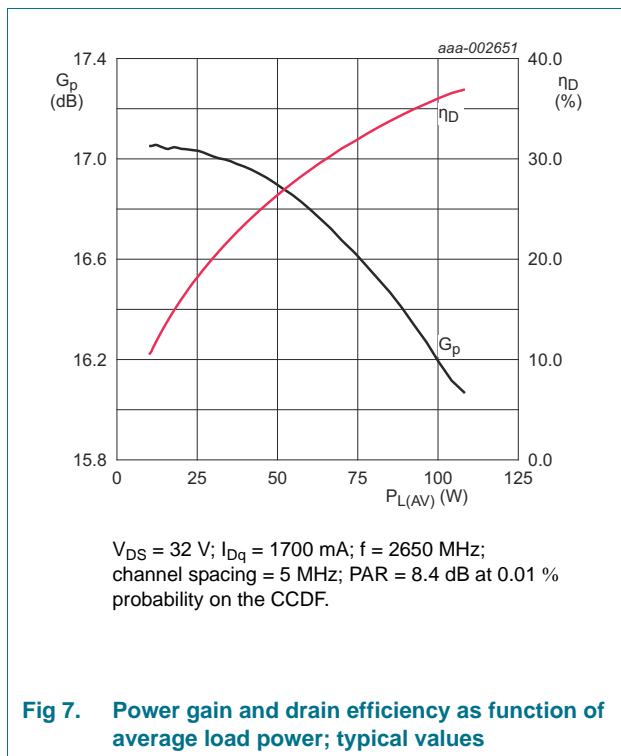
- (1) f = 2620 MHz
- (2) f = 2650 MHz
- (3) f = 2690 MHz



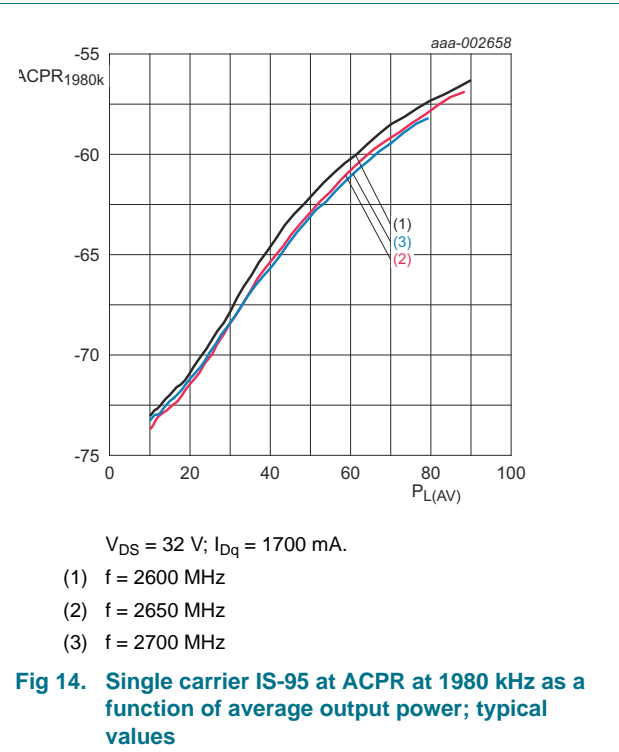
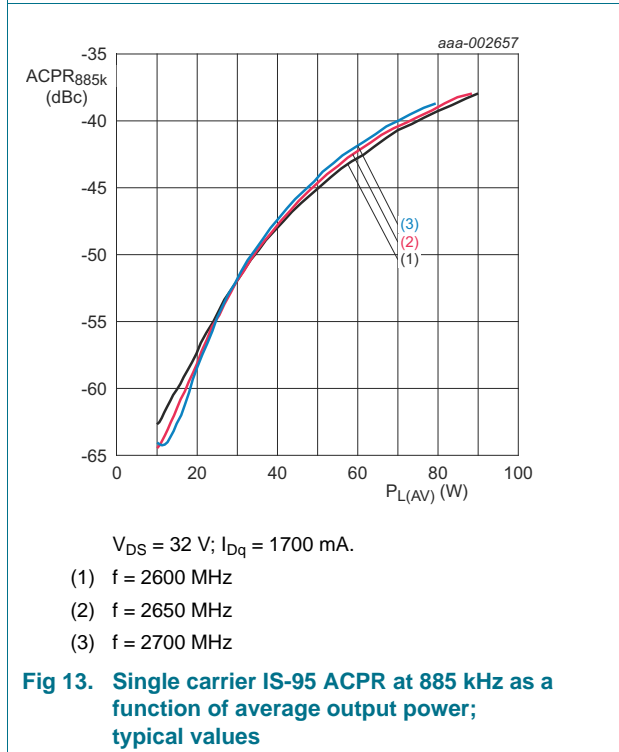
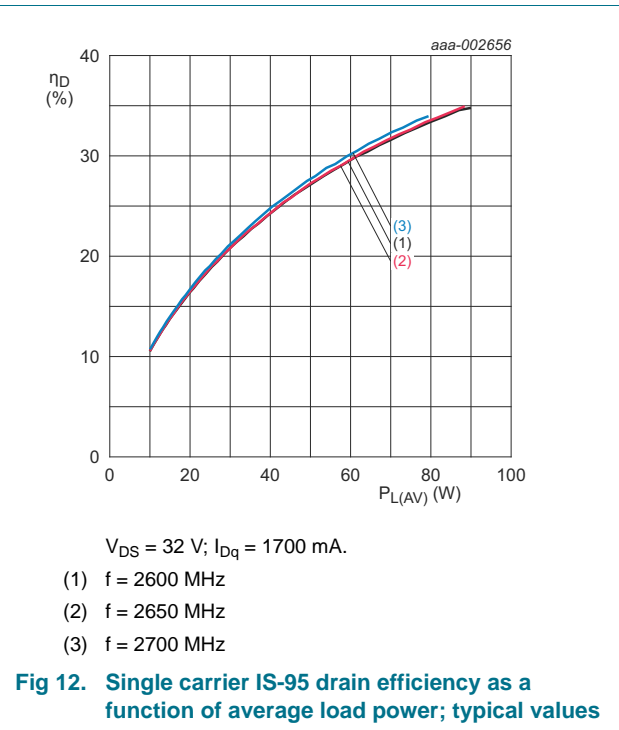
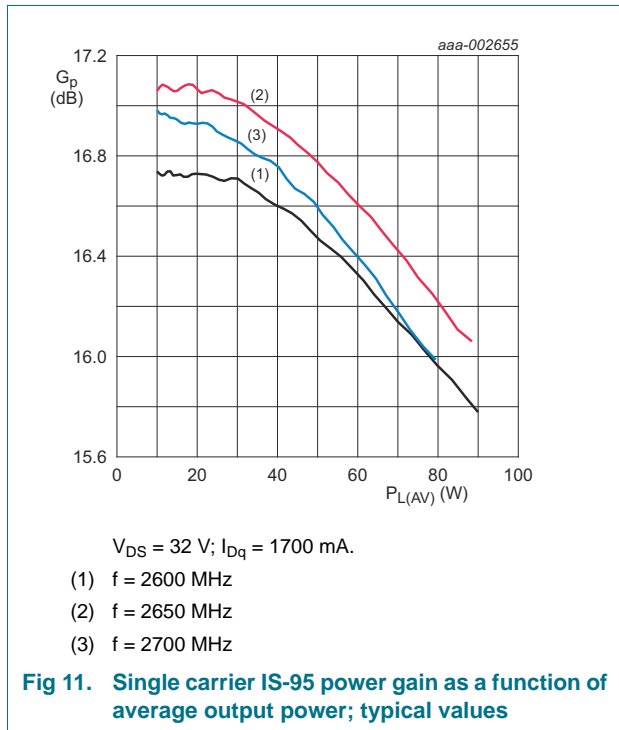
$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1700\text{ mA}$ ; PAR = 7.2 dB at 0.01 % probability on the CCDF.

- (1) f = 2620 MHz
- (2) f = 2650 MHz
- (3) f = 2690 MHz

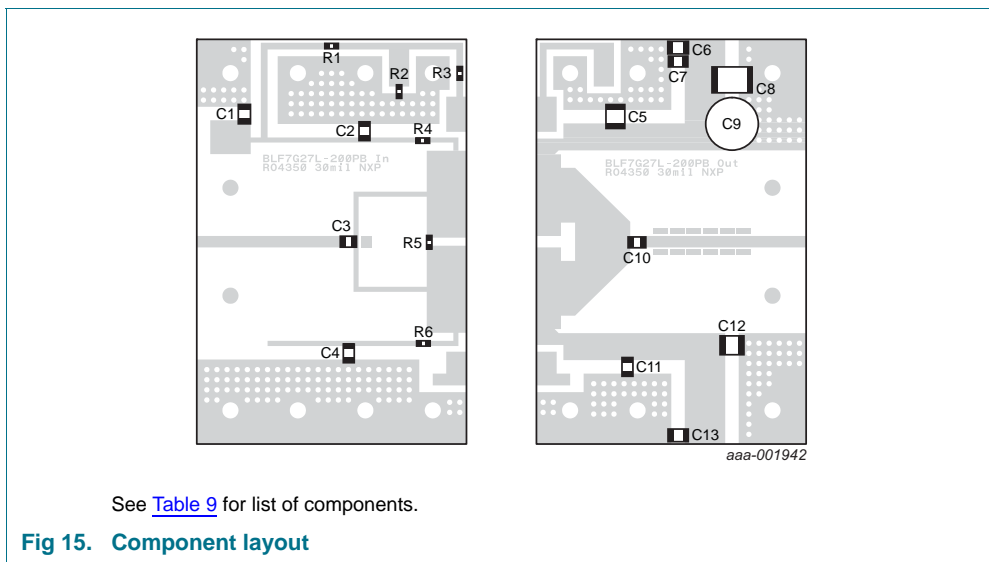
7.5 2-carrier W-CDMA



7.6 IS-95



**7.7 Test circuit**



**Table 9. List of components**

See [Figure 15](#) for component layout.

The used PCB material is Rogers RO4350B with a thickness of 0.76 mm.

Component	Description	Value	Remarks
C1, C6, C13	multilayer ceramic chip capacitor	4.7 $\mu$ F	[1] Murata
C2, C4	multilayer ceramic chip capacitor	9.1 pF	[2] ATC100B
C3	multilayer ceramic chip capacitor	22 pF	[3] ATC100A
C5, C10, C11	multilayer ceramic chip capacitor	8.2 pF	[2] ATC100B
C7	multilayer ceramic chip capacitor	470 nF	[4] AVX
C8, C12	multilayer ceramic chip capacitor	10 $\mu$ F	[5] TDK
C9	electrolytic capacitor	470 $\mu$ F	
R1	chip resistor	820 $\Omega$	[6] Philips 0603
R2	chip resistor	2K2 $\Omega$	[6] Philips 0603
R3	chip resistor	22 $\Omega$	[6] Philips 0603
R4, R6	chip resistor	10 $\Omega$	[6] Philips 0603
R5	chip resistor	33 $\Omega$	[6] Philips 0603

[1] Murata or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 100A or capacitor of same quality.

[4] AVX or capacitor of same quality.

[5] TDK or capacitor of same quality.

[6] Philips or resistor of same quality.



## 8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 8 leads

SOT1110A

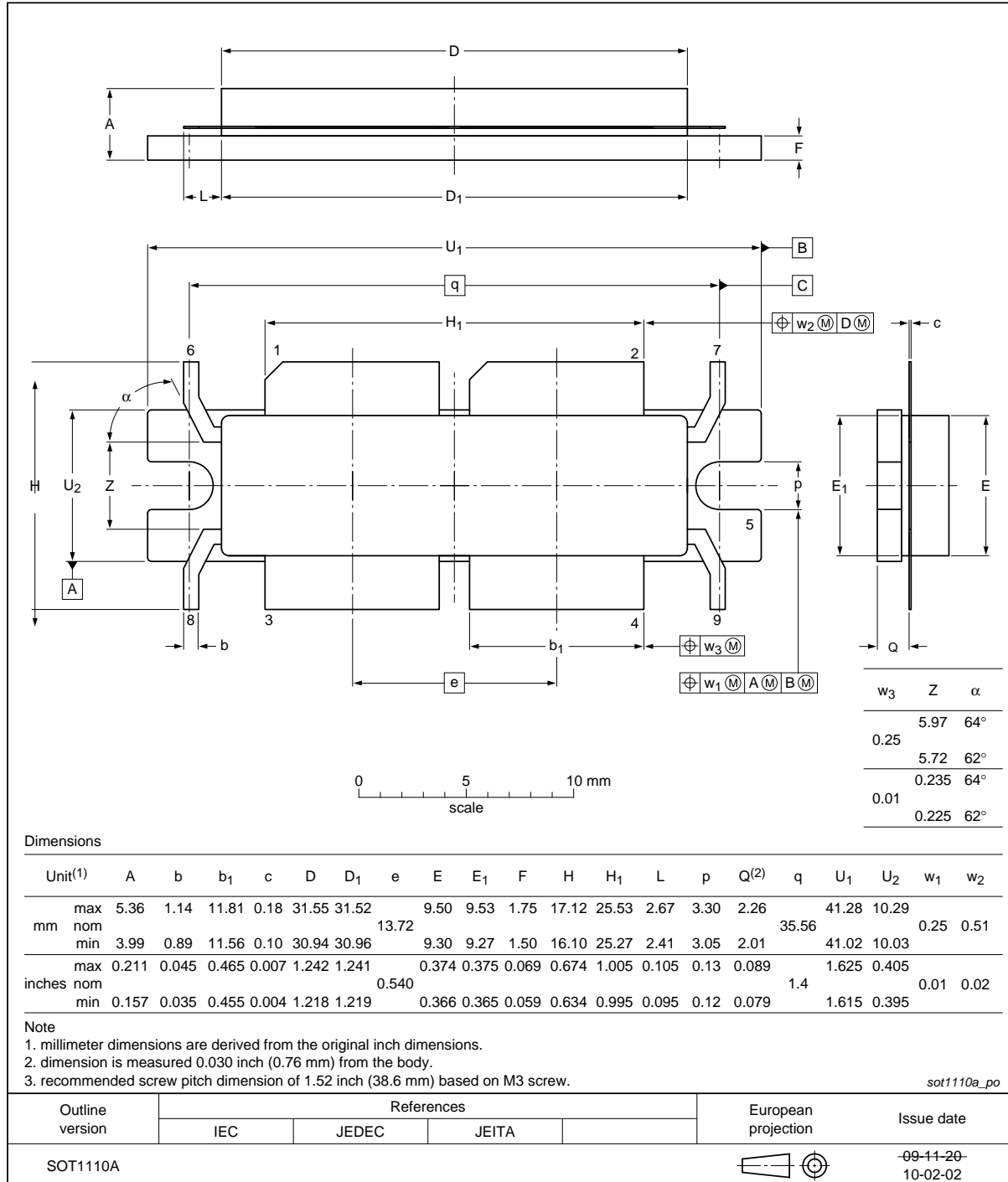


Fig 16. Package outline SOT1110A

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G27L-200PB v.2	20120220	Product data sheet	-	BLF7G27L-200PB_27LS-200PB v.1
Modifications: <ul style="list-style-type: none"> <li>• This document now only describes the BLF7G27L-200PB product.</li> <li>• <a href="#">Table 1 on page 1</a>: Some changes have been made.</li> <li>• <a href="#">Section 1.2 on page 1</a>: Some changes have been made.</li> <li>• <a href="#">Section 1.3 on page 1</a>: Some changes have been made.</li> <li>• <a href="#">Table 4 on page 2</a>: The line specifying <math>I_D</math> has been removed from the table.</li> <li>• <a href="#">Table 5 on page 2</a>: Some changes have been made.</li> <li>• <a href="#">Table 6 on page 3</a>: Some changes have been made.</li> <li>• <a href="#">Table 7 on page 3</a>: Some changes have been made.</li> <li>• <a href="#">Section 7.1 on page 3</a>: Some changes have been made.</li> <li>• <a href="#">Table 8 on page 4</a>: Some changes have been made</li> <li>• <a href="#">Section 7.2 on page 4</a>: Section has been added.</li> <li>• <a href="#">Section 7.3 on page 4</a>: Section has been added.</li> <li>• <a href="#">Section 7.4 on page 5</a>: Section has been added.</li> <li>• <a href="#">Section 7.5 on page 6</a>: Section has been added.</li> <li>• <a href="#">Section 7.6 on page 7</a>: Section has been added.</li> <li>• <a href="#">Section 7.7 on page 8</a>: Section has been added.</li> </ul>				
BLF7G27L-200PB_27LS-200PB v.1	20110405	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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