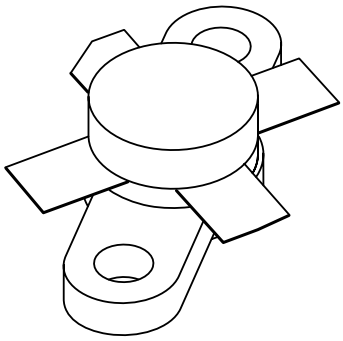
DATA SHEET



BLF244
VHF power MOS transistor

Product specification
Supersedes data of 1997 Dec 17

2003 Oct 13

Philips
Semiconductors

PHILIPS

VHF power MOS transistor BLF244

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123A flange package, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PIN CONFIGURATION

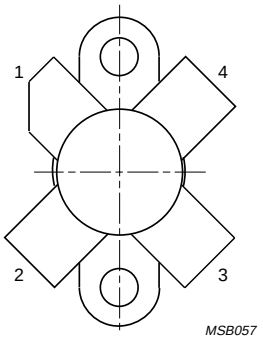


Fig.1 Simplified outline and symbol.

PINNING - SOT123A

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	15	>13	>50

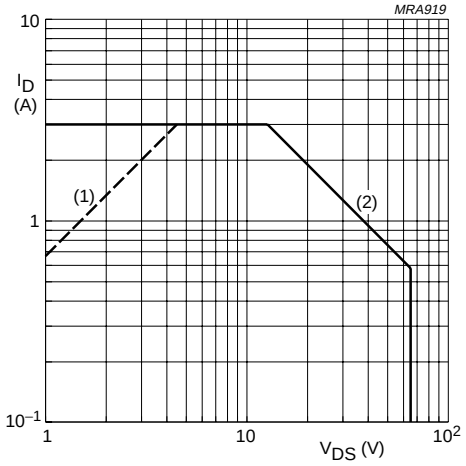
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	3	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	38	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

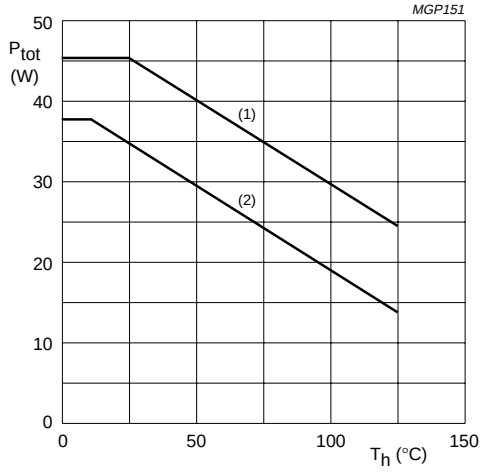
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 38 W	4.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 38 W	0.3	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power derating curves.

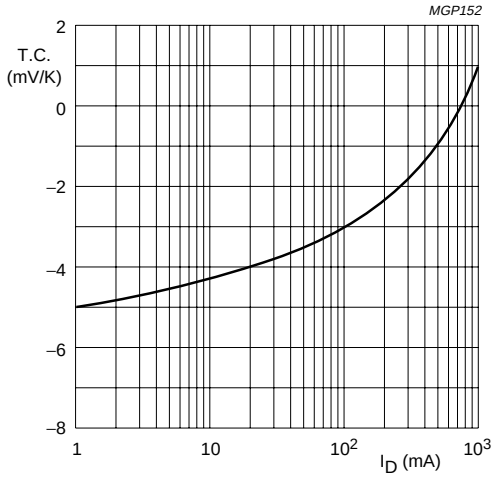
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 5 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	0.6	–	–	S
R_{DSon}	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	–	pF
F	noise figure; see Fig.13	I_D = 0.5 A; V_{DS} = 28 V; R1 = 23 Ω; T_h = 25 °C; f = 175 MHz; $R_{th\ mb\text{-}h}$ = 0.3 K/W	–	4.3	–	dB

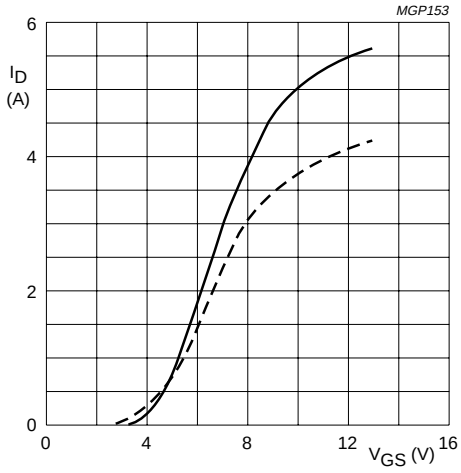
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



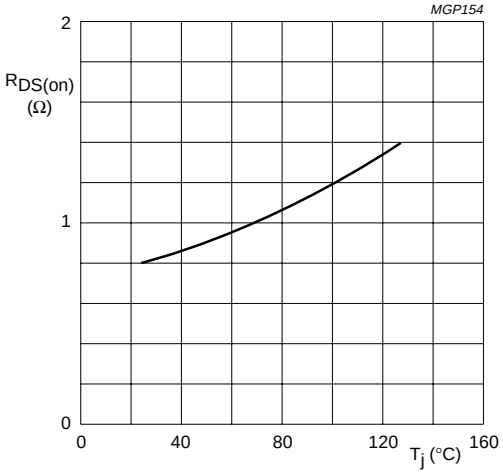
V_{DS} = 10 V; valid for T_j = 25 to 125 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



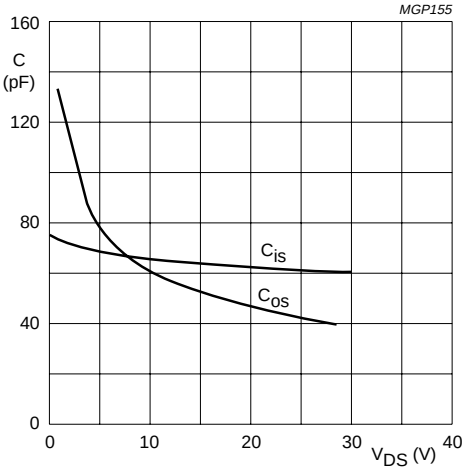
V_{DS} = 10 V.
solid line: T_j = 25 °C.
dotted line: T_j = 125 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



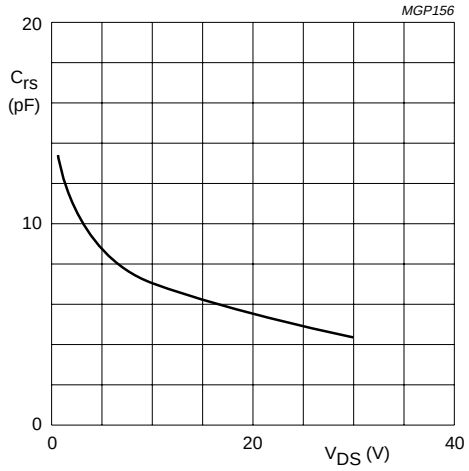
V_{GS} = 10 V; I_D = 0.75 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 3 K/W; unless otherwise specified.
RF performance in CW operation in a common source class-B circuit.

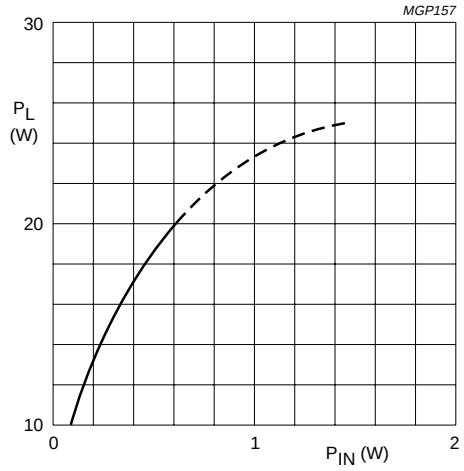
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	Z_i (Ω)[1]	Z_L (Ω)	R1 (Ω)
CW, class-B	175	28	25	15	>13 typ. 17	>50 typ. 65	3.0 – j4.0	6.3 + j9.8	46.4//46.4
	175	12.5	25	6	typ. 15	typ. 60	3.0 – j4.0	4.5 + j3.3	100

Note

1. R1 included.

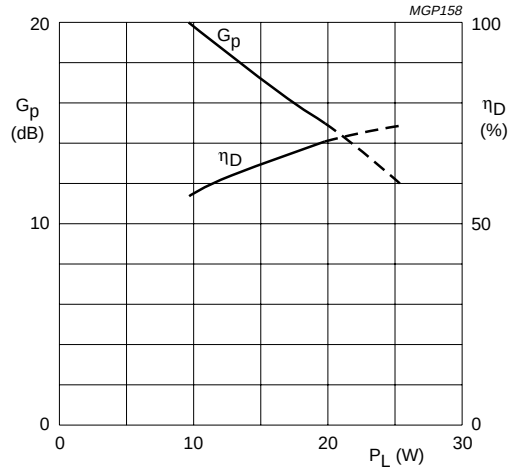
Ruggedness in class-B operation

The BLF244 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions: T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; at rated load power.



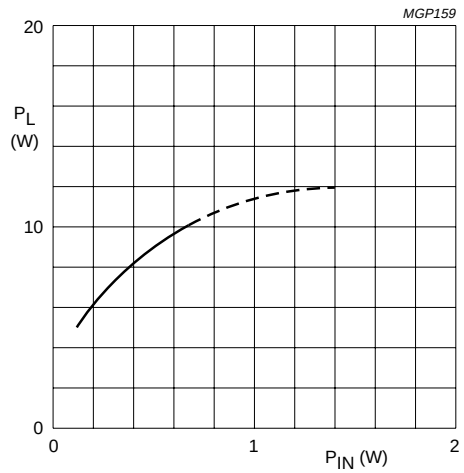
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.9 Load power as a function of input power; typical values.



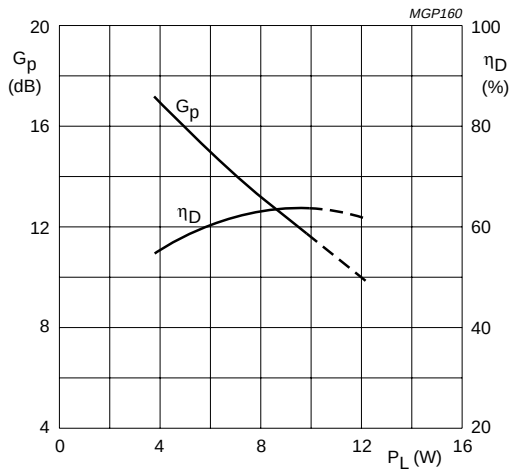
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.10 Power gain and efficiency as functions of load power; typical values.



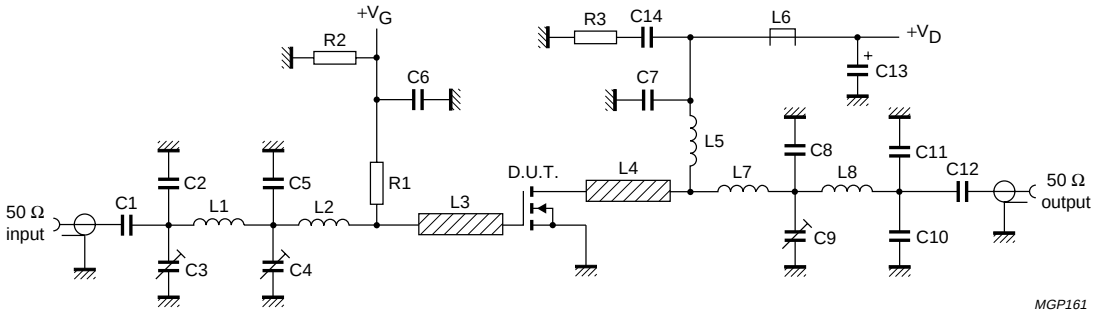
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.11 Load power as a function of input power; typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.12 Power gain and efficiency as functions of load power; typical values.



f = 175 MHz.

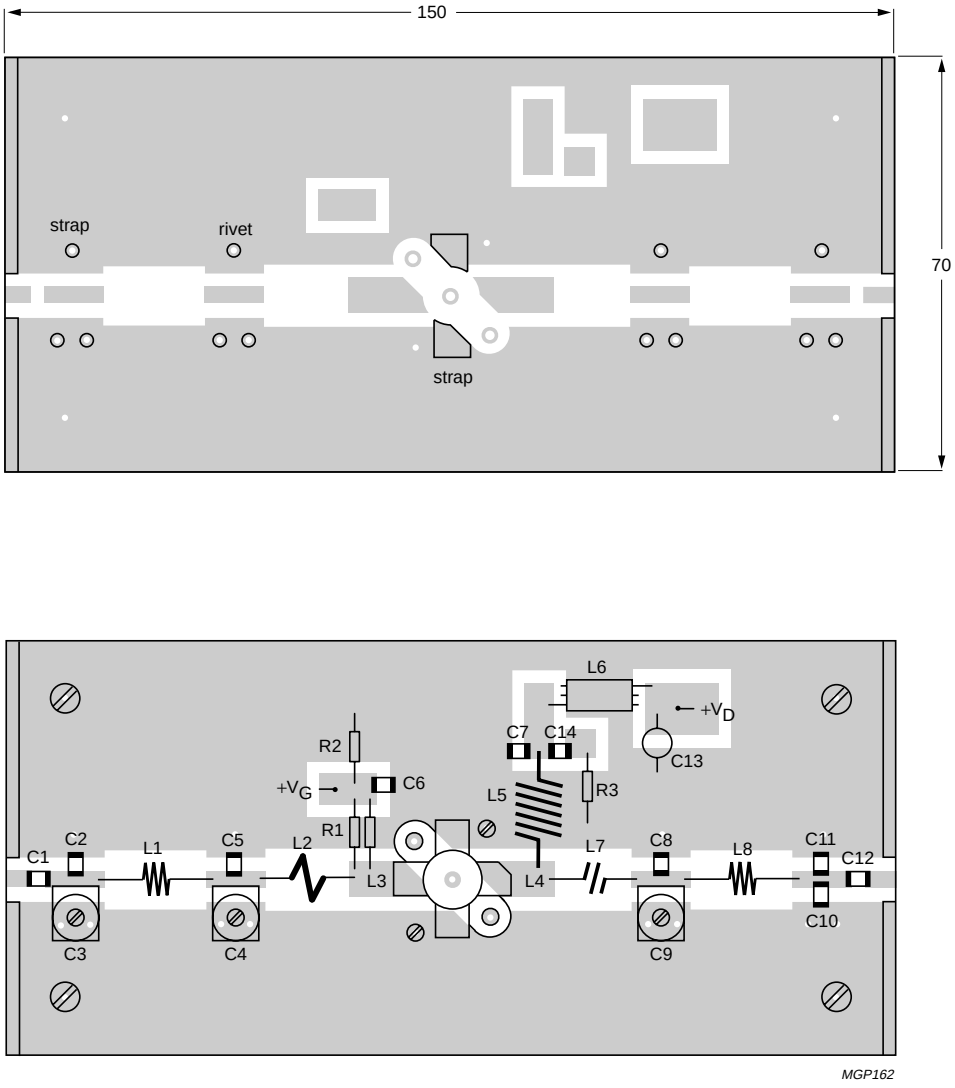
Fig.13 Test circuit for class-B operation.

List of components (see Fig.13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C12	multilayer ceramic chip capacitor; note 1	680 nF		
C2	multilayer ceramic chip capacitor; note 1	20 pF		
C3, C4, C9	film dielectric trimmer	5 to 60 pF		2222 809 08003
C5	multilayer ceramic chip capacitor; note 1	75 pF		
C6	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor; note 1	100 pF		
C8	multilayer ceramic chip capacitor; note 1	47 pF		
C10, C11	multilayer ceramic chip capacitor; note 1	11 pF		
C13	solid tantalum capacitor	2.2 μF		
C14	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	4 turns enamelled 1 mm copper wire	32 nH	length 6.3 mm int. dia. 3 mm leads 2 × 5 mm	
L2	1 turn enamelled 1 mm copper wire	12.2 nH	int. dia. 5.6 mm leads 2 × 5 mm	
L3, L4	stripline; note 2	30 Ω	15 × 6 mm	
L5	6 turns enamelled 1 mm copper wire	119 nH	length 10.4 mm int. dia. 6 mm leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
L7	2 turns enamelled 1 mm copper wire	19 nH	length 2.4 mm int. dia. 3 mm leads 2 × 5 mm	
L8	4 turns enamelled 1 mm copper wire	28.5 nH	length 8.5 mm int. dia. 3 mm leads 2 × 5 mm	
R1	metal film resistor; note 3			
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

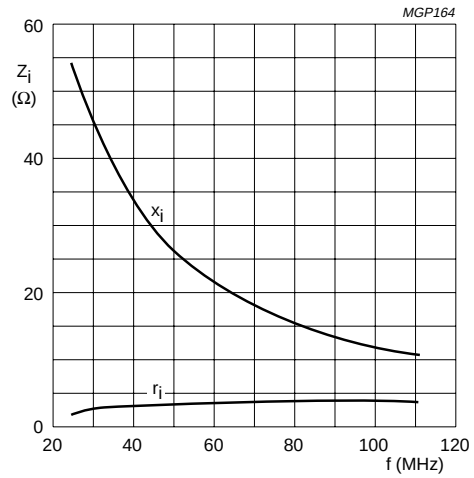
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5), thickness $\frac{1}{16}$ inch.
3. Refer to Application Information for value.



Dimensions in mm.

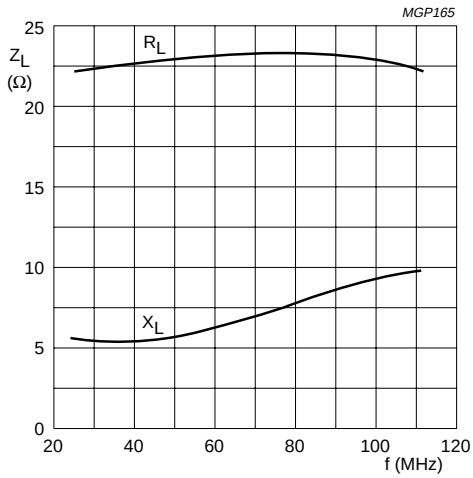
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being unetched copper to serve as ground plane. Earth connections are made by fixing screws, copper straps and hollow rivets under the sources and around the edges to provide a direct contact between the copper on the component side and the ground plane.

Fig.14 Component layout for 175 MHz class-B test circuit.



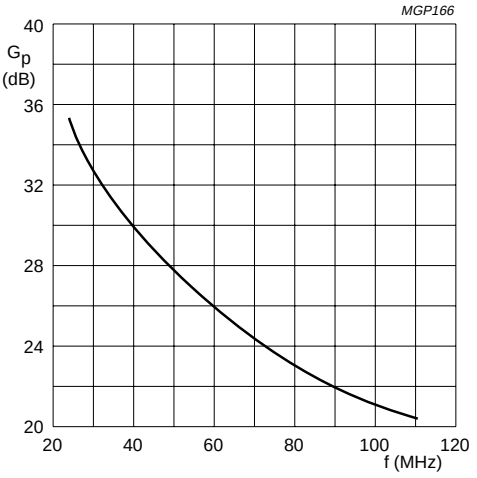
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.15 Input impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.16 Load impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.17 Power gain as function of frequency; typical values.

BLF244 scattering parameters

V_{DS} = 12.5 V; I_D = 25 mA; note 1

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\|s_{11}\|$	$\angle\Phi$	$\|s_{21}\|$	$\angle\Phi$	$\|s_{12}\|$	$\angle\Phi$	$\|s_{22}\|$	$\angle\Phi$
5	0.98	–18.6	15.11	165.1	0.02	75.8	0.98	–18.9
10	0.93	–35.0	14.06	152.3	0.04	63.1	0.95	–36.5
20	0.84	–63.4	11.55	130.0	0.06	42.1	0.86	–65.1
30	0.77	–83.3	9.20	114.5	0.07	27.3	0.80	–85.7
40	0.73	–97.6	7.41	102.8	0.07	16.5	0.76	–99.8
50	0.72	–107.9	6.09	93.7	0.07	8.5	0.74	–109.8
60	0.71	–115.7	5.09	86.2	0.07	2.0	0.74	–117.3
70	0.72	–121.4	4.32	80.1	0.07	–3.1	0.74	–123.1
80	0.72	–126.0	3.72	74.8	0.07	–7.2	0.75	–127.8
90	0.74	–130.0	3.26	70.1	0.006	–10.9	0.76	–131.9
100	0.75	–133.8	2.88	65.6	0.06	–14.3	0.78	–135.4
125	0.78	–142.0	2.16	55.5	0.05	–20.6	0.81	–142.4
150	0.81	–147.9	1.66	48.1	0.04	–22.9	0.84	–147.8
175	0.85	–152.7	1.33	42.2	0.03	–21.0	0.86	–152.4
200	0.87	–157.6	1.09	36.7	0.02	–12.8	0.88	–156.4
250	0.90	–165.1	0.75	28.8	0.01	46.1	0.92	–162.9
300	0.92	–171.5	0.56	23.8	0.03	80.9	0.94	–168.1
350	0.94	–176.8	0.42	21.4	0.04	88.3	0.95	–172.4
400	0.94	178.3	0.34	20.8	0.06	89.0	0.96	–176.2
450	0.95	174.0	0.28	21.9	0.07	88.8	0.96	–179.6
500	0.95	169.9	0.24	24.8	0.09	86.9	0.96	177.3
600	0.95	162.4	0.19	33.8	0.12	83.5	0.97	171.8
700	0.94	155.4	0.18	42.8	0.14	79.9	0.96	166.8
800	0.94	148.6	0.19	50.1	0.17	77.1	0.96	162.1
900	0.93	142.0	0.21	54.4	0.19	71.6	0.94	157.9
1000	0.92	135.5	0.23	59.6	0.22	73.5	0.93	162.9

Note

1. For more extensive s-parameters see internet:
   http://www.semiconductors.philips.com/markets/communications/wirelesscommunication/broadcast.

BLF244 scattering parameters

V_{DS} = 28 V; I_D = 25 mA; note 1

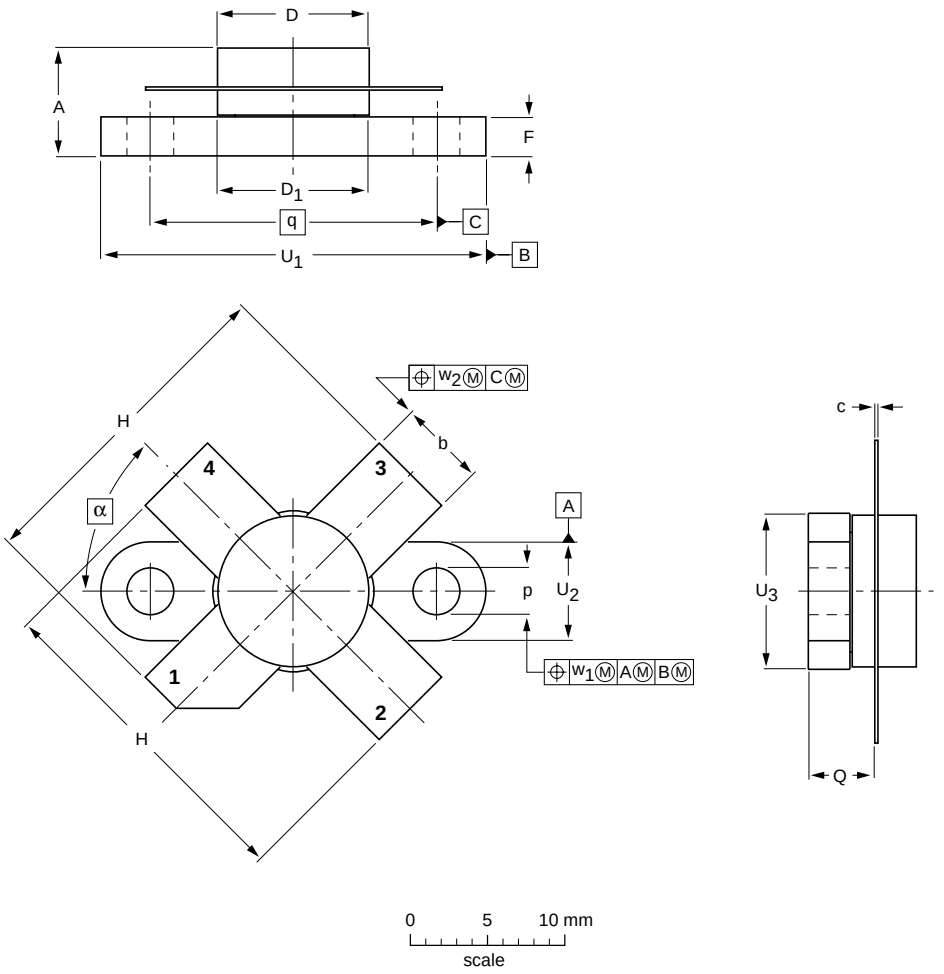
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\|s_{11}\|$	$\angle\Phi$	$\|s_{21}\|$	$\angle\Phi$	$\|s_{12}\|$	$\angle\Phi$	$\|s_{22}\|$	$\angle\Phi$
5	0.99	–15.9	15.62	167.8	0.01	78.5	0.98	–13.8
10	0.96	–30.1	14.85	157.2	0.03	68.0	0.96	–27.1
20	0.89	–56.5	12.92	137.3	0.04	49.3	0.88	–50.1
30	0.83	–76.5	10.79	122.3	0.06	35.1	0.81	–68.2
40	0.79	–91.7	8.98	110.5	0.06	24.1	0.76	–81.7
50	0.77	–103.1	7.55	101.1	0.06	15.8	0.73	–91.9
60	0.76	–111.8	6.40	93.4	0.06	9.1	0.72	–99.9
70	0.75	–118.3	5.50	87.1	0.06	3.8	0.72	–106.4
80	0.76	–123.5	4.79	81.7	0.06	–0.5	0.72	–111.8
90	0.76	–127.9	4.24	76.8	0.06	–4.3	0.73	–116.6
100	0.77	–132.0	3.77	72.2	0.06	–7.7	0.74	–120.8
125	0.79	–140.7	2.88	61.9	0.05	–14.3	0.77	–129.3
150	0.82	–146.7	2.24	54.2	0.04	–16.8	0.80	–135.8
175	0.85	–151.6	1.82	47.9	0.03	–15.2	0.83	–141.4
200	0.87	–156.5	1.50	42.0	0.02	–7.5	0.85	–146.3
250	0.89	–164.0	1.04	33.2	0.01	48.5	0.89	–154.2
300	0.92	–170.5	0.78	27.0	0.03	83.8	0.92	–160.5
350	0.93	–175.8	0.59	23.1	0.04	91.3	0.93	–165.7
400	0.94	179.1	0.47	20.9	0.06	91.9	0.95	–170.1
450	0.95	174.8	0.38	20.0	0.07	91.5	0.95	–174.1
500	0.94	170.7	0.32	20.8	0.09	89.4	0.96	–177.6
600	0.94	163.1	0.25	26.1	0.12	85.7	0.96	176.1
700	0.94	156.0	0.22	33.7	0.14	81.9	0.96	170.6
800	0.93	149.2	0.21	41.9	0.17	78.9	0.96	165.5
900	0.93	142.5	0.22	47.9	0.19	73.1	0.94	160.9
1000	0.92	136.1	0.23	57.3	0.17	75.3	0.93	165.9

Note

1. For more extensive s-parameters see internet:
   http://www.semiconductors.philips.com/markets/communications/wirelesscommunication/broadcast.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads **SOT123A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.78 9.42	2.72 2.31	20.71 19.93	3.33 3.04	4.63 4.11	18.42	24.87 24.64	6.48 6.22	9.78 9.39	0.25	0.51	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.385 0.371	0.107 0.091	0.815 0.785	0.131 0.120	0.182 0.162	0.725	0.980 0.970	0.255 0.245	0.385 0.370	0.010	0.020	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						99-03-29

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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