

BLF2425M7L140; BLF2425M7LS140

Power LDMOS transistor

Rev. 1 — 30 January 2012

Objective data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M7L140 and BLF2425M7LS140 are designed for high-power CW applications and are assembled in high performance ceramic packages, available in eared and earless versions

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Test signal	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η _D (%)
CW	2450	28	140	17.5	52

1.2 Features and benefits

- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched for ease of use (input and output)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

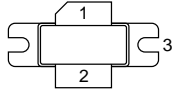

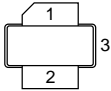
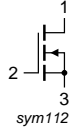
1.3 Applications

- Industrial, scientific and medical applications in the frequency range 2400 MHz to 2500 MHz



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF2425M7L140 (SOT502A)			
1	drain		 sym112
2	gate		
3	source [1]		
BLF2425M7LS140 (SOT502B)			
1	drain		 sym112
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M7L140	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF2425M7LS140	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 125\text{ W}$	0.28	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.16\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 216\text{ mA}$	1.5	1.8	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	-	42	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	500	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 216\text{ mA}$	-	1.87	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 7.56\text{ A}$	-	69	-	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: CW; $f = 2400\text{ MHz}$; $V_{DS} = 28\text{ V}$; $I_{Dq} = 1300\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$ unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 140\text{ W}$	15	17.5	-	dB
RL_{in}	input return loss	$P_L = 140\text{ W}$	-	-12	-8	dB
η_D	drain efficiency	$P_L = 140\text{ W}$	47	52	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF2425M7L140 and BLF2425M7LS140 are capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 1300\text{ mA}$; $P_L = 140\text{ W}$ (CW); $f = 2450\text{ MHz}$.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. $I_{Dq} = <tbid>$; $V_{DS} = <tbid>$. Z_S and Z_L defined in [Figure 1](#).

f (MHz)	Z_S (Ω)	Z_L (Ω)
<tbid>	<tbid>	<tbid>

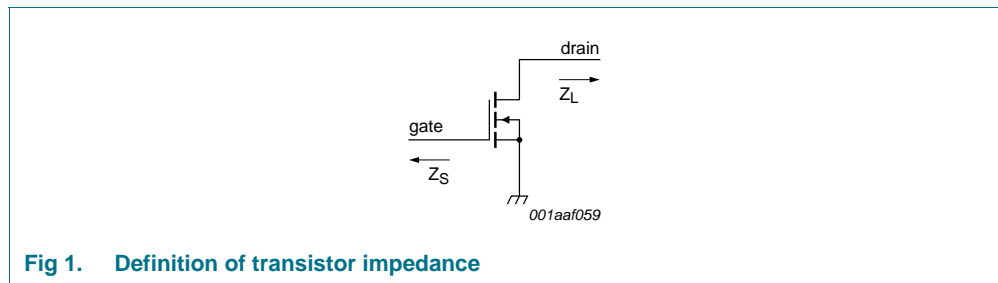


Fig 1. Definition of transistor impedance

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

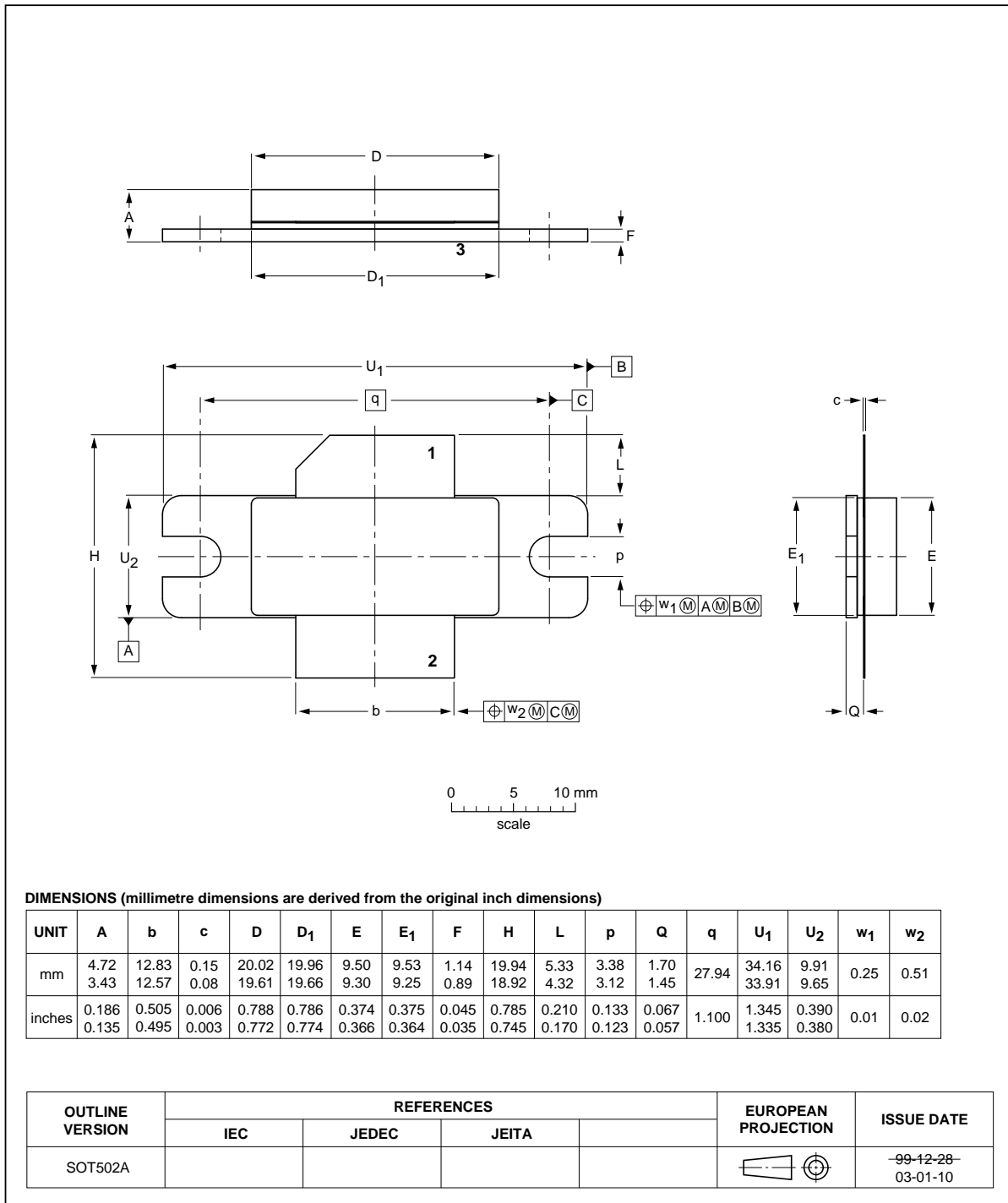


Fig 2. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

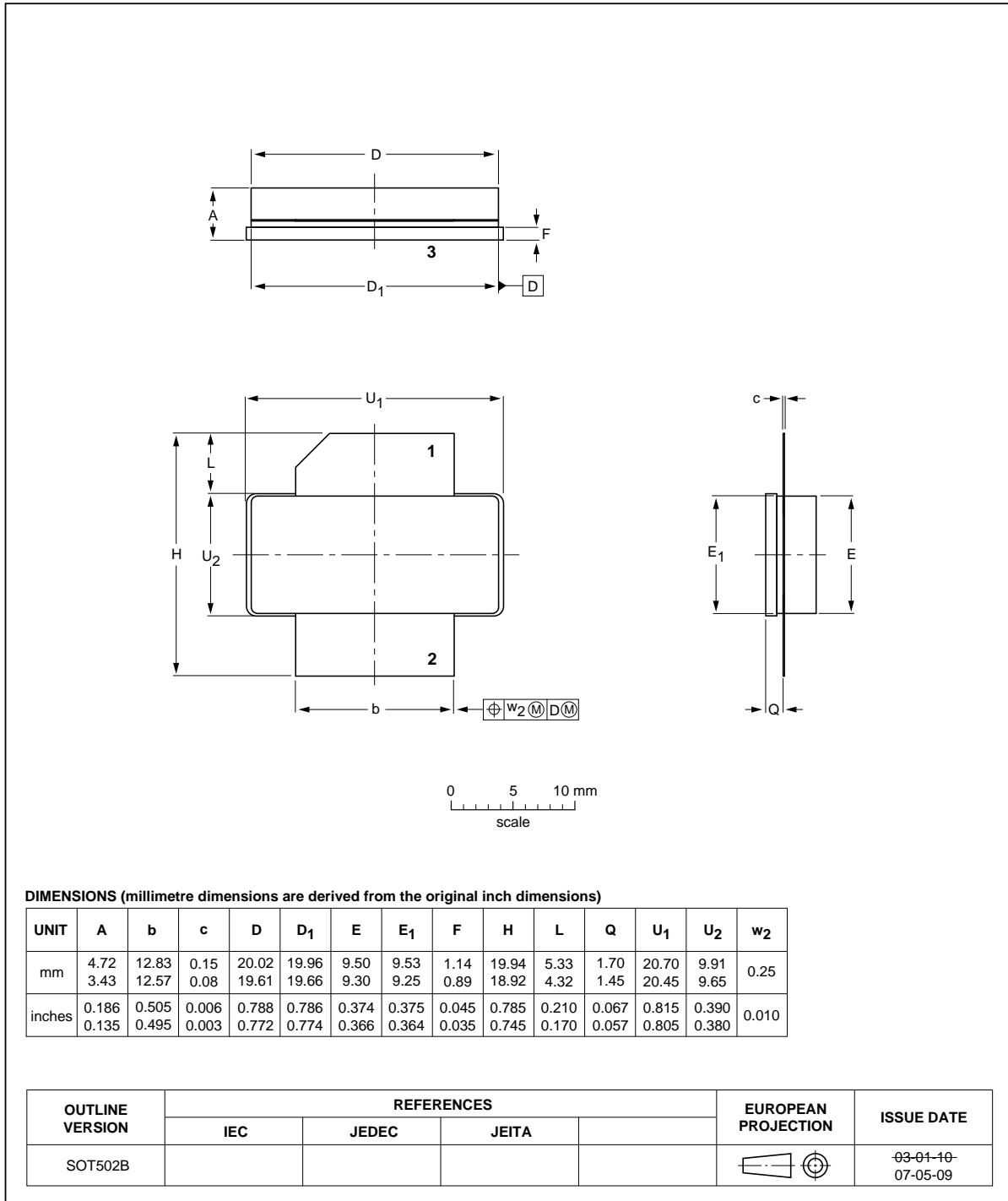


Fig 3. Package outline SOT502B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
CW	Continuous Wave
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M7L140_2425M7LS140 v.1	20120130	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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