

# PMZ390UN

N-channel TrenchMOS standard level FET

Rev. 01 — 12 July 2007

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Profile 55 % lower than SOT23
- Low on-state resistance
- Leadless package
- Footprint 90 % smaller than SOT23
- Fast switching
- Standard level compatible threshold

### 1.3 Applications

- Driver circuits
- Load switching in portable appliances

### 1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $R_{DS(on)} \leq 460 \text{ m}\Omega$
- $I_D \leq 1.78 \text{ A}$
- $P_{tot} \leq 2.50 \text{ W}$

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	<p>Transparent top view</p> <p><b>SOT883 (SC-101)</b></p>	<p>mbb076</p>
2	source (S)		
3	drain (D)		

### 3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
PMZ390UN	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883

### 4. Limiting values

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

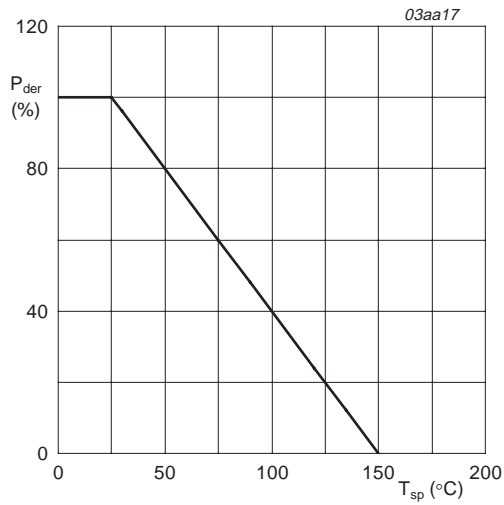
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-	±8	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	1.78	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	1.13	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	3.56	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	2.50	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C

**Source-drain diode**

$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	1.78	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	3.56	A

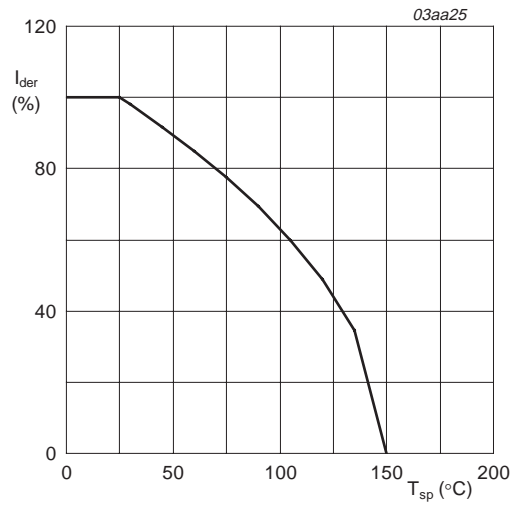
**Electrostatic discharge**

$V_{esd}$	electrostatic discharge voltage	all pins			
		human body model; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$	-	60	V
		machine model; $C = 200\text{ pF}$	-	30	V



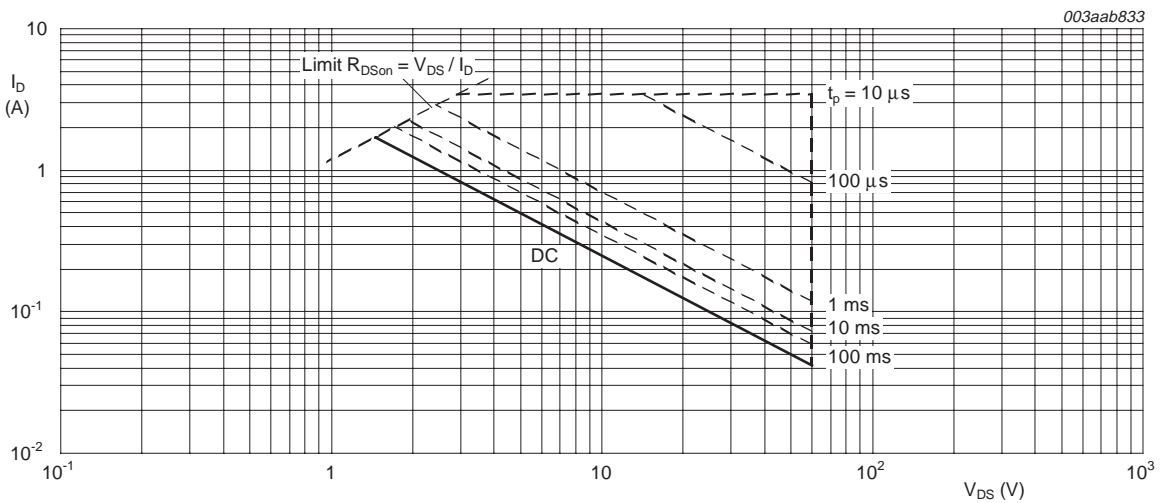
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	50	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	670	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

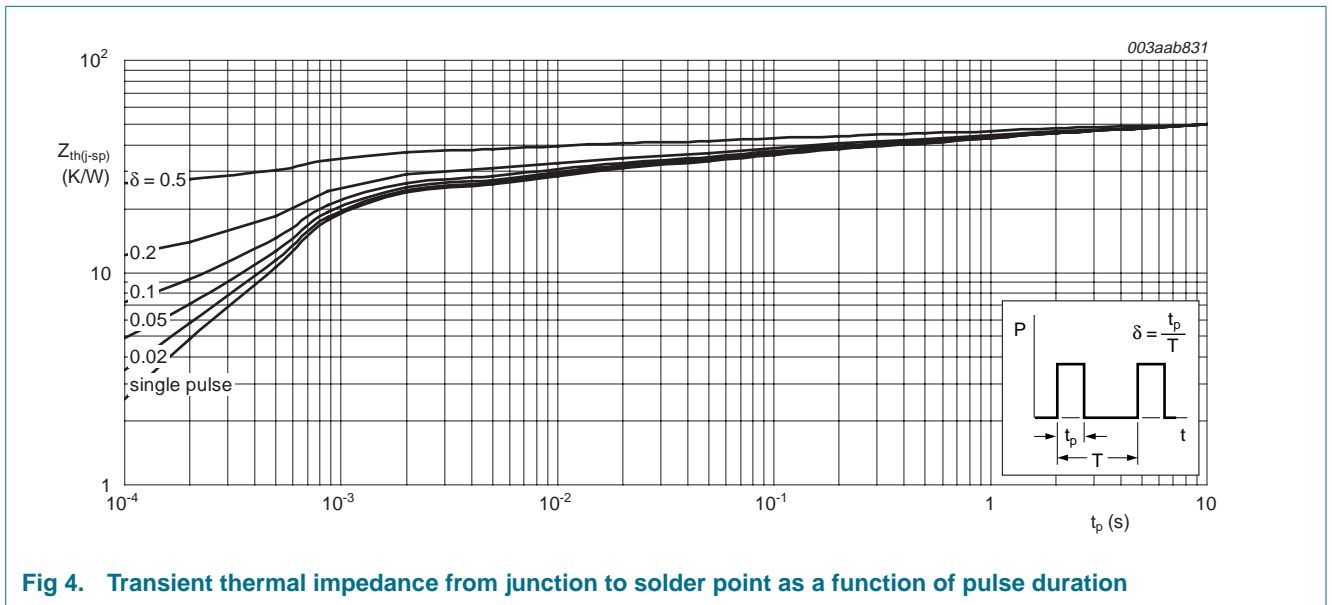


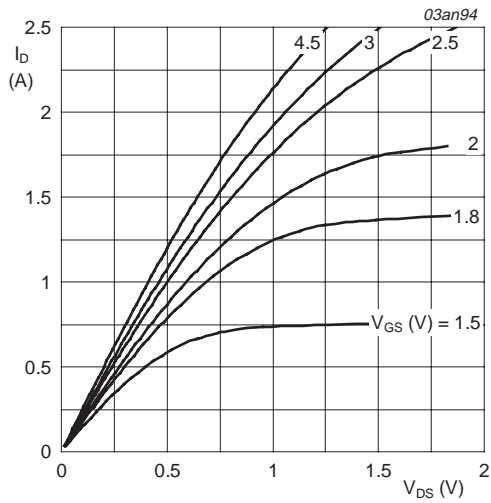
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

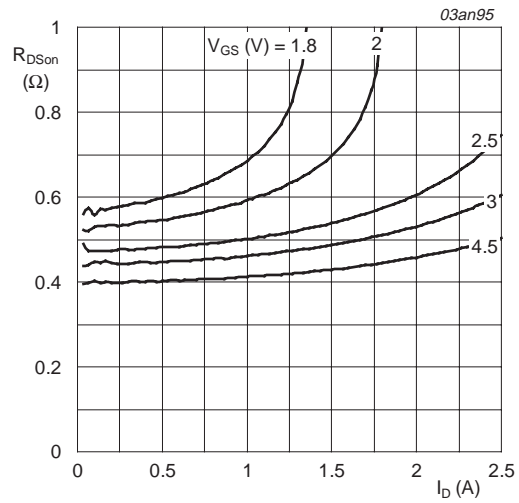
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25\ \text{mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		$T_j = 25\text{ °C}$	0.45	0.7	0.95	V
		$T_j = 150\text{ °C}$	0.25	-	-	V
		$T_j = -55\text{ °C}$	-	-	1.15	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 8\ \text{V}; V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 0.2\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		$T_j = 25\text{ °C}$	-	390	460	m $\Omega$
		$T_j = 150\text{ °C}$	-	663	782	m $\Omega$
		$V_{GS} = 2.5\ \text{V}; I_D = 0.1\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	460	560	m $\Omega$
		$V_{GS} = 1.8\ \text{V}; I_D = 0.075\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	550	730	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 1\ \text{A}; V_{DS} = 15\ \text{V}; V_{GS} = 4.5\ \text{V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	0.89	-	nC
$Q_{GS}$	gate-source charge		-	0.1	-	nC
$Q_{GD}$	gate-drain charge		-	0.2	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 25\ \text{V}; f = 1\ \text{MHz}$ ; see <a href="#">Figure 14</a>	-	43	-	pF
$C_{oss}$	output capacitance		-	7.7	-	pF
$C_{rss}$	reverse transfer capacitance		-	4.8	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\ \text{V}; R_L = 15\ \Omega; V_{GS} = 10\ \text{V}; R_G = 6\ \Omega$	-	4	-	ns
$t_r$	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
$t_f$	fall time		-	4.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 0.3\ \text{A}; V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 13</a>	-	0.76	1.2	V



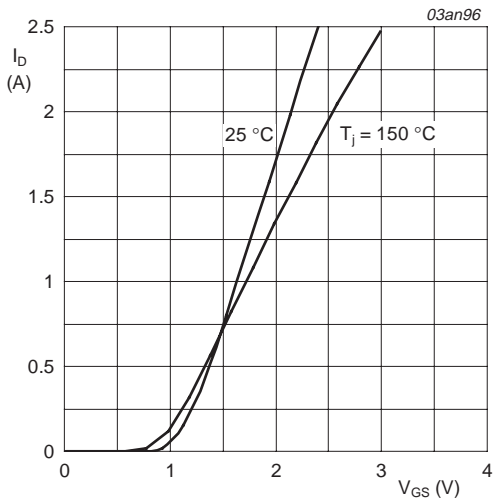
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



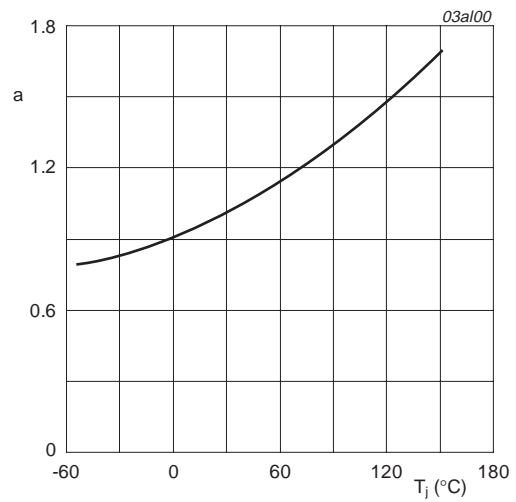
$T_j = 25\text{ }^\circ\text{C}$

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



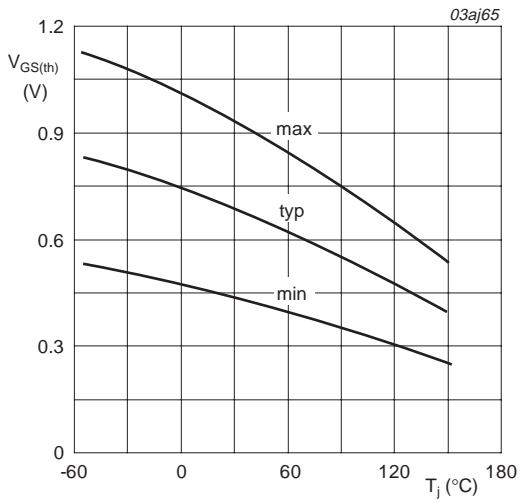
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



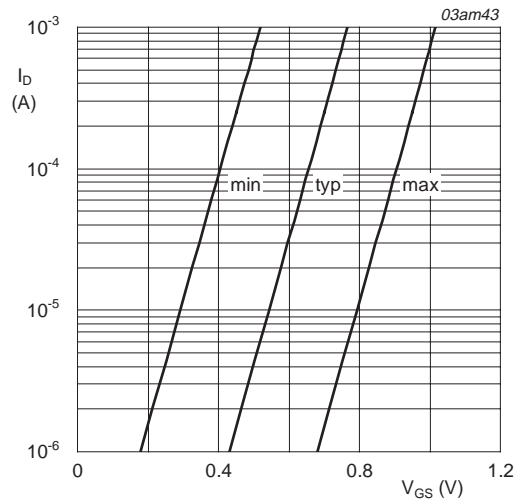
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



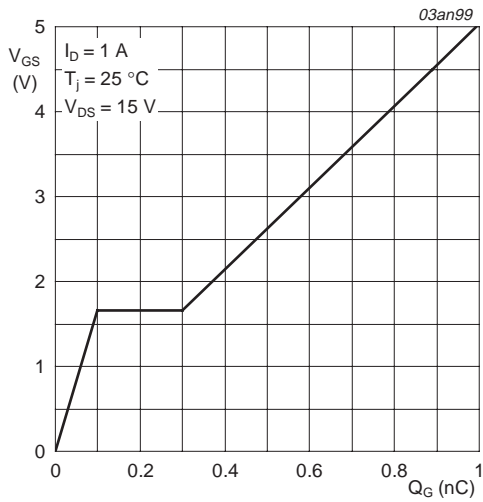
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1 \text{ A}; V_{DS} = 15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

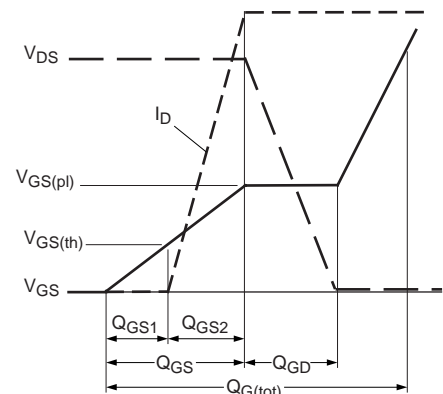
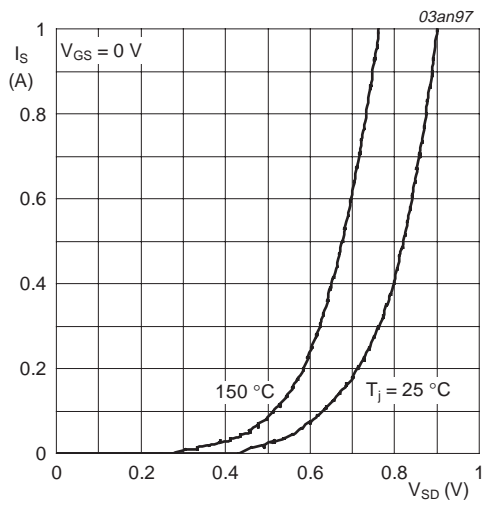
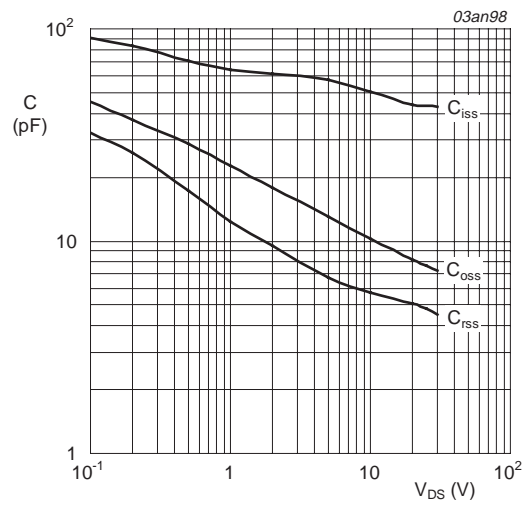


Fig 12. Gate charge waveform definitions



$T_j = 25$  °C and  $150$  °C;  $V_{GS} = 0$  V

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0$  V;  $f = 1$  MHz

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

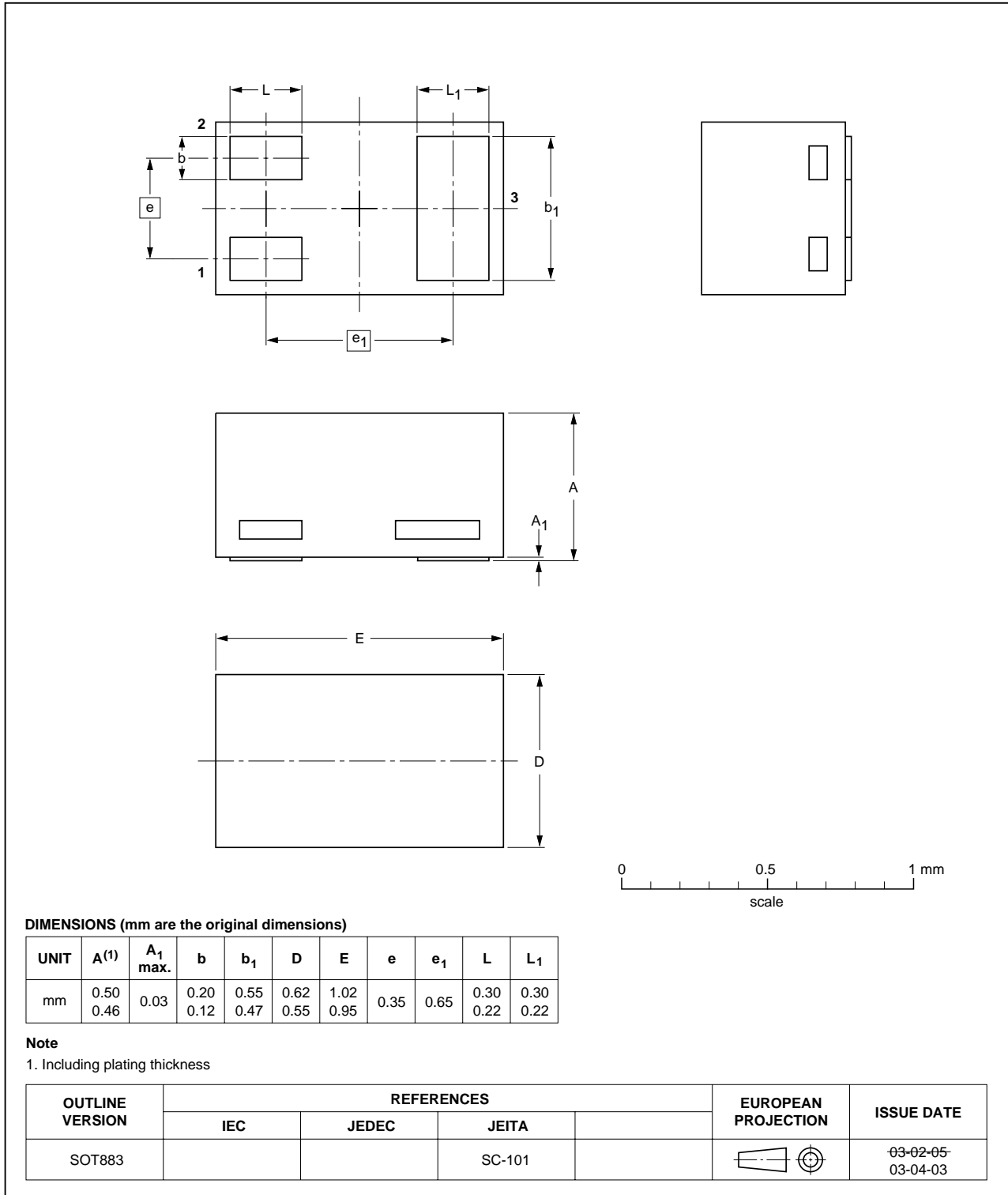
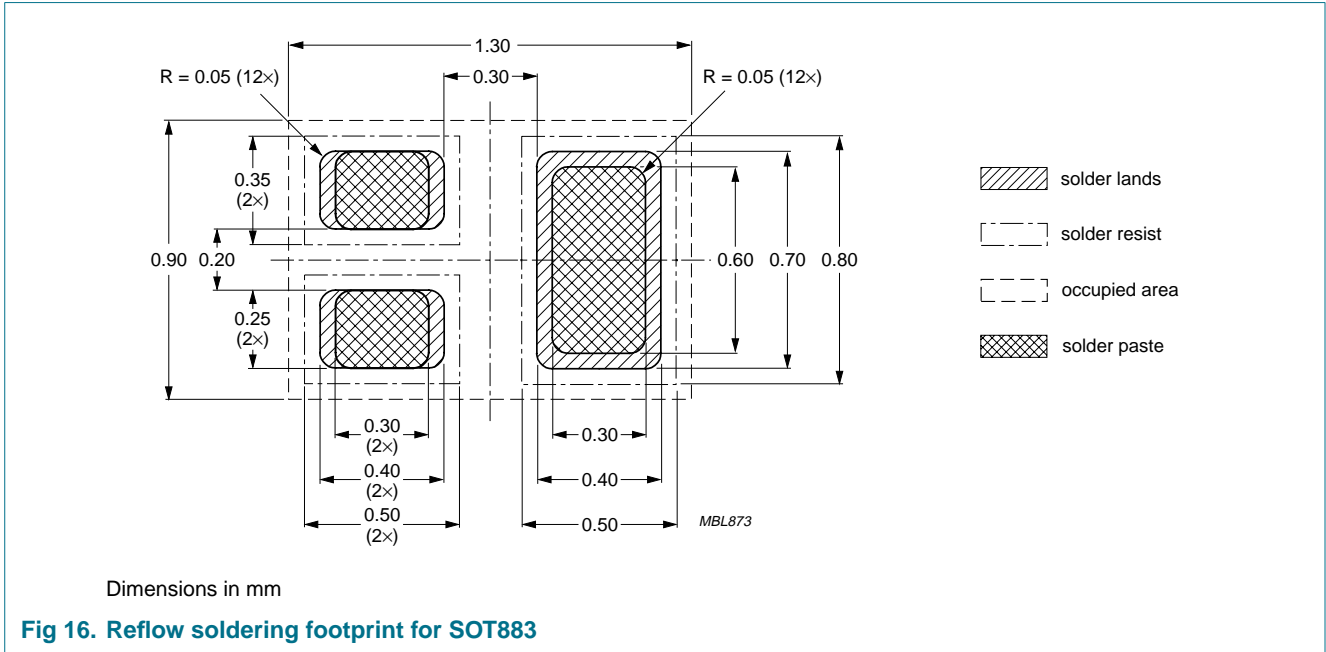


Fig 15. Package outline SO883 (SC-101)

8. Soldering



## 9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMZ390UN_1	20070712	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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