

# PHD97NQ03LT

## N-channel TrenchMOS logic level FET

Rev. 01 — 24 March 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Fast switching
- Lead-free packing
- Logic level threshold
- Low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- Computer motherboard high frequency DC-to-DC converters
- Switched-mode power supplies
- Voltage regulators

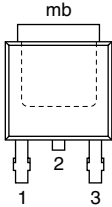
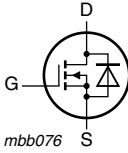
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	107	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 12\text{ V};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	1.9	-	nC
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	5.3	6.3	m $\Omega$

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT428 (SC-63; DPAK)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

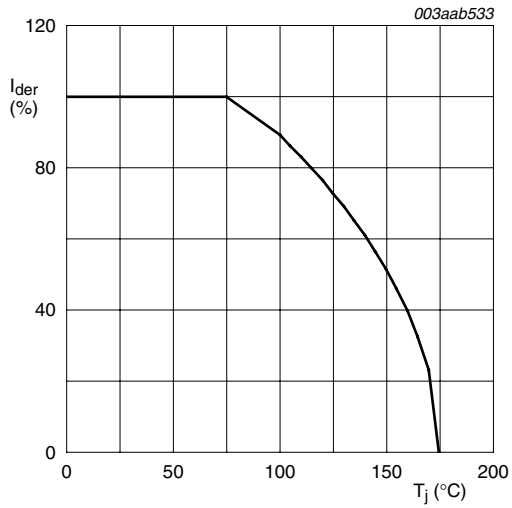
Type number	Package		Version
	Name	Description	
PHD97NQ03LT	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

Table 4. Limiting values

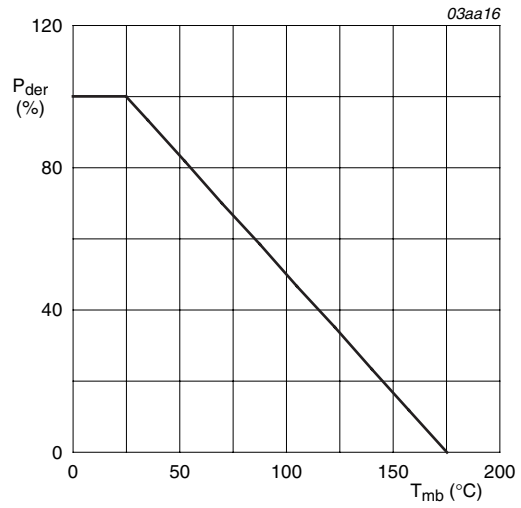
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$	-	25	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^\circ\text{C}$ ; see <a href="#">Figure 1</a>	-	69	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	75	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 3</a>	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	107	W
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ }^\circ\text{C}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $I_D = 35\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; unclamped; $t_p = 0.1\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	60	mJ



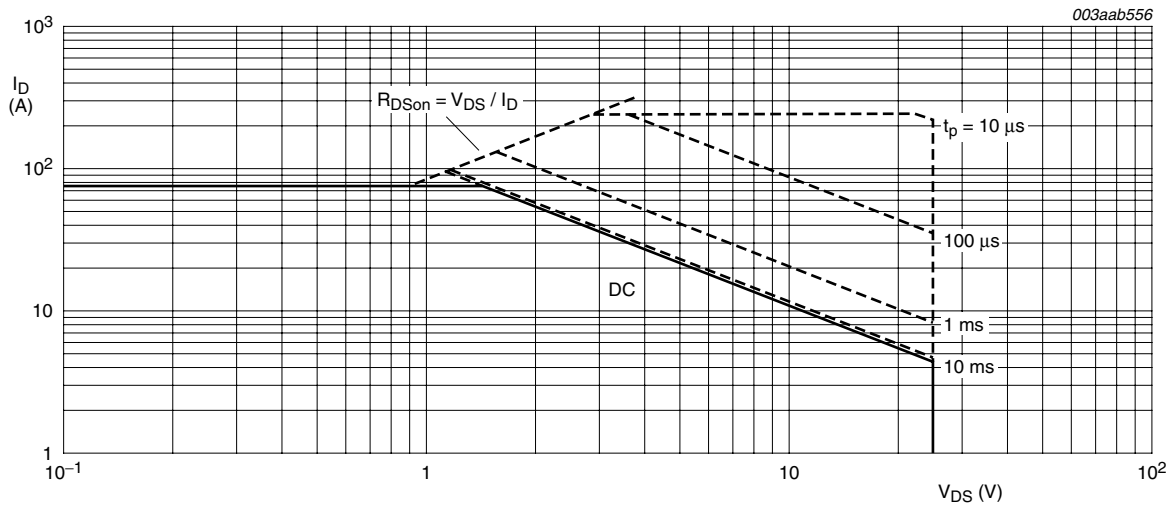
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse

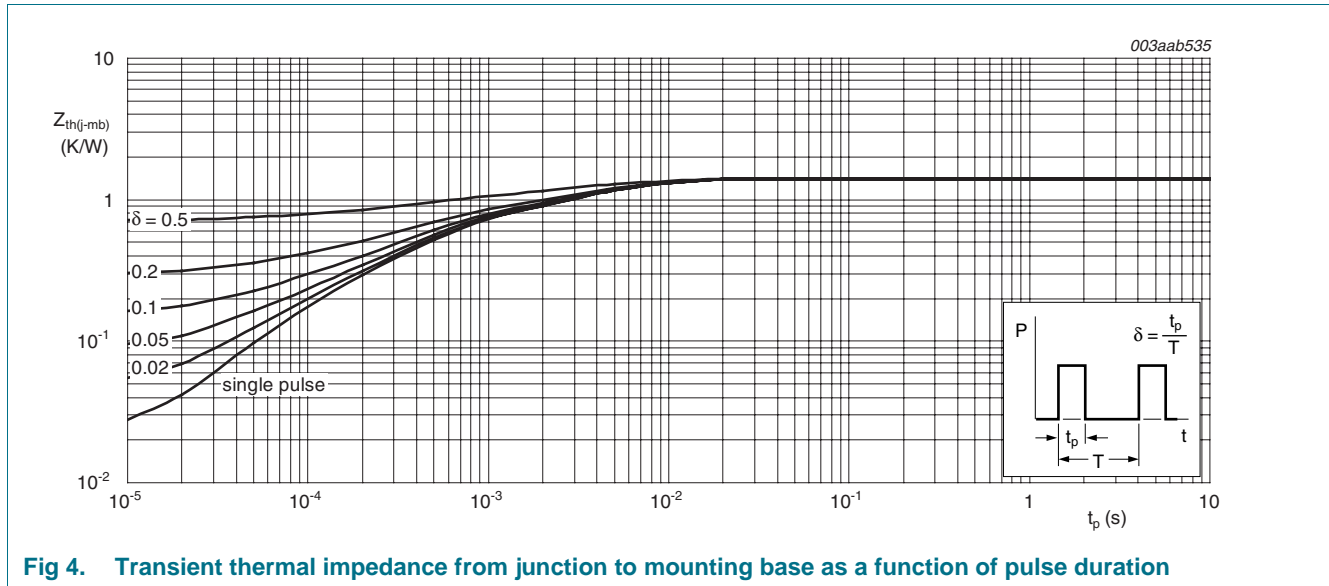
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	75	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

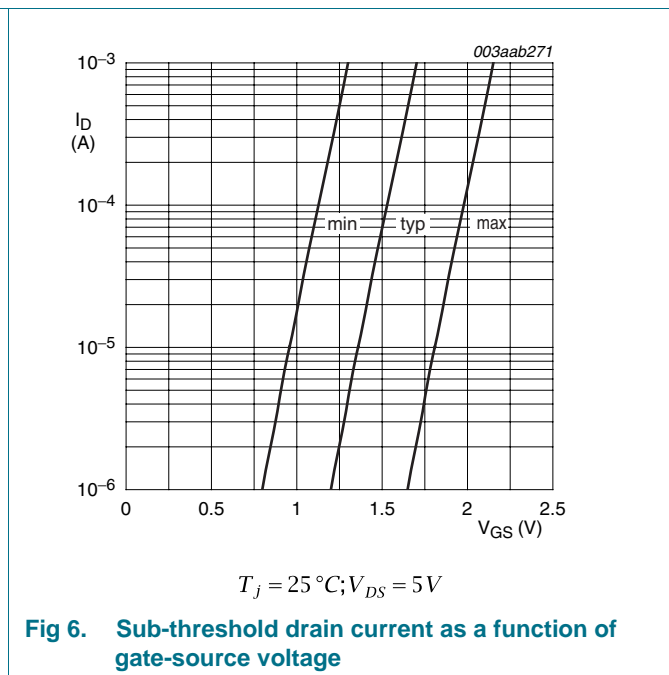
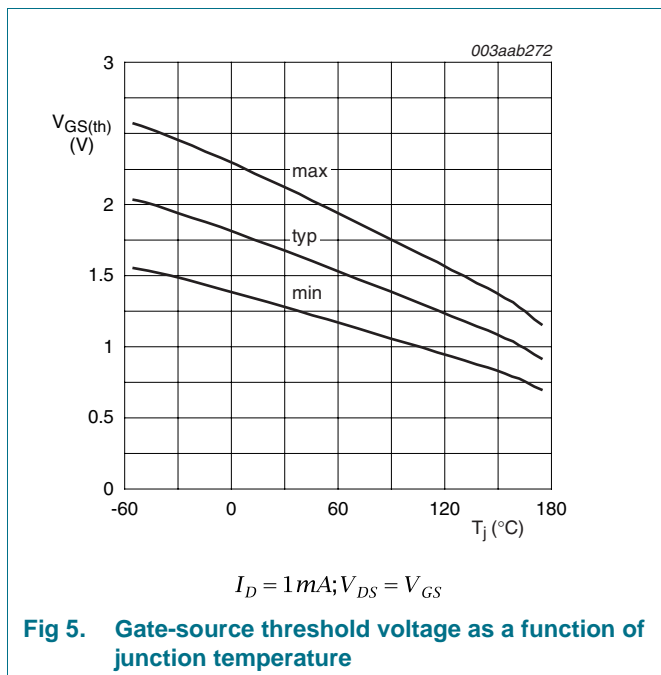
## 6. Characteristics

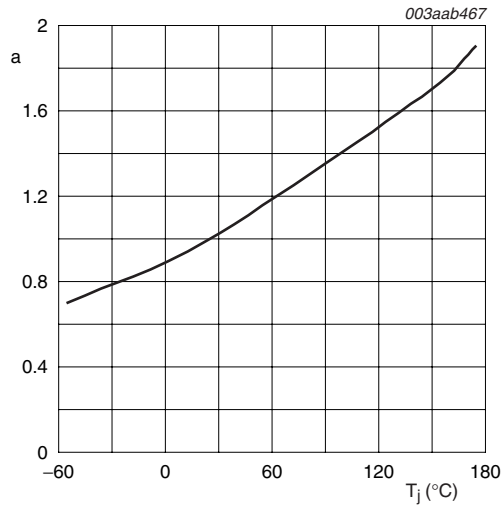
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a> ; see <a href="#">Figure 6</a>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a>	0.7	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a>	-	-	2.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	10.1	12	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	8	10.6	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	5.3	6.3	m $\Omega$
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.5	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	11.7	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 4.5 \text{ V}$	-	10.2	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	6.2	-	nC
$Q_{GS1}$	pre-threshold gate-source charge		-	3.4	-	nC
$Q_{GS2}$	post-threshold gate-source charge		-	2.8	-	nC
$Q_{GD}$	gate-drain charge		-	1.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	3.1	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	1570	-	pF
		$V_{DS} = 0 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$	-	1800	-	pF
$C_{oss}$	output capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	380	-	pF
$C_{rss}$	reverse transfer capacitance	$T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	160	-	pF

Table 6. Characteristics ...continued

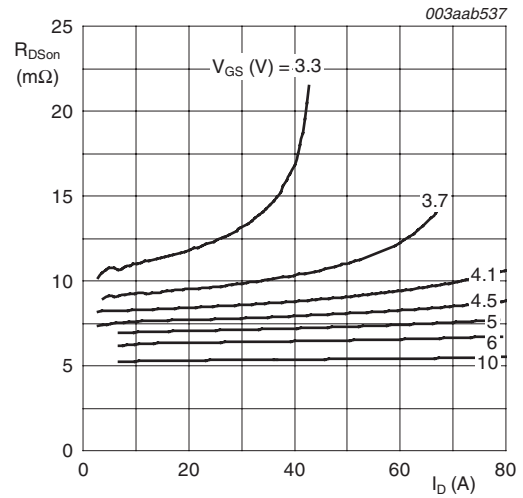
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\ \Omega; V_{GS} = 4.5\text{ V};$	-	18	-	ns
$t_r$	rise time	$R_{G(ext)} = 5.6\ \Omega$	-	33	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
$t_f$	fall time		-	12	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	0.87	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	38	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}$	-	14	-	nC





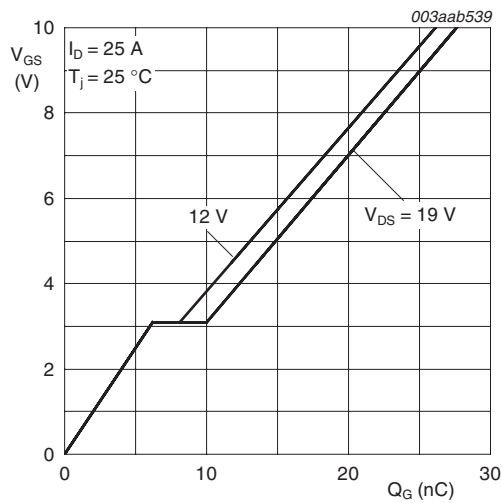
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 7. Normalized drain-source on-state resistance factor as a function of junction temperature**



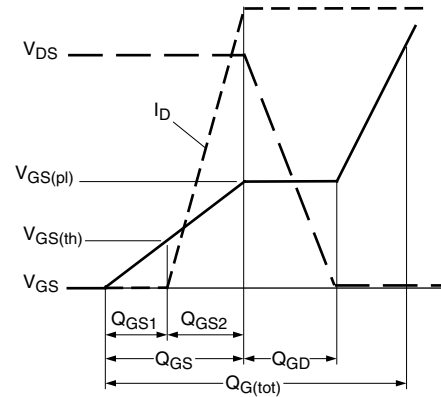
$T_j = 25^{\circ}C$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**

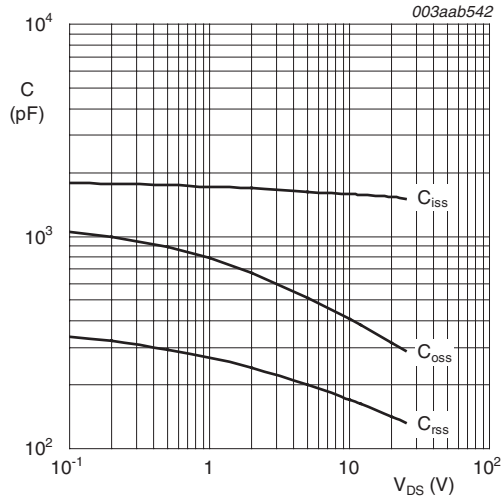


$I_D = 25A; V_{DS} = 12V \text{ and } 19V$

**Fig 9. Gate-source voltage as a function of gate charge; typical values**

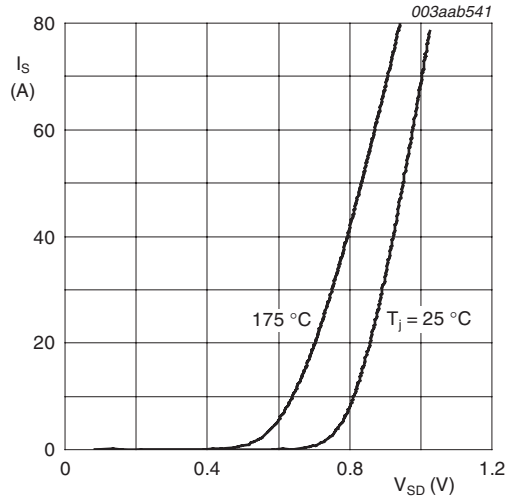


**Fig 10. Gate charge waveform definitions**



$V_{GS} = 0V; f = 1MHz$

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$T_j = 25^\circ C \text{ and } 175^\circ C; V_{GS} = 0V$

**Fig 12. Source current as a function of source-drain voltage; typical values**



7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

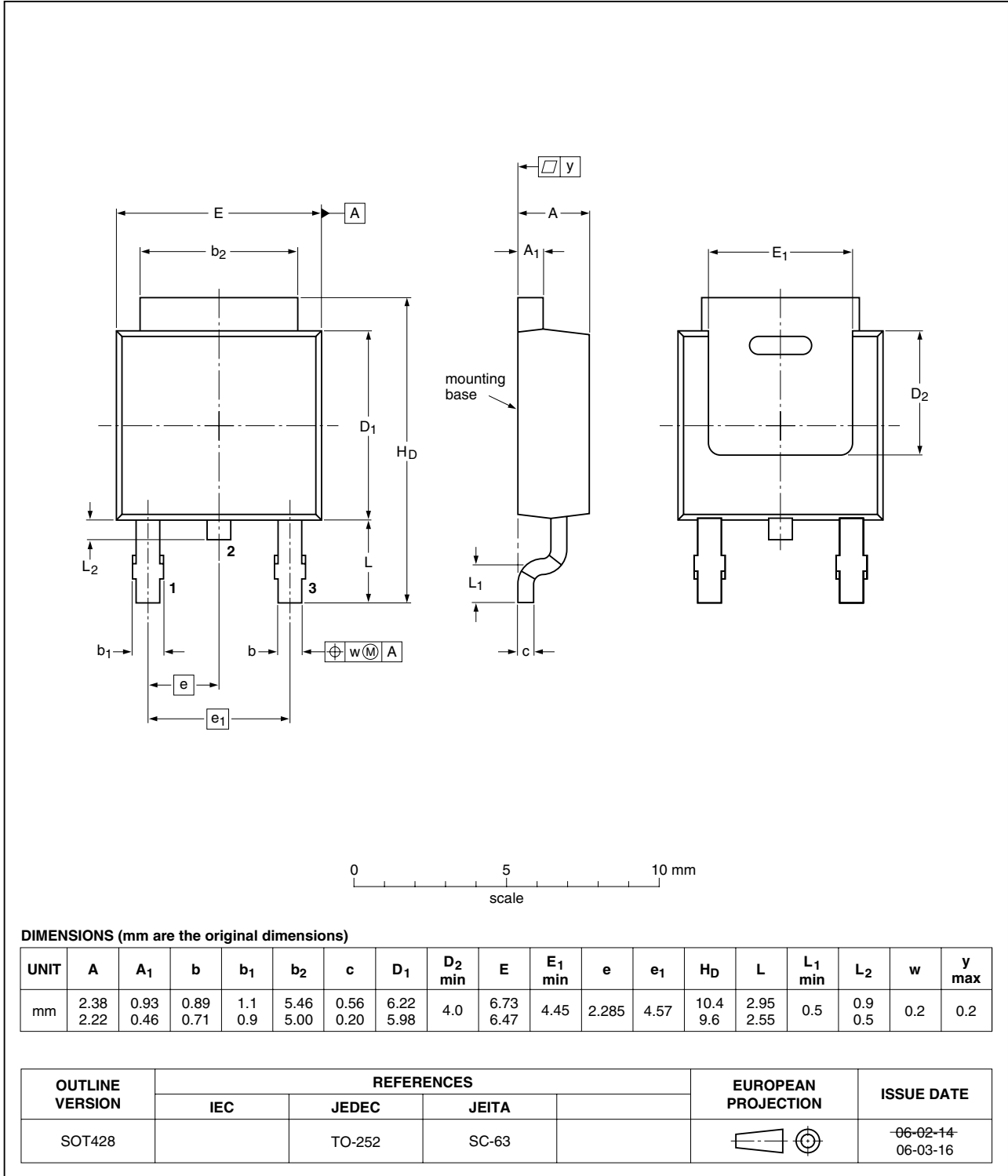


Fig 13. Package outline SOT428 (DPAK)

## 8. Revision history

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Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD97NQ03LT_1	20090324	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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