

N0118GA

SCR

Rev. 1 — 11 July 2011

Product data sheet

1. Product profile

1.1 General description

Planar passivated ultra sensitive gate Silicon Controlled Rectifier in a SOT54 (T0-92) plastic package.

1.2 Features and benefits

- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Ultra sensitive gate

1.3 Applications

- Electronic ballasts
- Safety shut down and protection circuits
- Sensing circuits
- Smoke detectors
- Switched Mode Power Supplies

1.4 Quick reference data

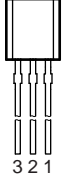

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$; see Figure 4 ; see Figure 5	-	-	8	A
$I_{T(AV)}$	average on-state current	half sine wave; $T_{\text{lead}} \leq 67\text{ °C}$; see Figure 3	-	-	0.51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{\text{lead}} \leq 67\text{ °C}$; see Figure 1 ; see Figure 2	-	-	0.8	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; see Figure 7	0.5	-	7	μA



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>SOT54 (TO-92)</p>	
2	G	gate		
3	K	cathode		

3. Ordering information

Table 3. Ordering information

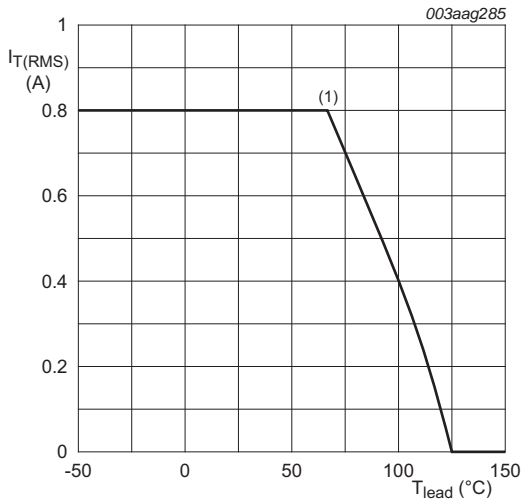
Type number	Package		
	Name	Description	Version
N0118GA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

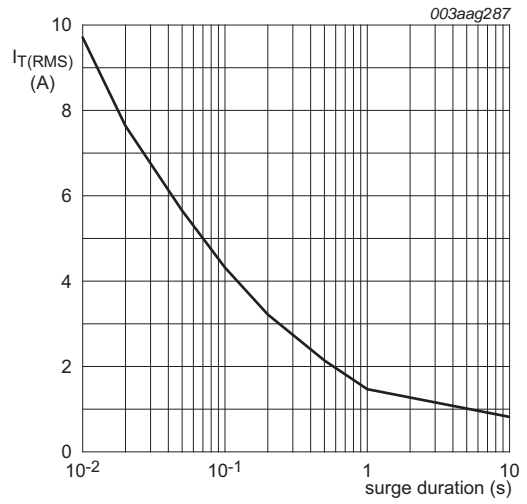
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 67\text{ °C}$; see Figure 3	-	0.51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 67\text{ °C}$; see Figure 1 ; see Figure 2	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; see Figure 4 ; see Figure 5	-	8	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	0.32	A ² s
di_T/dt	rate of rise of on-state current	$I_T = 0.8\text{ A}$; $I_G = 10\text{ mA}$; $di_G/dt = 0.1\text{ A}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C



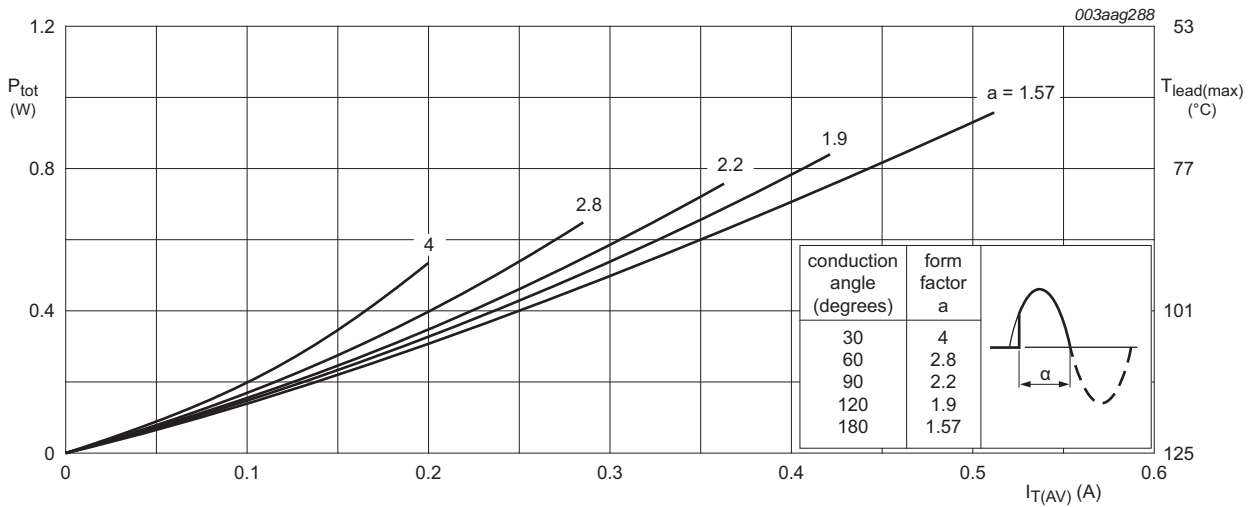
(1) $T_{lead} = 67\text{ }^{\circ}\text{C}$

Fig 1. RMS on-state current as a function of lead temperature; maximum values



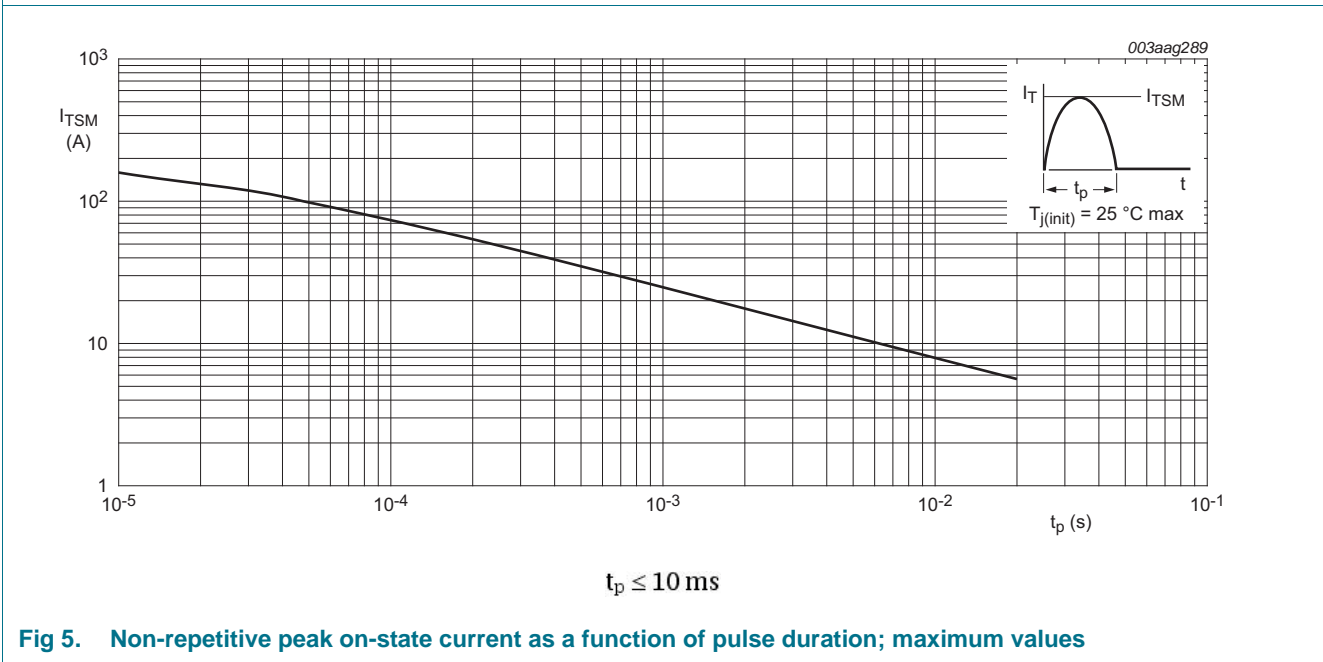
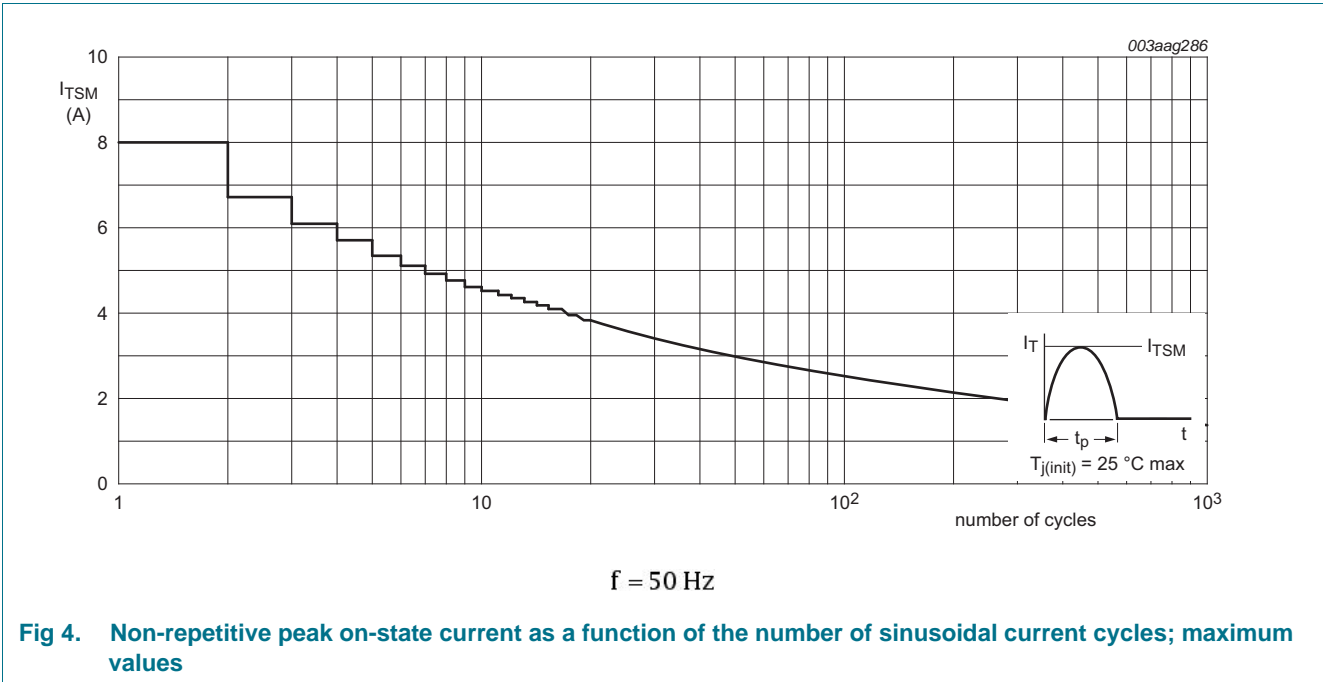
$f = 50\text{ Hz}$
 $T_{lead} = 67\text{ }^{\circ}\text{C}$

Fig 2. RMS on-state current as a function of surge duration; maximum values



$\alpha = \text{conduction angle}$
 $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

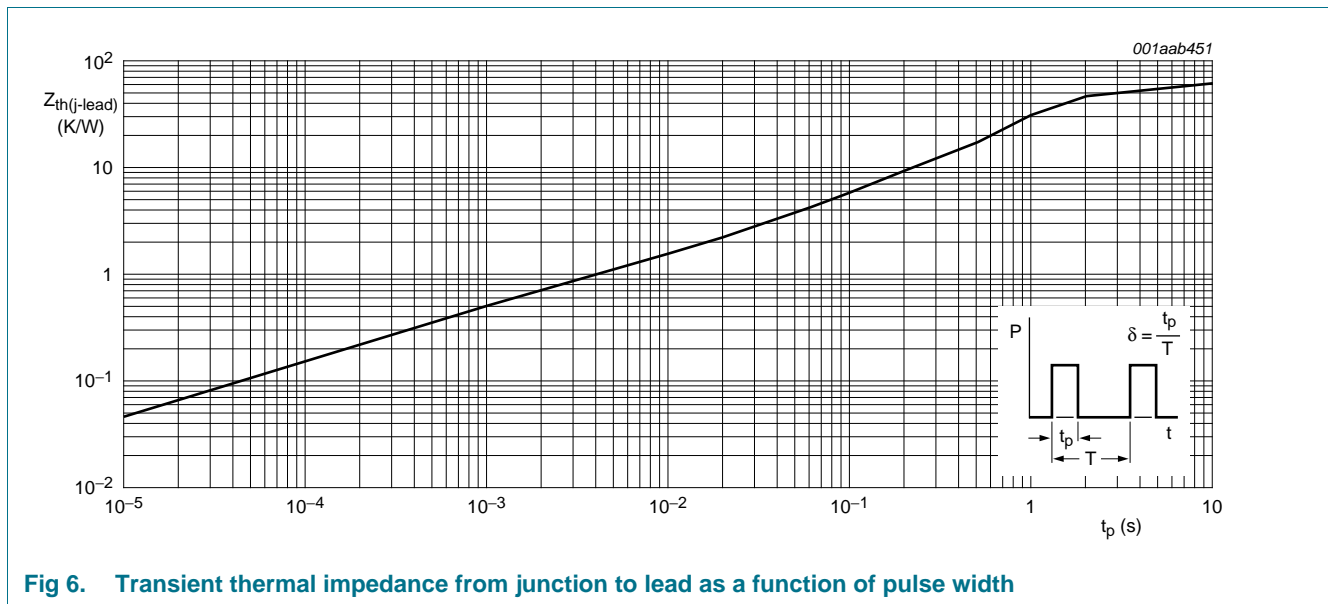
Fig 3. Total power dissipation as a function of average on-state current; maximum values



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	0.5	-	7	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 8	-	-	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	-	5	mA
V_T	on-state voltage	$I_T = 1.6\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 11	-	1.4	1.95	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 12	-	-	0.8	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$	-	-	10	μA
		$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$	-	-	100	μA
I_R	reverse current	$T_j = 25\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; $V_R = 600\text{ V}$	-	-	10	μA
		$T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; $V_R = 600\text{ V}$	-	-	100	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; exponential waveform; see Figure 13 ; see Figure 14	75	-	-	$\text{V}/\mu\text{s}$

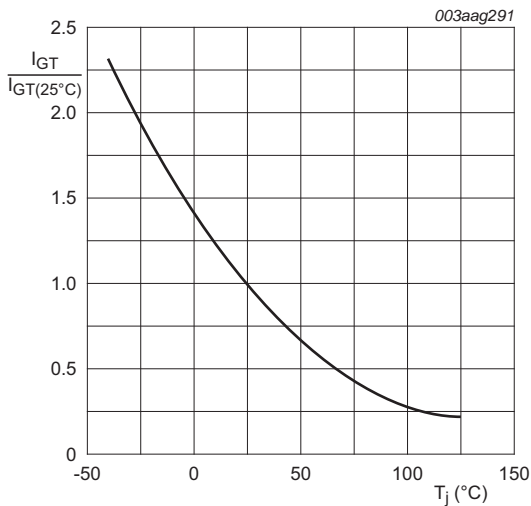
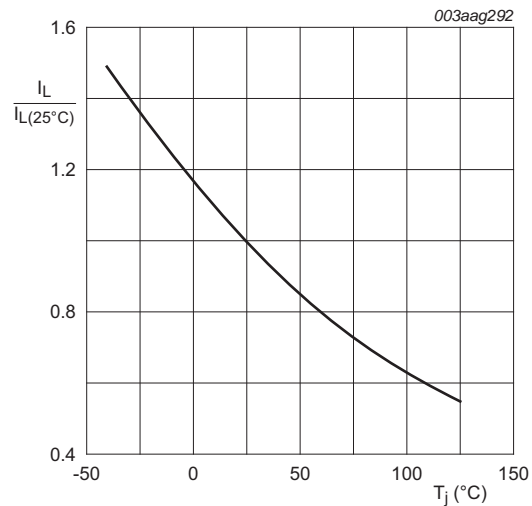
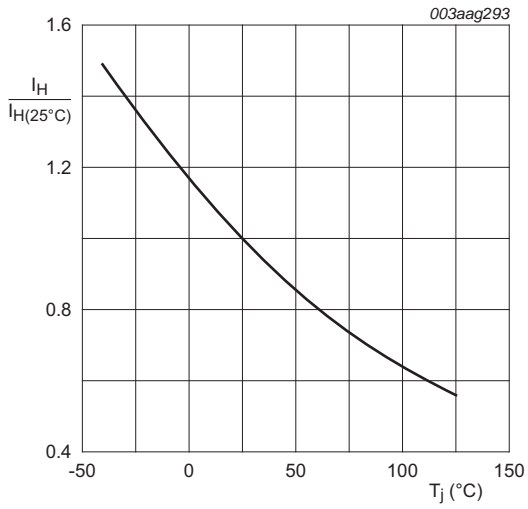


Fig 7. Normalized gate trigger current as a function of junction temperature



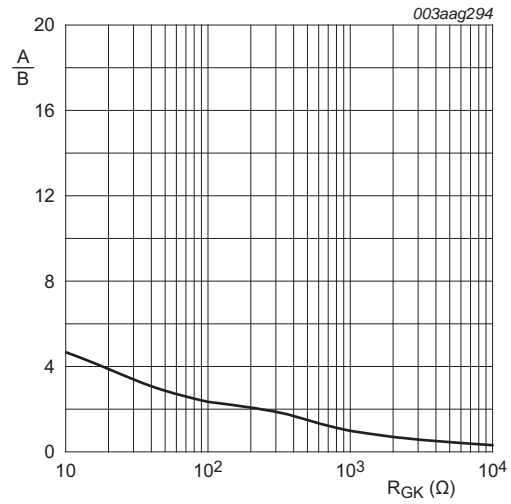
$R_{GK} = 1\text{ k}\Omega$

Fig 8. Normalized latching current as a function of junction temperature



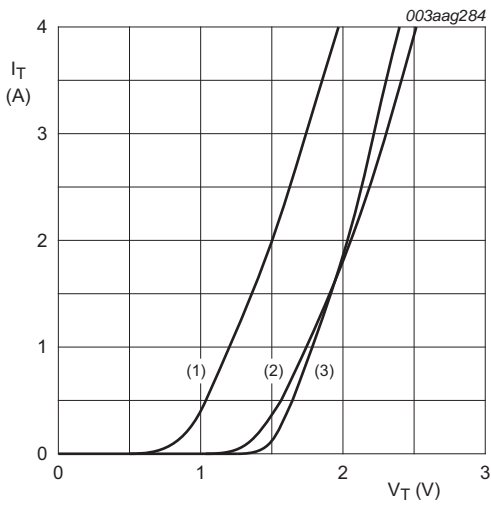
$R_{GK} = 1\text{ k}\Omega$

Fig 9. Normalized holding current as a function of junction temperature



$A = I_H [R_{GK}]$
 $B = I_H [R_{GK} = 1\text{ k}\Omega]$
 $T_j = 25\text{ }^\circ\text{C}$

Fig 10. Normalized holding current as a function of gate-cathode resistance (typical values)



$V_O = 1.383\text{ V}; R_S = 0.40\text{ }\Omega$
 (1) $T_j = 125\text{ }^\circ\text{C}$; typical values
 (2) $T_j = 125\text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25\text{ }^\circ\text{C}$; maximum values

Fig 11. On-state current as a function of on-state voltage

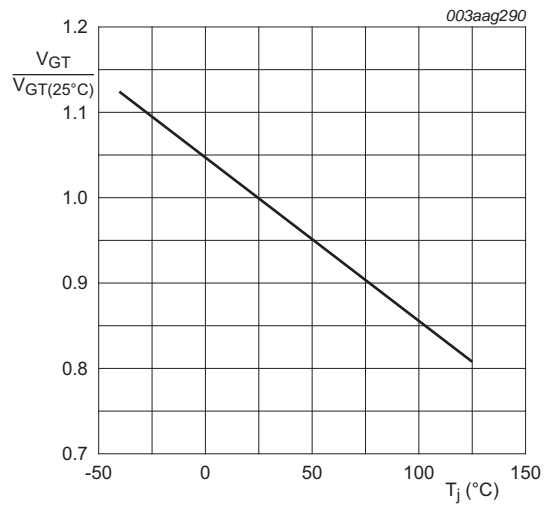
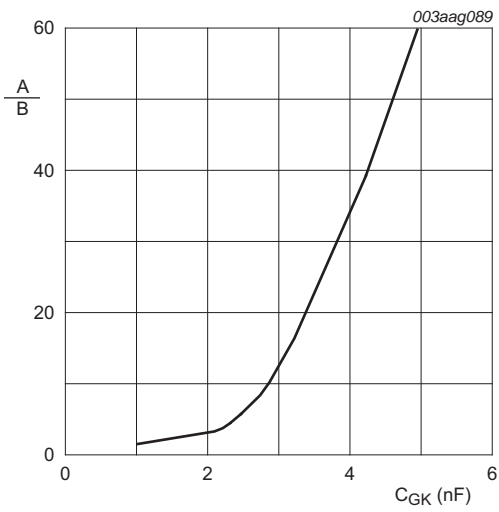


Fig 12. Normalized gate trigger voltage as a function of junction temperature

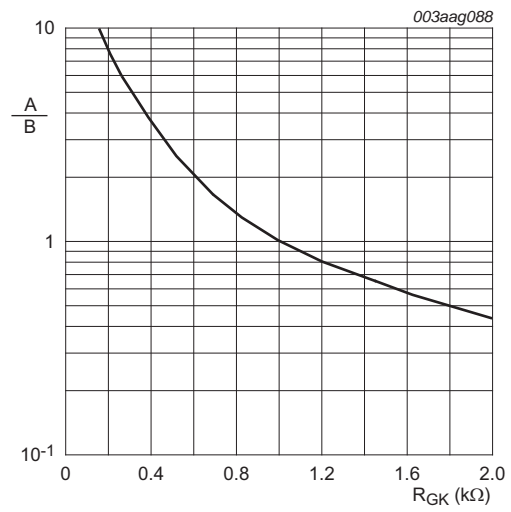


$$A = \frac{dV}{dt} [C_{GK}]$$

$$B = \frac{dV}{dt} [R_{GK} = 1\text{ k}\Omega]$$

$T_j = 125\text{ }^\circ\text{C}; R_{GK} = 1\text{ k}\Omega; V_{DM} = 402\text{ V}$

Fig 13. Normalized dV/dt immunity as a function of gate-cathode capacitance (typical values)



$$A = \frac{dV}{dt} [R_{GK}]$$

$$B = \frac{dV}{dt} [R_{GK} = 1\text{ k}\Omega]$$

$T_j = 125\text{ }^\circ\text{C}; V_{DM} = 402\text{ V}$

Fig 14. Normalized dV/dt immunity as a function of gate-cathode resistance (typical values)

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

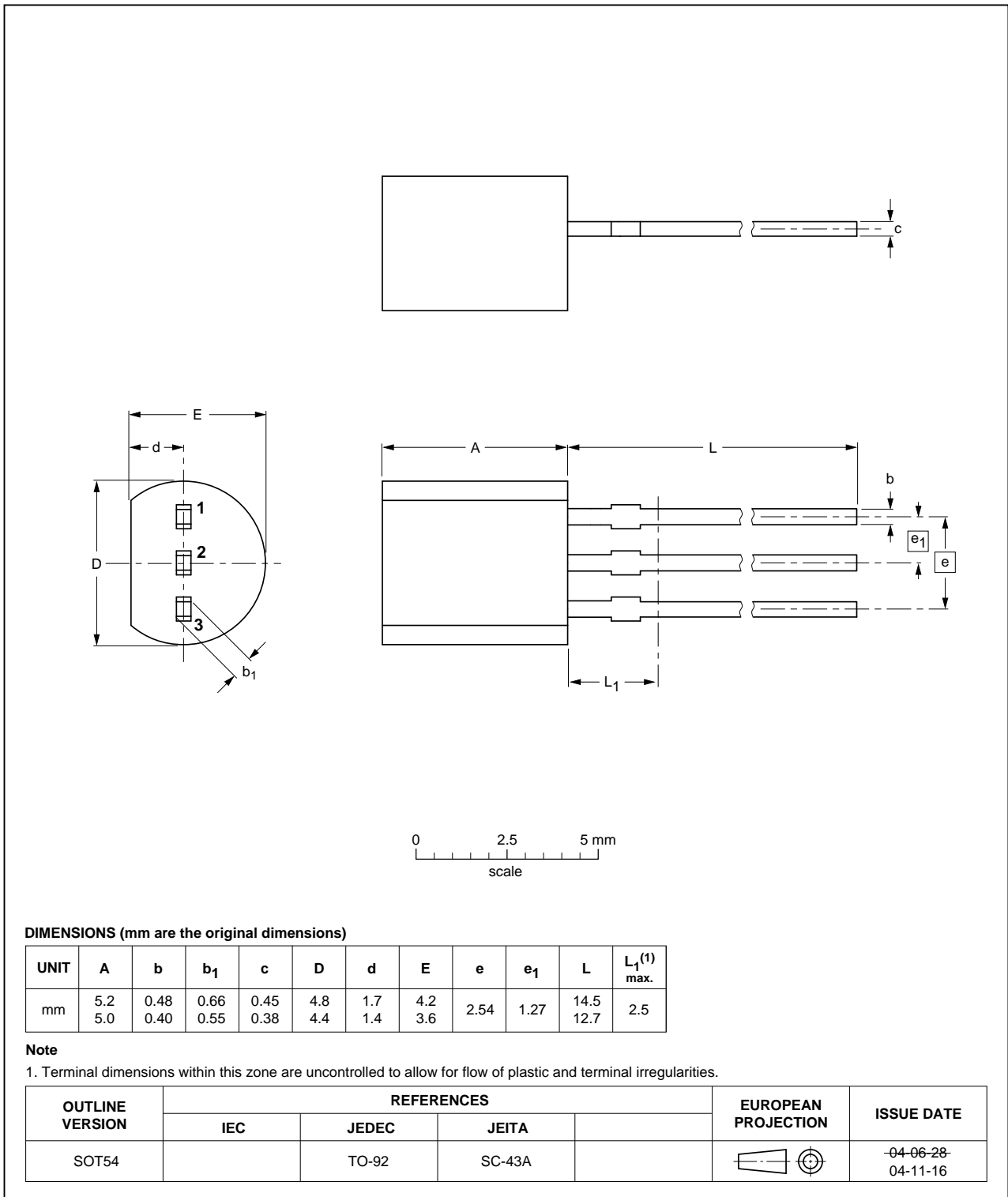


Fig 15. Package outline SOT54 (TO-92)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
N0118GA v.1	20110711	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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