# **BUK761R8-30C**

# N-channel TrenchMOS standard level FET

Rev. 02 — 20 August 2007

**Product data sheet** 

## 1. Product profile

#### 1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package, using NXP Ultra High-Performance (UHP) automotive TrenchMOS technology.

#### 1.2 Features

- 175 °C rated
- Standard level compatible
- Q101 compliant
- TrenchMOS technology

#### 1.3 Applications

- 12 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

#### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$I_D$	drain current	$V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; see <u>Figure 1</u> and <u>4</u>	[1][2]	-	-	100	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see Figure 2		-	-	333	W
Static ch	aracteristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see <u>Figure 12</u> and <u>13</u>		-	1.5	1.8	mΩ
Avalanci	ne ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\begin{split} I_D &= 100 \text{ A; } V_{sup} \leq 30 \text{ V;} \\ R_{GS} &= 50  \Omega;  V_{GS} = 10 \text{ V;} \\ T_{j(init)} &= 25 ^{\circ}\text{C} \end{split}$		-	-	1.7	J

<sup>[1]</sup> Refer to document 9397 750 12572 for further information.



<sup>[2]</sup> Continuous current is limited by package.

# 2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		$_{G}$ $(\Box \overline{A})$
mb	D	mounting base; connected to drain	   2   1   3     SOT404 (D2PAK)	mbb076 S

# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK761R8-30C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

# 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	ı	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	-	30	V
$V_{GS}$	gate-source voltage		-	-20	20	V
I <sub>D</sub>	drain current	$T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u> and <u>4</u>	[1][2]	-	100	Α
		$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u> and <u>4</u>	[1][2]	-	100	Α
		$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u> and <u>4</u>	[1][3]	-	312	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; $t_p \le 10 \mu s$ ; pulsed; see Figure 4	-	-	1249	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	333	W
T <sub>stg</sub>	storage temperature		-	-55	175	°C
Tj	junction temperature		-	-55	175	°C
Avalanc	he ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\begin{split} I_D &= 100 \text{ A; } V_{sup} \leq 30 \text{ V; } R_{GS} = 50  \Omega; \\ V_{GS} &= 10 \text{ V; } T_{j(init)} = 25  ^{\circ}\text{C} \end{split}$	-	-	1.7	J
E <sub>DS(AL)R</sub>	repetitive drain-source avalanche energy	see <u>Figure 3</u>	[4][5] [6][7]	-	-	J
Source-	drain diode					
Is	source current	T <sub>mb</sub> = 25 °C	[1][3]	-	312	Α
		T <sub>mb</sub> = 25 °C	[1][2]	-	100	Α
I <sub>SM</sub>	peak source current	$t_p \le 10 \ \mu s; \ pulsed; \ T_{mb} = 25 \ ^{\circ}C$	-	-	1249	Α
BUK761R8-30C_	_2				© NXP B.V. 200	7. All rights reserved

- [1] Refer to document 9397 750 12572 for further information.
- [2] Continuous current is limited by package.
- [3] Current is limited by chip power dissipation rating.
- [4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.
- [7] Refer to application note AN10273 for further information.

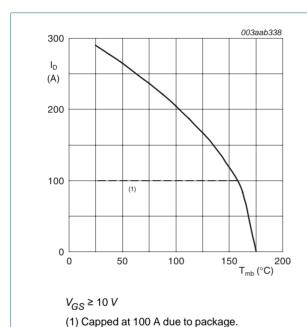


Fig 1. Continuous drain current as a function of mounting base temperature

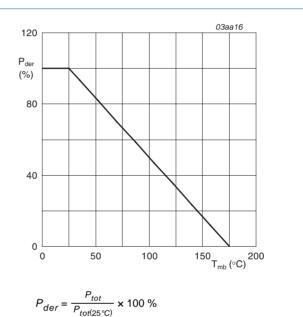
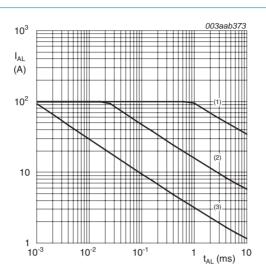
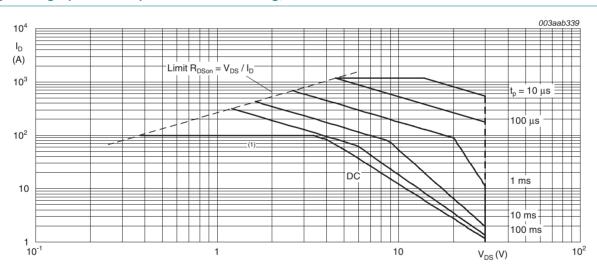


Fig 2. Normalized total power dissipation as a function of mounting base temperature



- (1) Single-pulse;  $T_{mb} = 25$  °C.
- (2) Single-pulse;  $T_{mh} = 150 \, ^{\circ}\text{C}$ .
- (3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



 $T_{mb}$  = 25 °C;  $I_{DM}$  is single pulse

(1) Capped at 100 A due to package.

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

#### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; minimum footprint	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.45	K/W

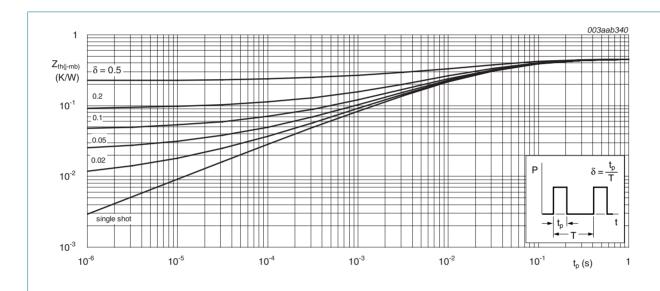


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	racteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V;$ $T_j = 25 °C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V;$ $T_j = -55 ^{\circ}C$	27	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see <u>Figure 10</u>	-	-	4.4	V
·		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 175 °C; see <u>Figure 11</u> and <u>10</u>	1	-	-	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 25 °C; see <u>Figure 11</u> and <u>10</u>	2	3	4	V

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Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$I_{DSS}$	drain leakage current	$V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_{j}$ = 25 $^{\circ}C$	-	0.02	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V};$ $T_j = 175 ^{\circ}\text{C}$	-	-	500	μΑ
$I_{GSS}$	gate leakage current	$V_{DS}$ = 0 V; $V_{GS}$ = 20 V; $T_j$ = 25 °C	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V};$ $T_j = 25 ^{\circ}\text{C}$	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C; see <u>Figure 12</u> and <u>13</u>	-	-	3.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 12 and 13	-	1.5	1.8	mΩ
Source-dr	ain diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 16</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$	-	73	-	ns
$Q_r$	recovered charge	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$	-	48	-	nC
Dynamic o	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V};$ $V_{GS} = 10 \text{ V}; \text{ see } \frac{\text{Figure } 14}{\text{ Figure } 14}$	-	150	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V};$ $V_{GS} = 10 \text{ V}; \text{ see } \frac{\text{Figure } 14}{\text{ Figure } 14}$	-	36	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V};$ $V_{GS} = 10 \text{ V}; \text{ see } \frac{\text{Figure } 14}{\text{ Figure } 14}$	-	52	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V};$ see <u>Figure 14</u>	-	5	-	V
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V};$ $f = 1 \text{ MHz}; T_j = 25 ^{\circ}\text{C};$ $see \underline{Figure 15}$	-	7762	10349	pF
C <sub>oss</sub>	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V};$ $f = 1 \text{ MHz}; T_j = 25 ^{\circ}\text{C};$ see Figure 15	-	1807	2168	pF
C <sub>rss</sub>	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V};$ $f = 1 \text{ MHz}; T_j = 25 ^{\circ}\text{C};$ $see \frac{\text{Figure 15}}{}$	-	996	1365	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 1.2 \Omega;$ $V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \Omega$	-	52	-	ns
t <sub>r</sub>	rise time	$V_{DS}$ = 25 V; $R_L$ = 1.2 $\Omega$ ; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 $\Omega$	-	110	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS}$ = 25 V; $R_L$ = 1.2 $\Omega$ ; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 $\Omega$	-	186	-	ns

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>f</sub>	fall time	$V_{DS}$ = 25 V; $R_L$ = 1.2 $\Omega$ ; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 $\Omega$	-	134	-	ns
L <sub>D</sub>	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nΗ
L <sub>S</sub>	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH

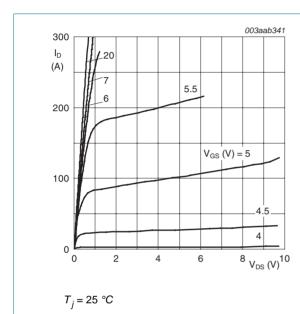
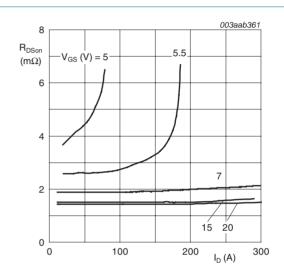


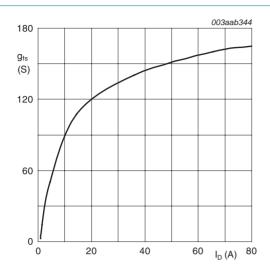
Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_i = 25 \, {}^{\circ}\text{C}$ 

Fig 7. Drain-source on-state resistance as a function of drain current; typical values

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 $T_i = 25 \text{ °C}; V_{DS} = 25 \text{ V}$ 

Fig 8. Forward transconductance as a function of drain current; typical values

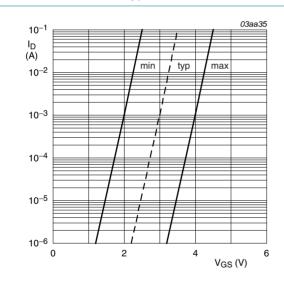
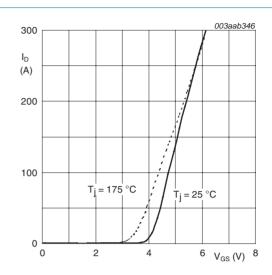


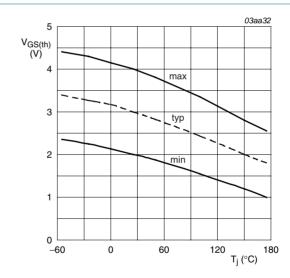
Fig 10. Sub-threshold drain current as a function of gate-source voltage

 $T_i = 25 \, ^{\circ}C; V_{DS} = V_{GS}$ 



$$V_{DS} = 25 V$$

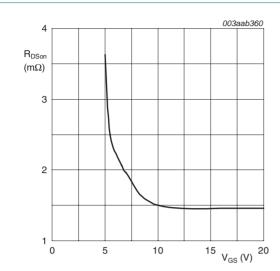
Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $I_D = 1 mA; V_{DS} = V_{GS}$ 

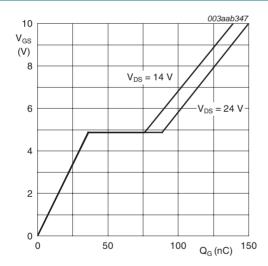
Fig 11. Gate-source threshold voltage as a function of junction temperature

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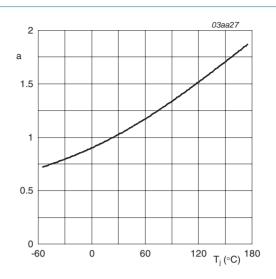
$$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$$

Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values



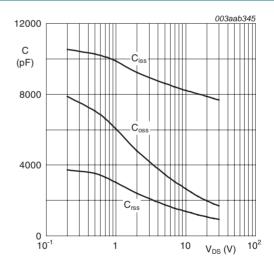
 $T_i = 25 \text{ °C}; I_D = 25 \text{ A}$ 

Fig 14. Gate-source voltage as a function of gate charge; typical values



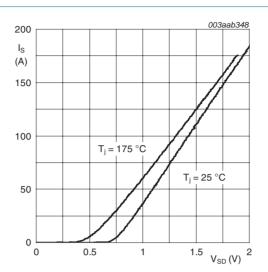
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



 $V_{GS} = 0 V$ ; f = 1 MHz

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



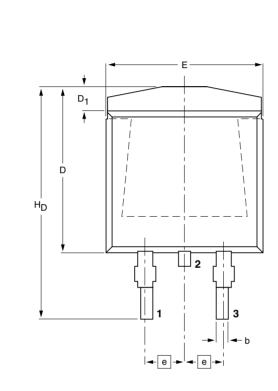
 $V_{GS} = 0 V$ 

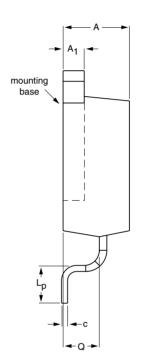
Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

# 7. Package outline

#### Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404** 





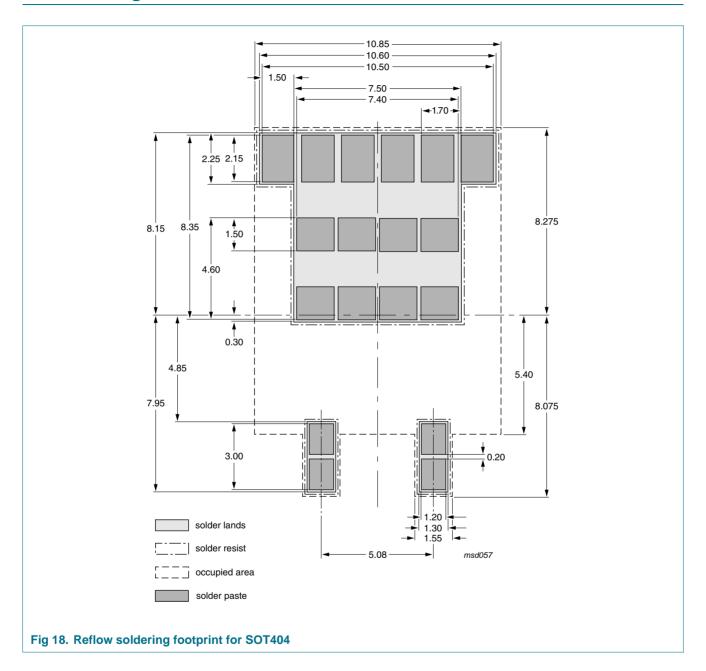
#### DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	С	D max.	D <sub>1</sub>	E	e	L <sub>p</sub>	НД	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT404					<del>-05-02-11</del> -06-03-16

Fig 17. Package outline SOT404 (D2PAK)

## 8. Soldering



**BUK761R8-30C** 

#### N-channel TrenchMOS standard level FET

# 9. Revision history

#### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK761R8-30C_2	20070820	Product data sheet	-	BUK761R8-30C_1
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>			
	<ul> <li>Legal texts</li> </ul>	have been adapted to the	new company name whe	ere appropriate.
BUK761R8-30C_1	20060725	Product data sheet	-	-

### 10. Legal information

#### 10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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