

# PESD3V3X1BL

Ultra low capacitance bidirectional ESD protection diode

Rev. 01 — 6 January 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a leadless ultra small Surface-Mounted Device (SMD) plastic package designed to protect one signal line from the damage caused by ESD and other transients.

### 1.2 Features

- Bidirectional ESD protection of one line
- ESD protection up to 9 kV
- Ultra low diode capacitance:  $C_d = 1.3$  pF
- IEC 61000-4-2; level 4 (ESD)
- Very low leakage current:  $I_{RM} = 1$  nA
- AEC-Q101 qualified

### 1.3 Applications

- USB interfaces
- Cellular handsets and accessories
- Antenna protection
- Portable electronics
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- FireWire
- Computers and peripherals
- High-speed data lines
- Audio and video equipment
- Subscriber Identity Module (SIM) card protection

### 1.4 Quick reference data



Table 1. Quick reference data

$T_{amb} = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per diode</b>						
$V_{RWM}$	reverse standoff voltage		-	-	3.3	V
$C_d$	diode capacitance	$f = 1$ MHz; $V_R = 0$ V	-	1.3	1.6	pF

## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	cathode (diode 1)	 <p>Transparent top view</p>	 <p>006aab041</p>
2	cathode (diode 2)		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PESD3V3X1BL	-	leadless ultra small plastic package; 2 terminals; body 1.0 × 0.6 × 0.5 mm	SOD882

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code
PESD3V3X1BL	SS

## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per device</b>					
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-55	+150	°C
$T_{stg}$	storage temperature		-65	+150	°C

**Table 6. ESD maximum ratings**

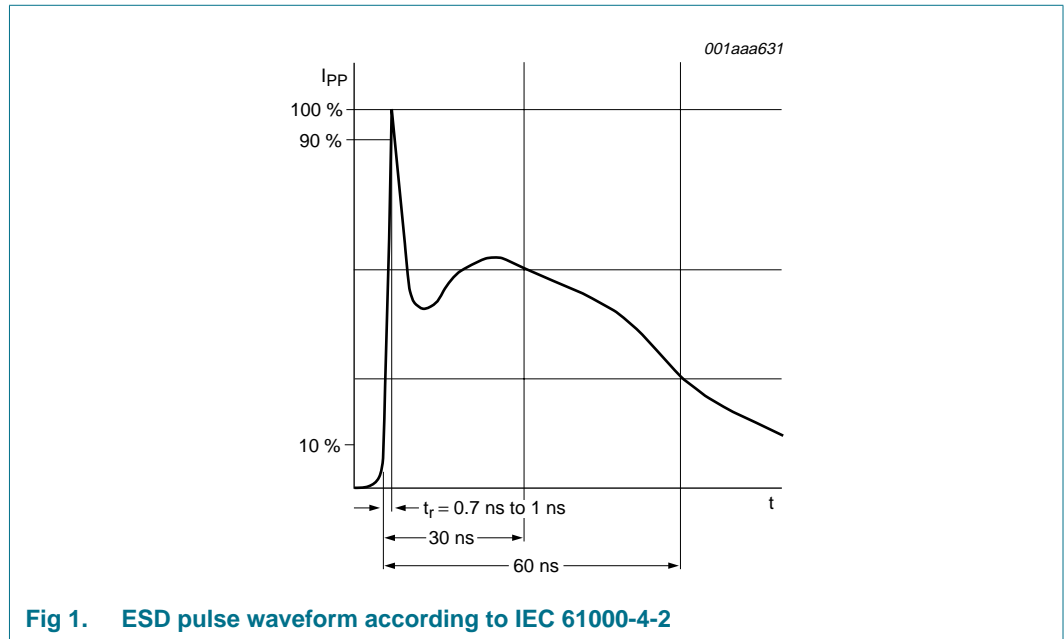
$T_{amb} = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1] -	9	kV
		MIL-STD-883 (human body model)	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

**Table 7. ESD standards compliance**

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV



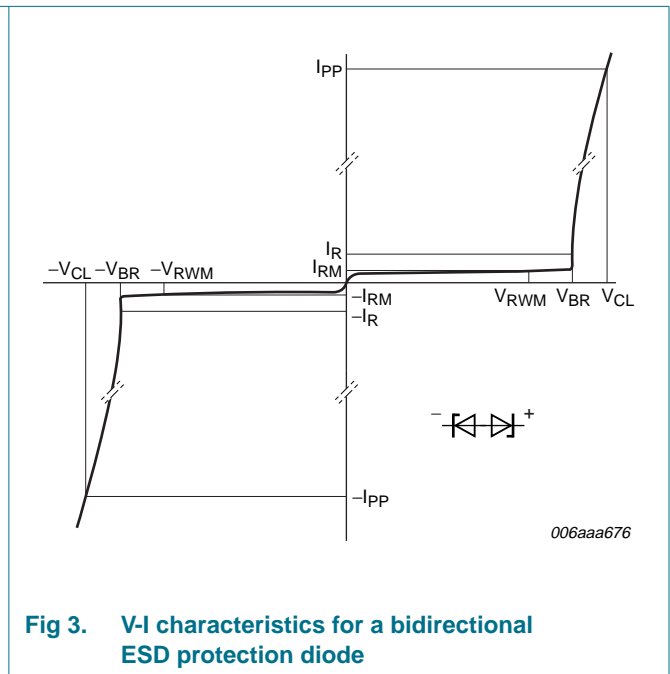
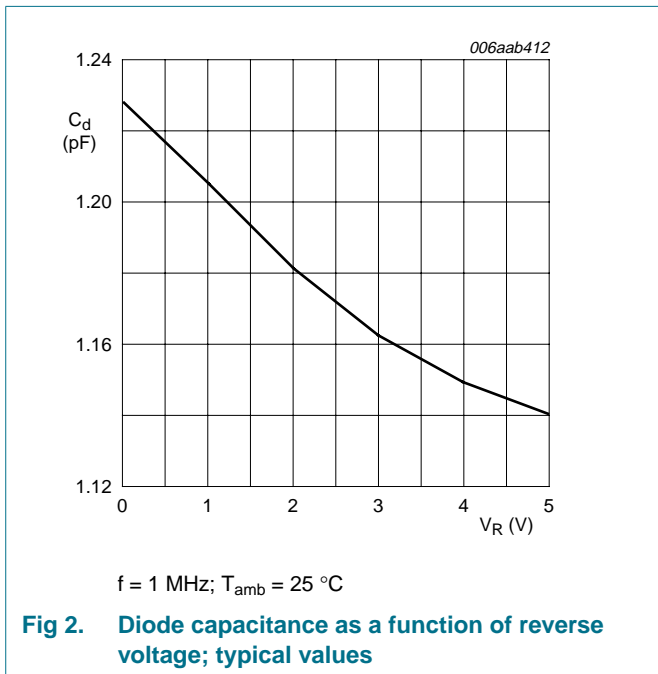
**Fig 1. ESD pulse waveform according to IEC 61000-4-2**

## 6. Characteristics

**Table 8. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per diode</b>						
$V_{RWM}$	reverse standoff voltage		-	-	3.3	V
$I_{RM}$	reverse leakage current	$V_{RWM} = 3\text{ V}$	-	1	100	nA
$V_{BR}$	breakdown voltage	$I_R = 5\text{ mA}$	5.0	6.3	7.8	V
$C_d$	diode capacitance	$f = 1\text{ MHz};$ $V_R = 0\text{ V}$	-	1.3	1.6	pF
$r_{dif}$	differential resistance	$I_R = 5\text{ mA}$	-	-	100	$\Omega$



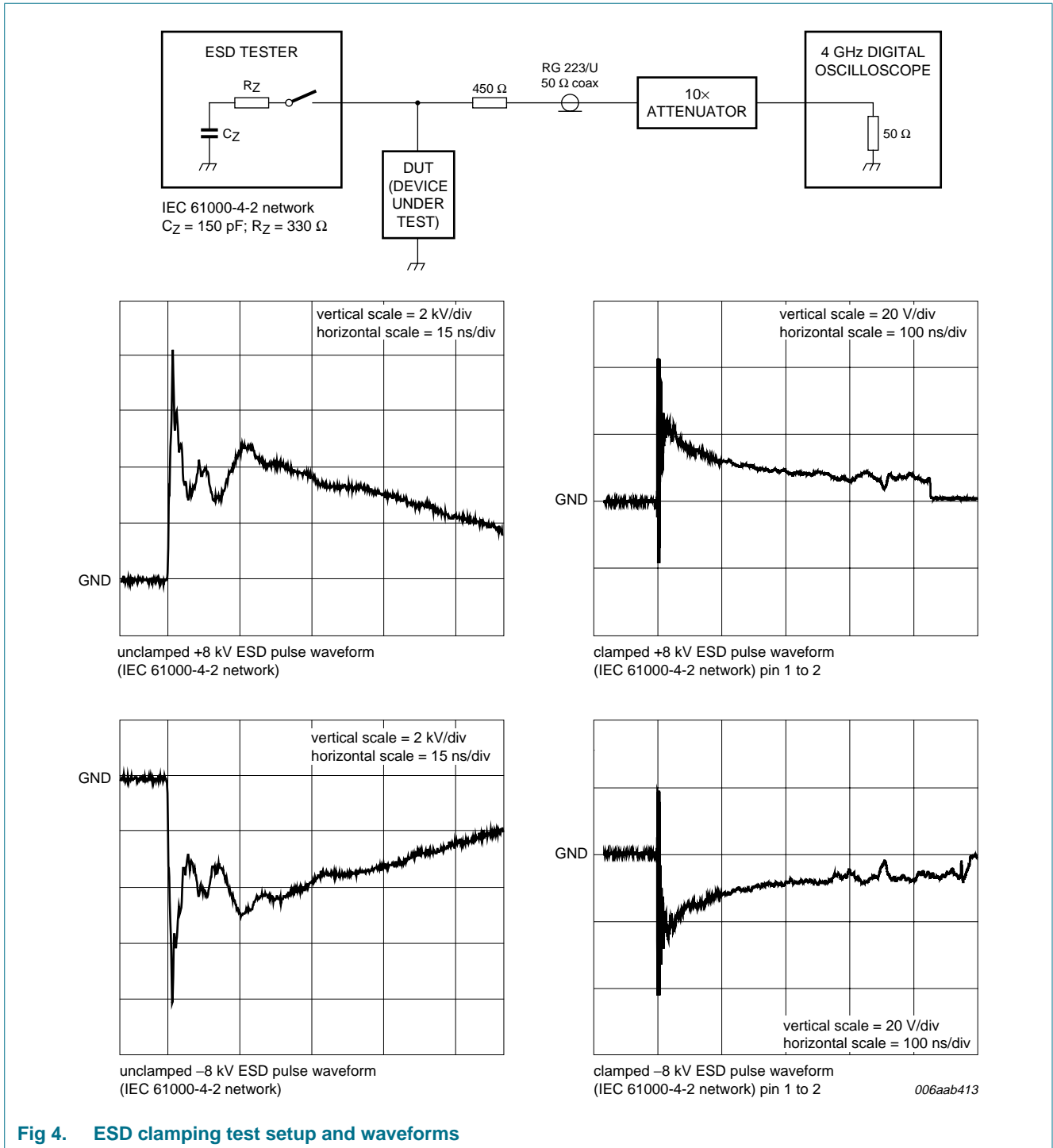


Fig 4. ESD clamping test setup and waveforms

## 7. Application information

The PESD3V3X1BL is designed for the protection of one bidirectional data or signal line from the damage caused by ESD. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground.

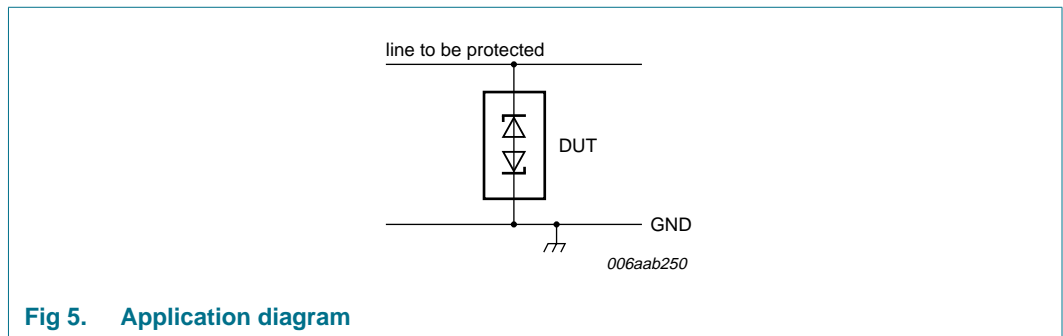


Fig 5. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD and Electrical Fast Transient (EFT). The following guidelines are recommended:

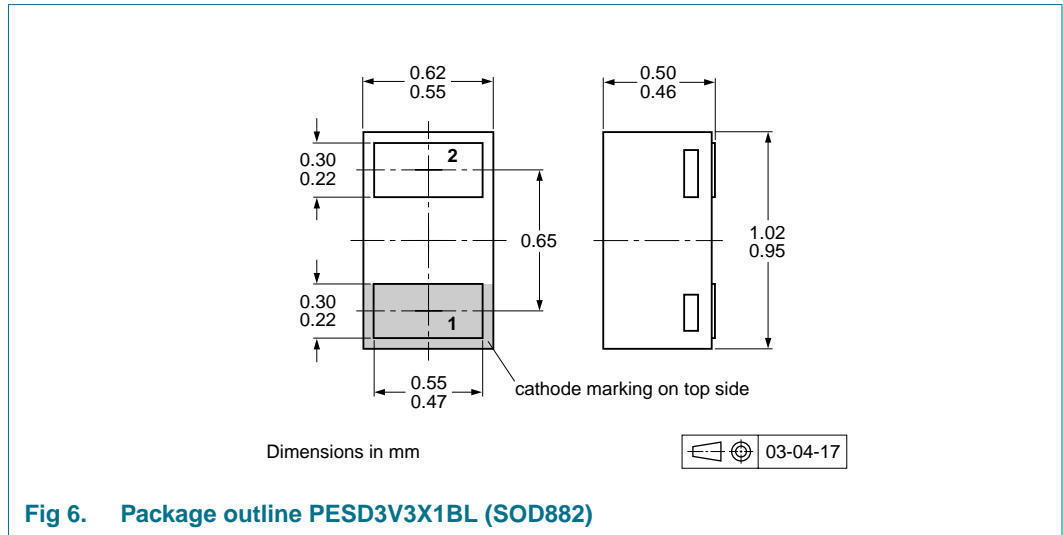
1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

## 8. Test information

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 9. Package outline



## 10. Packing information

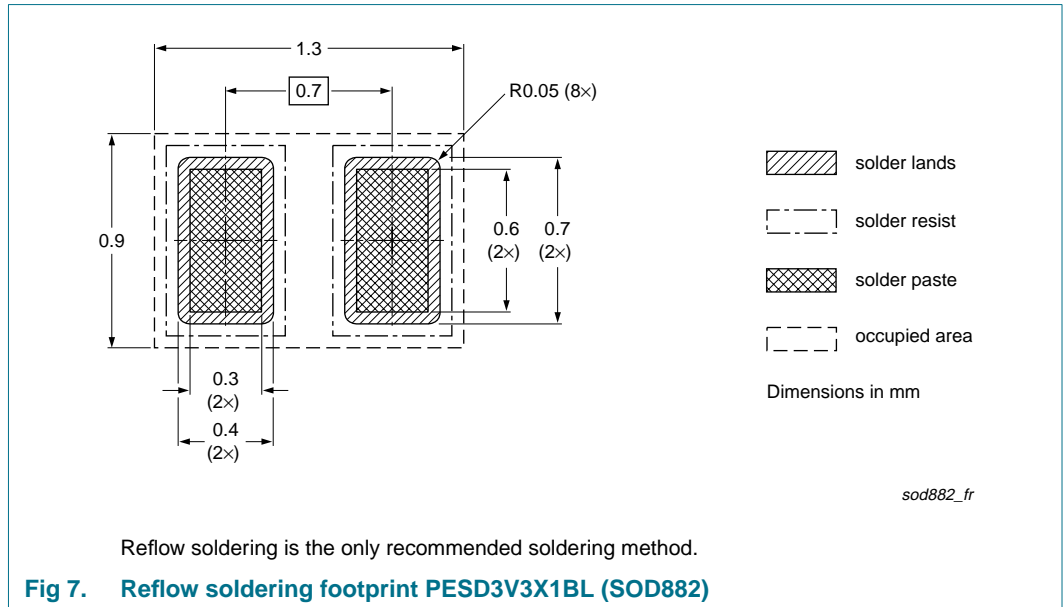
**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity
PESD3V3X1BL	SOD882	2 mm pitch, 8 mm tape and reel	10000
			-315

[1] For further information and the availability of packing methods, see [Section 14](#).

**11. Soldering**





## 12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3X1BL_1	20090106	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 15. Contents

<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	General description .....	1
1.2	Features .....	1
1.3	Applications .....	1
1.4	Quick reference data .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>2</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Marking</b> .....	<b>2</b>
<b>5</b>	<b>Limiting values</b> .....	<b>2</b>
<b>6</b>	<b>Characteristics</b> .....	<b>4</b>
<b>7</b>	<b>Application information</b> .....	<b>6</b>
<b>8</b>	<b>Test information</b> .....	<b>6</b>
8.1	Quality information .....	6
<b>9</b>	<b>Package outline</b> .....	<b>7</b>
<b>10</b>	<b>Packing information</b> .....	<b>7</b>
<b>11</b>	<b>Soldering</b> .....	<b>8</b>
<b>12</b>	<b>Revision history</b> .....	<b>9</b>
<b>13</b>	<b>Legal information</b> .....	<b>10</b>
13.1	Data sheet status .....	10
13.2	Definitions .....	10
13.3	Disclaimers .....	10
13.4	Trademarks .....	10
<b>14</b>	<b>Contact information</b> .....	<b>10</b>
<b>15</b>	<b>Contents</b> .....	<b>11</b>

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