TDF8554J

I²C-bus controlled 4 × 45 W power amplifier and multiple voltage regulator

Rev. 1 — 31 August 2011 Product data sheet

1. General description

The TDF8554J is one of a new generation of complementary quad Bridge-Tied Load (BTL) audio power amplifiers with full I²C-bus controlled diagnostics, multiple voltage regulator and two power switches intended for automotive applications.

The TDF8554J can operate at a battery voltage as low as 6 V making this amplifier suitable for stop/start-car operation. The amplifier uses a complementary DMOS output stage in a Silicon-On-Insulator (SOI)-based BCD process. The DMOS output stage ensures a high power output signal with perfect sound quality. The SOI-based BCD process ensures a robust amplifier, where latch-up cannot occur, with good separation between the four independent channels with every component isolated and without substrate currents.

The multiple voltage regulator comprises four programmable voltage regulators, one standby regulator and two power switches.

The TDF8554J is soft- and hardware downwards-compatible with its predecessor TDA8589XJ.

The TDF8554J includes features, such as selectable undervoltage for stop/start-cars which can be selected with additional I²C-bus instruction bytes. If these additional bytes are not sent, the TDF8554J has the same functionality as its predecessor IPAS TDA8589XJ.

2. Features and benefits

- Amplifier
  - Stop/start-car prepared: keeps operating without audible disturbance during engine start at a battery voltage as low as 6 V
  - I²C-bus mode (3.3 V and 5 V compliant)
  - Can drive 2 Ω or 4 Ω loads
  - Speaker fault detection
  - Start-up diagnostics with load detection: open, short, present; filtered for door-slam and chatter relays
  - AC load (tweeter) detection with low and high current mode
  - Gain select after start-up without audible disturbance
  - Programmable gain (26 dB and 16 dB), independently programmable for the front and rear channels
  - Line driver mode (16 dB and mid-tap voltage $0.25V_P$ for stop/start-cars)
  - Programmable clip detection: 2 %, 5 % or 10 %

- Programmable thermal pre-warning
- If the temperature protection of the regulator is activated, the amplifier is muted before the regulator is switched off
- Loss of ground and open V_P safe (with 150 mΩ series impedance and a maximum supply decoupling capacitor of 2200 μF)
- All amplifier outputs short-circuit proof to ground, supply voltage and across the load (channel independent)
- All pins short-circuit proof to ground
- Temperature-controlled gain reduction to prevent audio holes at high junction temperatures
- Programmable low battery voltage detection to enable 7.5 V or 6 V minimum battery voltage operation
- Overvoltage protection (load-dump safe up to V_P = 50 V) and overvoltage pre-warning at 16 V
- Offset detection

- Multiple regulator
  - Good stability for any regulator with almost any output capacitor
  - Five voltage regulators (microcontroller, display, audio processor, mechanical digital and mechanical drive)
  - I^2C-bus controlled
  - Selectable output voltages for regulators 1, 4 and 5
  - Low dropout voltage PNP output stages
  - High supply voltage ripple rejection
  - Low noise for all regulators
  - Two power switches (antenna switch and amplifier switch)
  - Standby regulator (microcontroller supply) operational during load dump and thermal shut-down
  - Low standby quiescent current (only regulator 2 operational)
  - Backup functionality for regulator 2
- Protection
  - If connection to the battery voltage is reversed, all regulator voltages will be zero
  - Able to withstand output voltages up to 18 V if supply line is short-circuited
  - Thermal protection to avoid thermal breakdown
  - Load-dump protection
  - Regulator outputs protected from DC short-circuit to ground or to supply voltage
  - All regulators protected by foldback current limiting
  - Power switches protected from loss-of-ground

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3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifiers						
$V_{P(oper)}$	operating supply voltage	$R_L = 4\ \Omega$	6	14.4	18	V
I_q	quiescent current	no load	-	260	350	mA
		no load; $V_P = 7$ V	-	190	-	mA
P_o	output power	$R_L = 4\ \Omega$; $V_P = 14.4$ V; maximum power; $V_i = 2$ V RMS square wave	37	40	-	W
		$R_L = 4\ \Omega$; $V_P = 14.4$ V; THD = 0.5 %	18	20	-	W
		$R_L = 4\ \Omega$; $V_P = 14.4$ V; THD = 10 %	23	25	-	W
		$R_L = 2\ \Omega$; $V_P = 14.4$ V; THD = 10 %	40	44	-	W
		$R_L = 2\ \Omega$; $V_P = 14.4$ V; maximum power; $V_i = 2$ V RMS square wave	58	64	-	W
THD	total harmonic distortion	$P_o = 1$ W to 12 W; $f_i = 1$ kHz; $R_L = 4\ \Omega$	-	0.01	0.1	%
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz (6th order); $R_S = 50\ \Omega$				
		amplifier mode	-	40	60	μV
		line driver mode	-	25	33	μV
Voltage regulators						
Supply						
V_P	supply voltage	regulators 1, 3, 4 and 5 on	10.0	14.4	18	V
		regulator 2 on	40	-	-	V
		jump start for t < 10 minutes	-	-	30	V
		load dump protection for $t \leq 50$ ms and $t_r \geq 2.5$ ms	-	-	50	V
		overvoltage for shut-down	20	-	-	V
$I_{q(tot)}$	total quiescent current	standby mode; $V_P = 14.4$ V	-	150	190	μA
Regulator 1						
$V_{O(reg)}$	regulator output voltage	$0.5\text{ mA} \leq I_O \leq 400\text{ mA}$; $12\text{ V} < V_P < 18\text{ V}$; selectable via I²C-bus				
		IB2[D3:D2] = 01	7.9	8.3	8.7	V
		IB2[D3:D2] = 10	8.1	8.5	8.9	V
		IB2[D3:D2] = 11	8.3	8.7	9.1	V
Regulator 2						
$V_{O(reg)}$	regulator output voltage	$0.5\text{ mA} \leq I_O \leq 350\text{ mA}$; $10\text{ V} \leq V_P \leq 18\text{ V}$				
		TDF8554J/N4	3.1	3.3	3.5	V
		TDF8554J/N2	4.75	5.0	5.25	V
Regulator 3						
$V_{O(reg)}$	regulator output voltage	$0.5\text{ mA} \leq I_O \leq 300\text{ mA}$; $10\text{ V} \leq V_P \leq 18\text{ V}$	3.1	3.3	3.5	V

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Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Regulator 4						
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 800 mA; 10 V ≤ V_P ≤ 18 V; selectable via I^{2}C-bus				
		IB2[D7:D5] = 001	4.75	5.0	5.25	V
		IB2[D7:D5] = 010	5.7	6.0	6.3	V
		IB2[D7:D5] = 011	6.6	7.0	7.4	V
		IB2[D7:D5] = 100	8.1	8.6	9.1	V
Regulator 5						
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 400 mA				
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0001	5.7	6.0	6.3	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0010	6.65	7.0	7.37	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0011	7.8	8.2	8.6	V
		10.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0100	8.55	9.0	9.45	V
		11 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0101	9	9.5	10.0	V
		11.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0110	9.5	10	10.5	V
		13 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0111	9.9	10.4	10.9	V
		14.2 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1000	11.8	12.5	13.2	V
		12.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1001	$V_P - 1.0$	-	-	V
Power switches						
V_{do}	dropout voltage	switch 1; I_O = 400 mA	-	0.6	1.1	V
		switch 2; I_O = 400 mA	-	0.6	1.1	V

[1] If the regulator is set to a voltage higher than the supply voltage, the regulator will act as a switch with a voltage drop of 1 V.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDF8554J/N2[1]	DBS37P	plastic DIL-bent-SIL power package; 37 leads (lead length 6.8 mm)	SOT725-1
TDF8554J/N4[2]			

[1] $V_{O(reg2)}$ = 5.0 V

[2] $V_{O(reg2)}$ = 3.3 V

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5. Block diagram

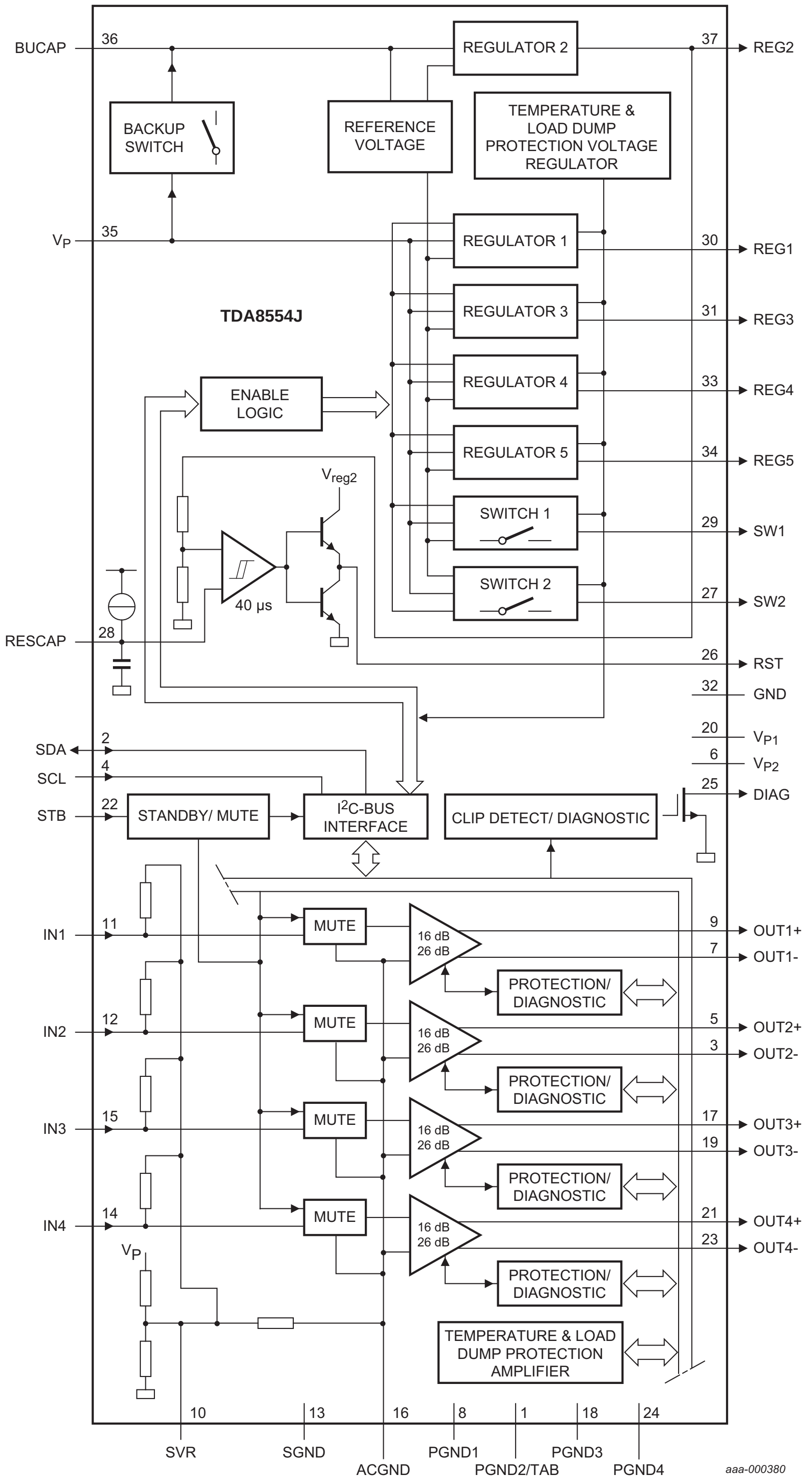

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

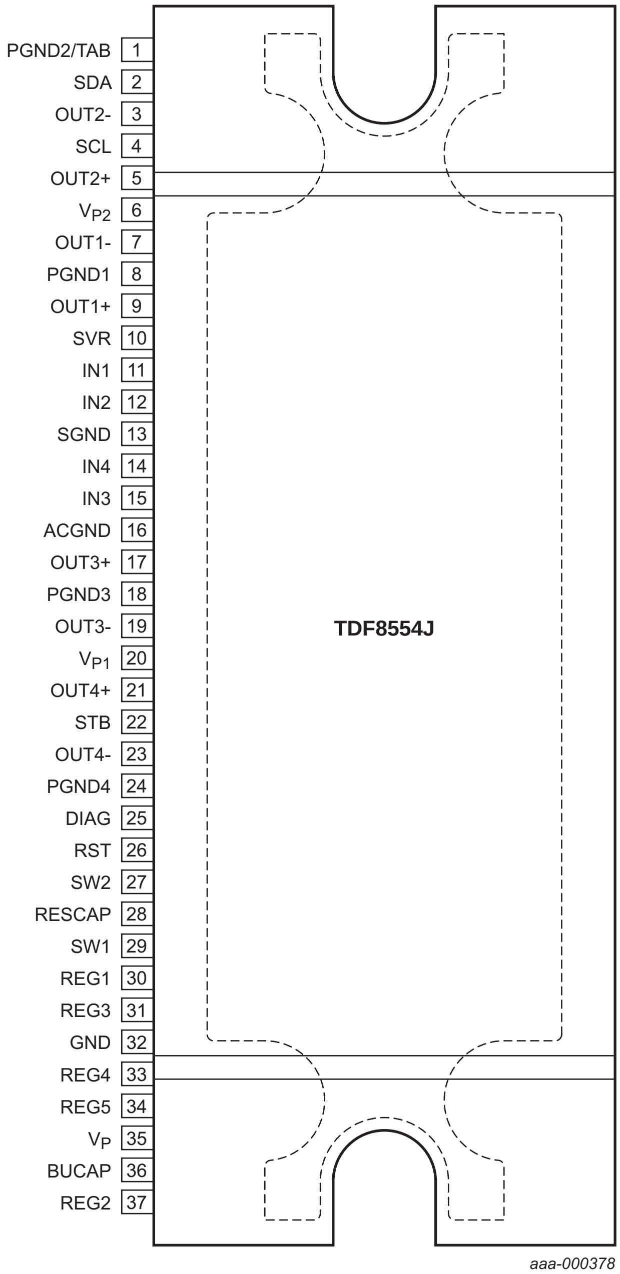

Fig 2. Pin configuration

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6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
PGND2/TAB	1	power ground 2 and connection for heatsink
SDA	2	I^2C-bus data input and output
OUT2–	3	channel 2 negative output
SCL	4	I^2C-bus clock input
OUT2+	5	channel 2 positive output
V_{P2}	6	power supply voltage 2 to amplifiers
OUT1–	7	channel 1 negative output
PGND1	8	power ground 1
OUT1+	9	channel 1 positive output
SVR	10	half supply voltage filter capacitor
IN1	11	channel 1 input
IN2	12	channel 2 input
SGND	13	signal ground
IN4	14	channel 4 input
IN3	15	channel 3 input
ACGND	16	AC ground
OUT3+	17	channel 3 positive output
PGND3	18	power ground 3
OUT3–	19	channel 3 negative output
V_{P1}	20	power supply voltage 1 to amplifiers
OUT4+	21	channel 4 positive output
STB	22	standby or operating mode select input
OUT4–	23	channel 4 negative output
PGND4	24	power ground 4
DIAG	25	diagnostic and clip detection output, active LOW
RST	26	reset output
SW2	27	antenna switch; supplies unregulated voltage to car aerial motor
RESCAP	28	reset delay capacitor
SW1	29	amplifier switch output
REG1	30	regulator 1 output; supply voltage for audio section of radio and CD player
REG3	31	regulator 3 output; supply voltage for signal processor section (mechanical digital) of CD player
GND	32	combined voltage regulator, power and signal ground
REG4	33	regulator 4 output; supply voltage for mechanical section (mechanical drive) of CD player
REG5	34	regulator 5 output; supply voltage for display section of radio and CD player

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Table 3. Pin description *...continued*

Symbol	Pin	Description
V_P	35	power supply to voltage regulators
BUCAP	36	connection for backup capacitor
REG2	37	regulator 2 output; supply voltage to microcontroller

7. Functional description amplifier section

The TDF8554J is a complementary quad Bridge-Tied Load (BTL) audio power amplifier made using SOI-based BCDMOS technology. It contains four independent amplifiers in a BTL configuration. The amplifier remains fully operational at a battery voltage as low as 6 V. Below 6 V a crank detector is activated to shut down the amplifier without audible plops.

The TDF8554J is protected against overvoltage, short-circuit, overtemperature, open ground and open V_P connections.

The diagnostics for temperature and clip levels are programmable via the I^2C-bus. The status of each amplifier can be read separately for output offset, load or no load, short-circuit or speaker falsely connected.

During amplifier start-up, the built-in start-up diagnostic can be used to detect shorted load, open load, short to ground or short to V_P.

The input stage is biased at (0.23 × battery voltage + 1.4 V) and can handle an input voltage of 8 V peak. The DC input bias voltage can be measured on pin SVR. By biasing the voltage on 0.23 × battery voltage + 1.4 V (= 4.7 V at a supply voltage of 14.4 V), the input capacitors can remain biased even with an engine start crank as low as 6 V. If the input capacitors are allowed to discharge quickly, a small (audible) input signal will be generated caused by the difference in input time-constant (different AC ground and input capacitor). This small input signal is amplified to the output and will generate plop noise at the output.

The BCDMOS process with an isolated substrate ensures a robust amplifier (latch-up cannot occur) and low crosstalk between the channels (every component isolated, no substrate currents) resulting in perfect sound quality.

7.1 Start-up and shut-down timing

The capacitor on pin SVR is used for smooth start-up and shut-down which prevents the amplifier from producing switch-on or -off plop noise. Increasing the SVR capacitor value increases start-up and shut-down time.

If the amplifier is switched on in I^2C-bus mode (IB1[D0] = 1), the amplifier output voltage is charged to half the supply voltage.

To enable short start-up times, the 70 kΩ input resistance is reduced to 3 kΩ during start-up until just before the start-up mute release.

During start-up, the amplifier cannot distinguish between a short to ground or a speaker fault. If a speaker fault occurs during start-up, the amplifier enters protection mode and switches off that channel.

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If the amplifier starts, and a speaker fault occurs (double-fault condition: one side of the speaker connected to ground and one side of the speaker connected to one output), the amplifier only sets the speaker fault detection bits.

If the amplifier is switched off by the I²C-bus (IB1[D0] = 0), the soft mute is activated and the capacitor on pin SVR is discharged. If the amplifier is switched off by pulling pin STB LOW, the amplifier is muted (fast mute) and then the capacitor on pin SVR is discharged. This fast mute can be used for instance, when an external engine start detection is used.

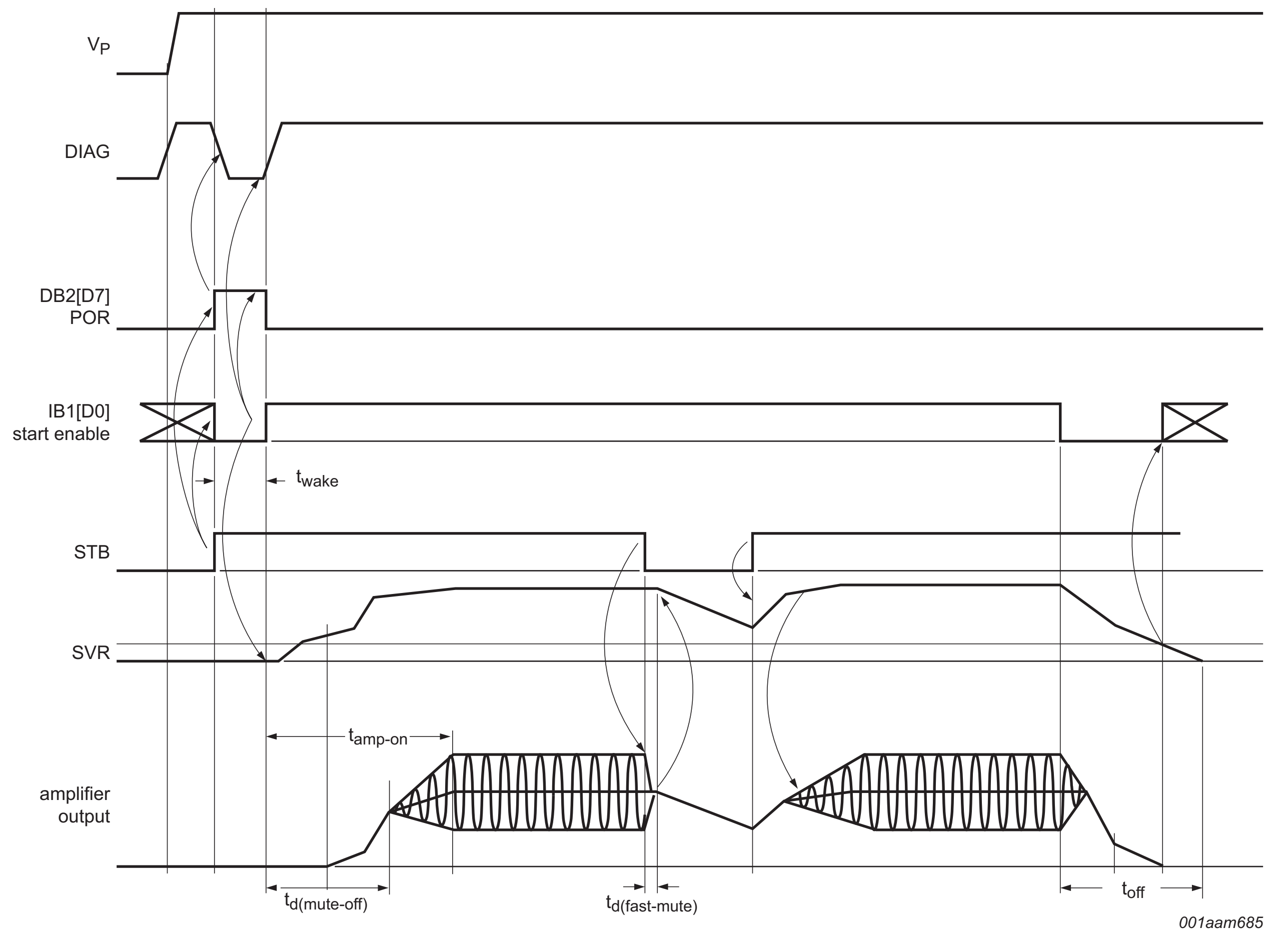

Fig 3. Start-up and shut-down in I²C mode

7.2 Engine start and low voltage operation

The voltage on pin SVR is used as a reference voltage for the input bias (set to 0.23 × battery voltage + 2 × diode voltage V_{be}) and as a reference for generating half the filtered supply voltage at the amplifier output. The capacitor on pin SVR is required for improved supply voltage ripple rejection and channel separation between the four channels.

The DC output voltage relates to the SVR voltage to prevent common mode ripple on the speaker lines. If the supply voltage drops during an engine start, the output will follow slowly due to the SVR capacitor. To create sufficient headroom for the output signal below a battery voltage of 10 V, the DC-output voltage will directly follow half the supply voltage.

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This ensures that at low supply voltage the undistorted output power is maximized. If the battery voltage is above 10 V the DC-output voltage relates to the SVR voltage and is filtered for supply ripple again.

The DC input voltage follows the supply voltage slowly (SVR capacitor) to prevent audible plops, even during engine start.

If the battery voltage drops below 6 V, low V_P mute is activated. During the low V_P mute the amplifier fast mutes (approximately 400 μs). When mute is completed, the capacitor on pin ACGND and on pin SVR are both discharged to prevent audible plops. If the battery voltage rises again above the low V_P mute threshold (6 V), and there has been no Power-On Reset (POR) (DB2[D7]) = 1, the amplifier starts automatically. The amplifier only restarts if the SVR capacitor has been discharged to 0.7 V to prevent a start-up plop. If the battery voltage has dropped too much that the internal registers lose their information, a POR occurs and the amplifier will not restart automatically. Pin DIAG is pulled LOW to indicate a POR has occurred.

The device prevents amplifier plops during engine start. To prevent plops on the amplifier output caused by, for instance, a tuner regulator out of regulation, the voltage on pin STB can be made zero when an engine start is detected. Pin STB activates the fast mute, suppressing disturbances at the amplifier inputs.

The built-in low battery mute voltage default is set to 5.5 V, but can also be set to 7.2 V via the I^2C-bus.

When the low battery voltage mute is set to 7.2 V, the amplifier activates the fast mute (400 μs) and enters the same cycle when the low V_P mute was set to 5.5 V: discharge of the ACGND and SVR capacitors when the mute is completed and start-up when the supply voltage is above 8 V, when no POR has occurred.

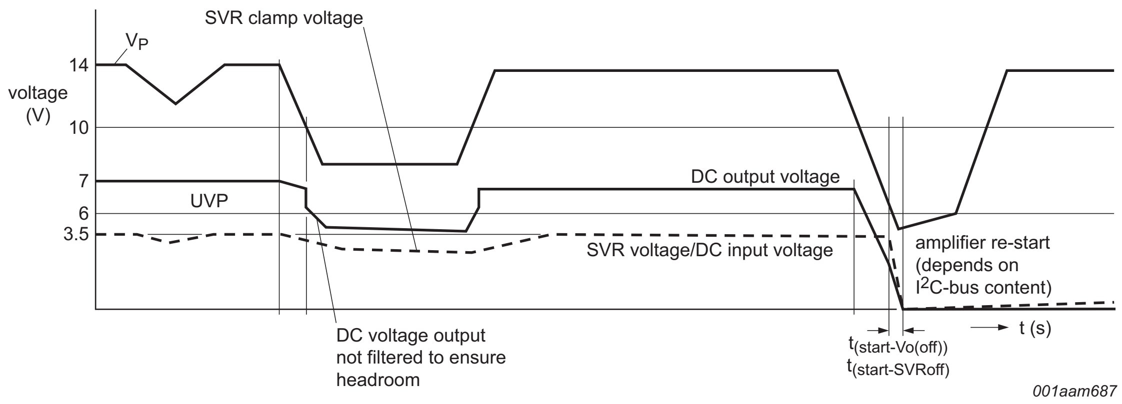

Fig 4. Engine start protection

7.3 POR behavior

If the supply voltage drops below 4.5 V, the content of the I^2C latches cannot be guaranteed and POR is activated at a typical V_P level of 3.1 V. All latches are reset, the amplifier is switched off and pin DIAG is pulled LOW to indicate that a POR has occurred (DB2[D7] = 1). If IB1[D0] is set, the power-on flag is reset, pin DIAG is released and the amplifier starts.

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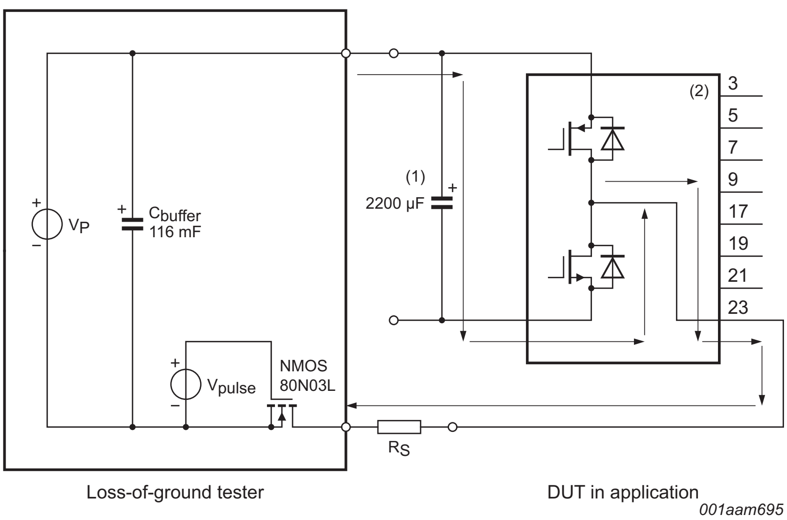
7.4 Protection

7.4.1 Output protection and short-circuit protection

If a short-circuit to ground, V_P or across the load occurs on one or more amplifier outputs, only the amplifier with the short will be switched off. The channel that has a short-circuit and the type of short-circuit can be read via the I^2C-bus. Pin DIAG is pulled LOW to indicate there is a problem. The window protection prevents a restart of the channel with a short to ground or battery. With a short across the load the amplifier is switched on again after 15 ms to check if the short across the load is still present. If the short-circuit conditions are still present, the channel is switched off. If several channels have a short across the load at the same time, the channels are switched on one by one to prevent high supply current switching with four shorts across the load at the same time. The 15 ms cycle reduces power dissipation. To prevent audible distortion, the amplifier channel with the short can be disabled via the I^2C-bus.

7.4.2 Loss-of-ground/loss of V_P failure

Loss-of-ground/loss of V_P is a double-fault condition: the ground (or V_P) wire of the set is not connected and the ground (or V_P) wire is connected to one of the loudspeaker outputs. In this situation the supply capacitor in the set is charged through the body diode of the output power transistor. This body diode (between the drain and the source of the power transistor) is always present in amplifiers with MOS output stages. The capacitor charge current depends on the series impedance of the supply lines, the output impedance of the loss-of-ground tester and the value of the capacitor; see Figure 5. To simulate a worst-case condition, the loss-of-ground tester is equipped with a buffer capacitor of 116 mF to simulate a very low output impedance. With a R_S of 63 mΩ, peak currents of more than 70 A have been measured.



(1) Capacitor value can be 2200 μF to 10000 μF.

(2) Amplifier output stage.

Fig 5. Test circuit for loss-of-ground test

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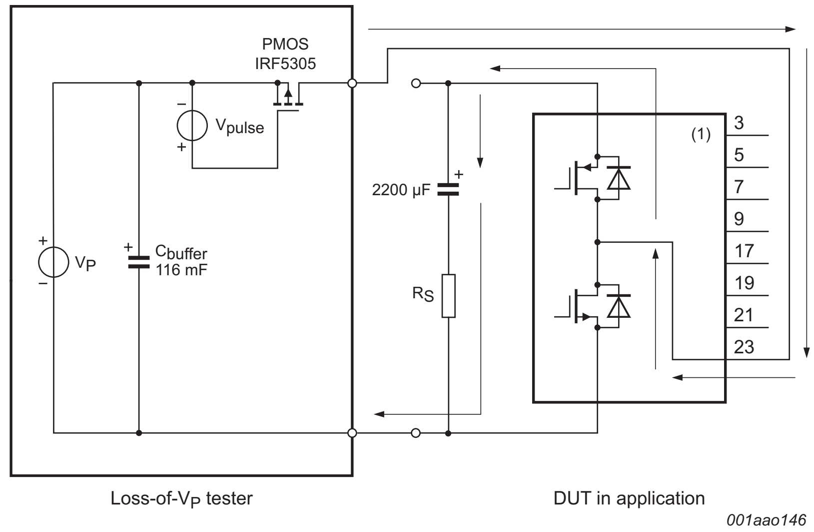

(1) Amplifier output stage.

Fig 6. Test circuit for loss-of-V_P test

7.4.3 Speaker fault detection

There are two protection features available to prevent damage to the speaker if one side of the speaker is connected to ground.

- A check for a speaker fault operates during start-up. This is included in the check for a short to ground; the channel that has the speaker fault is switched off. If the short to ground bit is set, it can mean either a short to ground or a speaker fault. At start-up it is difficult to distinguish between a speaker fault and a short to ground. The amplifier is protected against both, but the speaker fault bit is not always set.
- A check for a speaker fault operates continuously. If a speaker fault is detected and IB5[D3] = 1, bit D3 in registers DB1 to DB4 are set but the amplifier is not switched off and pin DIAG is not pulled LOW.

7.4.4 Overvoltage warning and load dump protection

If the battery voltage V_P exceeds the maximum value of $V_{th(ovp)}$, the device switches off the output stages of the amplifier to protect the output transistors. The overvoltage pre-warning bit is set when the supply voltage level exceeds the value of $V_{P(ovp)pwarn}$.

Although the amplifier switches off the output stages, the device remains operational during load dump conditions (maximum value of V_P at load dump protection; duration 50 ms, rise time > 2.5 ms). The occurrence of the load dump situation can last for a longer time without damaging the device. Provided that the I^2C-bus supply is within the levels specified, communication with the I^2C-bus bus during load dump situations remains possible and the status of the channel outputs can be read.

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7.4.5 Thermal pre-warning and thermal protection

If the average junction temperature reaches one of the adjustable levels set via the I^2C-bus, selected with IB3[D4], pre-warning is activated resulting in pin DIAG LOW (if selected) and can be read via the I^2C-bus. The default setting for the thermal pre-warning is IB3[D4] = 0, setting the warning level at $T_{j(AV)(pwarn)}$ = 160 °C.

If the temperature increases further, the temperature-controlled gain reduction is activated for all four channels to reduce the output power; see Figure 7. If this does not reduce the average junction temperature, all four channels are switched off at the absolute maximum temperature T_{off}.

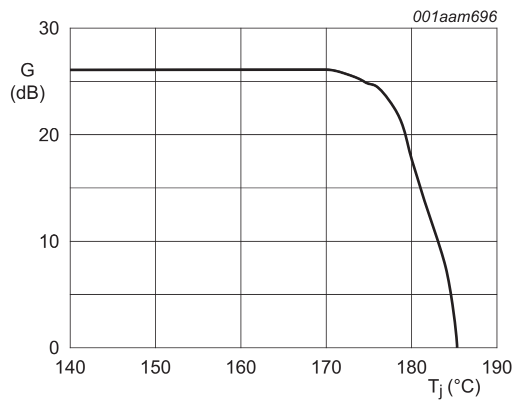

Fig 7. Temperature controlled amplifier gain

7.5 Diagnostics

Diagnostic information can be read via the I^2C-bus, but can also be made available at pin DIAG. This information is seen at pin DIAG as a logical OR. In case of a failure, pin DIAG remains LOW and the microcontroller can read the failure information via the I^2C-bus; pin DIAG can be used as a microcontroller interrupt to minimize I^2C-bus traffic. When the failure is removed, pin DIAG is released.

If the clip information is not needed, it can be removed from pin DIAG, enabling pin DIAG to be used as an interrupt input for the microprocessor.

Table 4. Diagnostic information on pin DIAG

Diagnostic information	Pin DIAG
Power-on reset	after power-on reset; pin DIAG will remain LOW until amplifier has started
Low battery	yes
Clip detection	can be enabled if IB4[D2] = 0
Temperature pre-warning	yes
Short-circuit outputs to battery, ground or across the load	yes
Speaker fault detection	yes
Offset detection	no
Load detection	no

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Table 4. Diagnostic information on pin DIAG

Diagnostic information	Pin DIAG
Overvoltage protection (20 V)	yes
Over voltage pre-warning (16 V)	can be enabled if IB4[D3] = 1
Start-up diagnostic notification	no
Maximum temperature protection active	yes

7.5.1 Start-up diagnostics with DC load detection

If the start-up diagnostics are enabled, the load condition of all four channels is determined. At the end of the start-up diagnostics cycle, not only the load condition is known (shorted load, normal load or open load), but also if a separate amplifier is connected or if the outputs are shorted to battery or ground. If a separate amplifier (booster) is detected, the amplifier can start-up in line driver mode (low gain setting).

The load diagnostic is insensitive to door-slam (slowly moving speaker due to slamming of the car door) and to external interference such as crosstalk of relays switching in the wiring harness; see Figure 8.

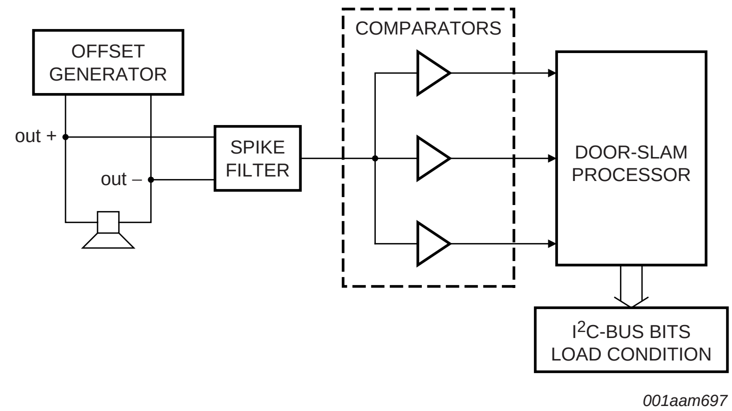

Fig 8. Principle of start-up diagnostics

The load detection values are shown in Figure 9.

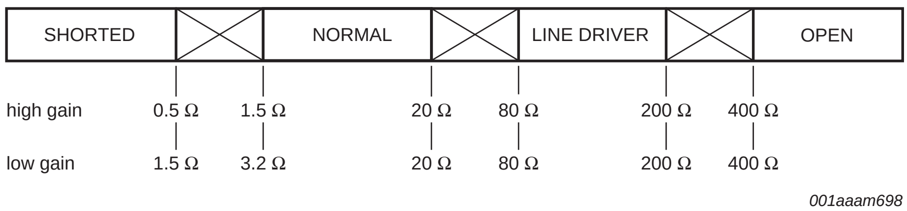

Fig 9. Start-up diagnostics load detection levels

If only 4 Ω speakers are connected, the low gain mode can be selected during the start-up diagnostics. A shorted load is indicated until an impedance of 1.5 Ω is reached. Even ‘soft’ shorts in the wiring harness will be detected.

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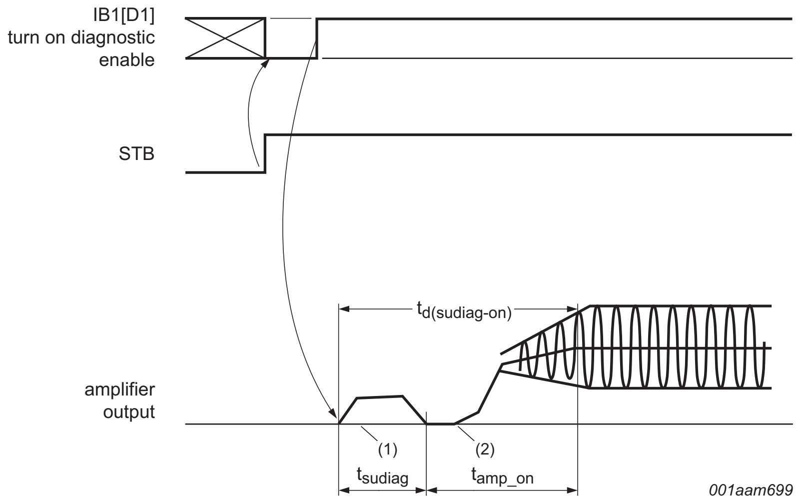

(1) First stage: open load/load/line driver short across the load.

(2) Second stage: amplifier start plus short to ground/V_P speaker fault.

Fig 10. Start-up with start-up diagnostics

In the first stage an offset is generated across the load. To avoid plop-noise, the offset is generated in 15 ms, next the actual load measurement is done. Finally, the offset across the load is reduced again after 15 ms. The complete start-up measurement cycle lasts for t_{sudiag}.

If the voltage of the outputs is more than 3.5 V during the first stage, the start-up diagnostic is switched off to avoid damage to the amplifier. This can happen with a door slam or with a short to V_P. If a short to V_P is applied, the shorted channel will report not valid after the first stage. If only 1 or 2 channels report not valid after the first stage, a short to V_P or of those channels can be assumed. If all 4 channels report not valid, an under- or over-voltage during the start-up diagnostic cycle can be assumed.

The start-up diagnostics has a built-in spike filter to remove disturbances caused by switching relays in the wiring harness or EMC. The door-slam processor filters out disturbances caused when the car door closes: car door-slam can cause the speakers to move slowly which disturbs the measurement. With these filter techniques, reliable load detection is performed in a single start-up diagnostics cycle.

If necessary, the start-up diagnostics can be repeated. Only the first stage, where the speaker load is determined, is sensitive to disturbance and can be repeated. When the start-up diagnostics start, the invalid bits are set, and “the start-up diag busy bit” (bit DB4[D6]) indicates that the start-up diagnostic is not yet completed. When the start-up is completed, or interrupted by a POR, the “start-up diag busy bit” is reset.

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There are two possible situations:

- the start-up diagnostics are enabled (IB1[D1] = 1) and the amplifier start is not enabled (IB1[D0] = 0), bit “start-up diag busy bit” is reset when the start-up diagnostics are completed, and the I^2C-bus data bits are set. Toggling the start-up diagnostics bit re-starts the start-up diagnostics. The invalid bits are set and bit “start-up diag busy bit” indicates that the start-up diagnostics are not completed.
- the start-up diagnostics are enabled (IB1[D1] = 1) and the amplifier start is enabled (IB1[D0] = 1). After the first stage, the amplifier is started and when start-up is completed, just before the start-up mute release (DC output voltage is 1.4 V below midtap voltage), bit “start-up diag busy bit” indicates that the start-up diagnostic is completed. It is not necessary to toggle the start-up diagnostics and has no purpose.

The first and second stages of the start-up diagnostics can be repeated:

Start-up with the start-up diagnostics (IB1[D1] = 1) and the amplifier start enabled (IB1[D0] = 1). Wait until DB4[D6] = 0 which indicates that the start-up diagnostics cycle is completed. Read the start-up diagnostics information. Shut down the amplifier by making the start-up bit logic 0. When DB4[D6] = 0, the amplifier is completely shut down and a new start-up cycle can be programmed.

Table 5. Start-up diagnostics I^2C-bus bits

DC load bits[1]		Meaning
DBx[D5]	DBx[D4]	
0	0	normal load
0	1	line driver mode
1	0	open load
1	1	invalid: overvoltage or undervoltage (V_P < 10 V) has occurred, or start-up diagnostics not completed, or channel has short to V_P; indicated in second stage

[1] DBx[D3] indicates a shorted load; DBx[D1] indicates a short to V_P; DBx[D0] indicates a short to ground. When set, D4, D5 have no meaning.

If during the start-up diagnostics an engine start occurs, the generated offset to measure the DC load is reduced and the start-up diagnostics cannot be performed correctly. In this case the invalid combination DBx[D4:D5] = 11 is set.

The start-up diagnostics information in the I^2C-bus bits is combined with the AC load detection allowing the start-up diagnostics information to be read when IB4[D0] = 1 (the advanced load detection is enabled). If IB4[D0] = 0, only normal and not normal loads can be detected.

Remark: the shorted load, and short to V_P or ground information from the start-up diagnostics is cleared after an I^2C-bus read. Bits DBx[D5] and DBx[D4] indicate the real situation: when the short is removed, the bits are cleared. The DBx[D5] and DBx[D4] information, generated at start-up, is refreshed after a new start-up diagnostics cycle.

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7.5.2 DC offset detection

The offset detection can be performed with no input signal (for instance when the DSP is muted after a start-up) or with an input signal. An I^{2}C-bus read of the output offset is performed, the I^{2}C-bus latches of DBx[D2] are set. If the amplifier BTL output voltage is within a window with a threshold of 1.3 V (typical), the latches of DBx[D2] are reset and the setting is disabled. If for example, after 1 s another I^{2}C-bus read is performed and the offset bits are still set, the output did not cross the offset threshold during the last 1 s; see Figure 11. This can mean either a frequency below 1 Hz was applied (1 s I^{2}C-bus read interval) or an output offset of more than 1.3 V is present.

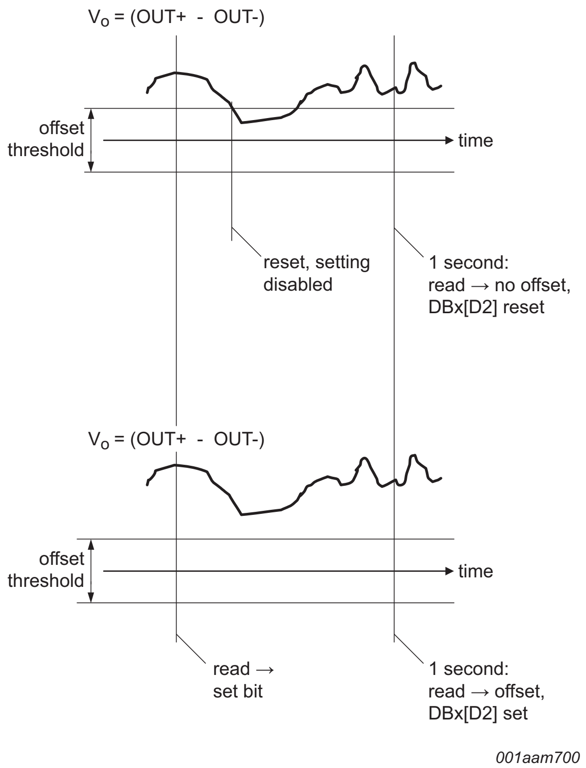

Fig 11. Offset detection

7.5.3 AC load detection

The AC load detection, set with IB1[D1] = 1, is used to detect if AC-coupled speakers such as tweeters are connected correctly. The detection requires a 19 kHz sine wave to be applied to the inputs of the amplifier. A high current AC-load detection mode can be selected, for example during car assembly, or a low current AC-load detection mode, for example during switch on of car radio. The output voltage over the load impedance generates an amplifier current. If the amplifier peak current exceeds a 500 mA (peak) threshold (or 275 mA peak in low current mode) four times, the AC-load detection bit is set. The 4 ‘threshold cross’ counter is used to prevent false AC-load detection caused by switching the input signal on or off.

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An AC-coupled speaker reduces the impedance at the output of the amplifier in a certain frequency band. The presence of an AC-coupled speaker can be determined using a high current mode (IB4[D5] = 0, see Figure 12) or using a low current detection mode (IB4[D5] = 1; see Figure 13).

If for instance a 19 kHz input signal is generated with a peak output voltage of 2 V the I^{2}C-bus bits are guaranteed to be set with a (total AC + DC) load less than 4 Ω and are guaranteed not set with a load of more than 9 Ω.

When IB1[D1] = 1 the AC-load detection measurement cycle is enabled, the peak counter is reset and the measuring cycle starts. The AC-load detection can only be performed after the amplifier has completed its start-up cycle. Since the AC-load information in the I^{2}C-bus bits is combined with the start-up diagnostics, the AC-load information can be read when IB4[D0] = 0. If IB4[D0] = 1, the stored AC-load bits cannot be read, but their values are preserved.

The interpretation of the line driver and amplifier mode DC load bit for AC load detection is shown in Table 6.

Table 6. AC load detection

IB4[D0] = 0	DB1 to 4 [D4] (AC load bit)
No AC load detected	0
AC load detected	1

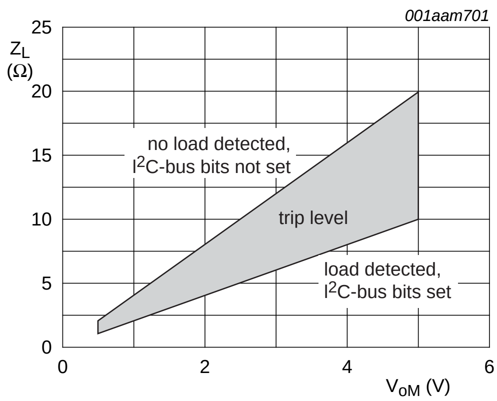

Fig 12. AC-load impedance as a function of peak output voltage (high current AC-load detection)

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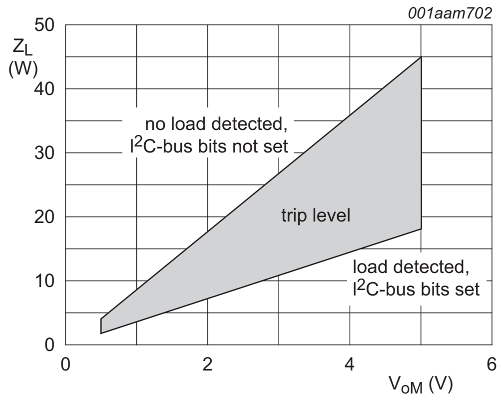

Fig 13. AC-load impedance as a function of peak output voltage (low current AC-load detection)

7.5.4 Distortion (clip-) detection

If the amplifier output clips to the supply voltage or ground, the output signal becomes distorted. If the distortion per channel exceeds a selectable threshold (2 %, 5 % or 10 %), pin DIAG is activated.

The clip detection level can be programmed via the I^2C-bus. The clip information is blocked below a supply voltage of 10 V to avoid false clip detection during engine start, or can be programmed to operate at the low voltage detection level of 7.2 V or 5.5 V.

Since it is possible to have different amplifier gain settings between the front and rear channels and there is only one clip reference current, the clip detect levels are only accurate for the channels with the highest gain. In line driver mode the DC-output voltage is 0.24V_P and clip detection will still indicate a clip, but the levels will not be accurate.

7.6 Line driver mode and low gain mode

The TDF8554J amplifier can be used as a line driver or as a low gain amplifier. In both situations, the gain needs to be set to 16 dB via I^2C-bus (IB3[D5:D6]) and can be independently set for front channels (1 and 3) and rear channels (2 and 4). The main difference between the line driver mode and low gain mode is the DC-output voltage.

In line driver mode the TDF8554J can be used to drive a separate amplifier or booster. In this mode the DC output voltage is set to 0.23 × battery voltage and is filtered with the capacitor connected to pin SVR (V_{SVR}). The reason to not set the DC output voltage to half the battery voltage is to allow engine starts at a battery voltage as low as 6 V. The DC output voltage remains approximately 3 V during engine start. If the DC output voltage is set to half the battery voltage, with an engine start the common mode voltage will change quickly from 7 V to 3 V. This drives the input stage of the booster below the ground level.

If the TDF8554J amplifier is used as a low gain amplifier in a booster, the DC output voltage is set to half of the supply voltage to ensure maximum undistorted output power.

The line driver and low gain modes can be selected with I^2C-bus IB4[D4].

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Table 7. DC output voltage as a function of different gain settings

Channels 1 and 3 gain setting (dB)	Channels 2 and 4 gain setting (dB)	Line driver/low gain mode IB4[D4][1]	All channels DC output voltage (V)
26	26	X	$0.5V_P$
16	26	X	$0.5V_P$
26	16	X	$0.5V_P$
16	16	low gain mode	$0.5V_P$
16	16	line driver mode	$0.23V_P$

[1] X = neither mode selected.

7.7 I²C-bus

If pin STB is LOW, the total quiescent current is low, and the I²C-bus lines are not loaded. When pin STB is switched HIGH, the TDF8554J enters operating mode and performs a POR which results in pin DIAG going LOW. The TDF8554J starts when IB1[D0] = 1. Bit D0 also resets the 'power-on reset occurred' bit (DB2[D7]) and releases pin DIAG.

Soft mute and hard mute can be activated via the I²C-bus. Soft mute can be activated independently for the front channels (1 and 3) and rear channels (2 and 4), and mutes the audio in 15 ms. Hard mute activates the mute for all channels at the same time and mutes the audio in 400 μs. Unmuting after a hard mute will be a soft unmute of approximately 15 ms. When pin STB is switched to standby mode, and the amplifier has started, first the hard mute is activated and then the amplifier shuts down. It is possible to fully mute the amplifiers within 400 μs by making pin STB LOW, for example during an engine start.

7.8 I²C-bus diagnostic bits read out/cleared after read

The amplifier's diagnostic information can be read via the I²C-bus. The I²C-bus bits are set on a failure and will be reset with the I²C-bus read command (clear after read). Even when the failure is removed the microprocessor will know what was wrong by reading the I²C-bus. Old information is read during an I²C-bus read. Most up-to-date information is read after two consecutive read commands.

Cleared after read means that the I²C-bus bits are cleared after a read command. The Clear command is done only if all four data bytes are read. If only three data bytes are read, the I²C-bus latches are not cleared and the old value remains in the latches.

When selected, pin DIAG will give up-to-date diagnostic information. When a failure is removed, pin DIAG will be released instantly, independently of the I²C-bus latches.

8. Functional description voltage regulator section

The voltage regulator section contains:

- Four switchable regulators and one permanent active regulator
- Two power switches with loss-of-ground protection
- Reset push-pull output
- Backup functionality

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The quiescent current has a very low level of 150 μA (typical value) with only regulator 2 active. Due to the low voltage operation of the application, low dropout voltage regulators are used.

All the regulators, except for the standby regulator, can be controlled by the I^{2}C-bus. The device has in addition to the regulators, two I^{2}C-controlled power switches which are capable of delivering 400 mA continuous current. This device has several fail-safe protection modes. This module conforms to peak transient tests and protects against high continuous voltage (24 V), short-circuits and thermal stress. The standby regulator will maintain output as long as possible even in thermal shutdown or any other fault condition. During overvoltage stress, all outputs except regulator 2 will shut off and the device is able to supply a minimum current for an indefinite amount of time allowing sustained memory for a microprocessor. Also, there is a provision for use of a reserve supply capacitor that will hold enough energy for regulator 2 to allow a microprocessor to prepare for loss of voltage.

8.1 Standby regulator output

Regulator 2 is intended as a supply for a microcontroller. It has a low quiescent current and cannot be switched. This regulator will not shut down with the switched regulators and cannot be controlled by the I^{2}C-bus. This regulator will not shut down during load dump transients or high temperature protection.

8.2 Backup capacitor

The backup capacitor (C_{backup}) is used as a backup supply for the regulator 2 output when the battery supply voltage (V_P) cannot support the regulator 2 voltage.

8.3 Backup function

A backup function is implemented by a switch which behaves like an ideal diode between pins V_P and BUCAP. The forward voltage of this ideal diode depends on the current flowing through it. This function allows regulator 2 to be supplied during brief periods when no supply voltage is present on pin V_P. It requires an external capacitor connected to pin BUCAP and ground. When the supply voltage is present on pin V_P this capacitor will be charged to a level of V_P – 0.3 V. This charge can now be used to supply regulator 2 when V_P is absent for a short time.

The delay time (t_{delay}) can be calculated using Equation 1:

$$t_{delay} = C_{backup} \times R_L \times \left(\frac{V_P - (V_{REG2} - 0.5)}{V_{REG2}}\right) \quad (1)$$

Example: V_P = 14.4 V, V_{REG2} (voltage on pin REG2) = 5.0 V (N2) or 3.3 V (N4), R_L = 1 kΩ and C_{backup} = 100 μF providing a t_{delay} of 178 ms (N2) or 321 ms (N4).

When an overvoltage condition occurs, the voltage on pin BUCAP is limited to approximately 24 V.

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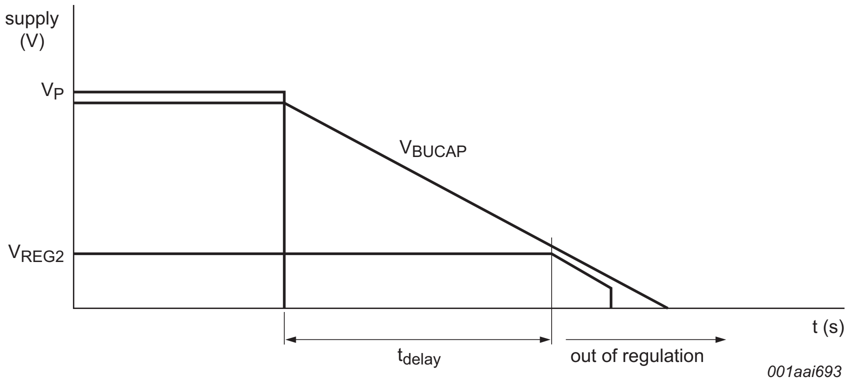

Fig 14. Backup capacitor function

8.4 Reset output

A reset pulse is generated at pin RST when the output voltage of regulator 2 rises above the reset threshold value. The reset output is a push-pull output that both sources and sinks current. The output voltage can switch between ground and $V_{O(REG2)}$, and operates at a low regulator 2 voltage or V_{BUCAP}. The RST signal is controlled by a low-voltage detection circuit which, when activated, pulls pin RST LOW (reset active) when $V_{O(REG2)}$ is $\leq V_{th(rst)}$. If $V_{O(REG2)} \geq V_{th(rst)}$, pin RST goes HIGH. The reset pulse is delayed by 40 μs internally. To extend the delay and to prevent oscillations occurring at the threshold voltage, an external capacitor can be connected to pin RESCAP. Note that a reset pulse is not generated when $V_{O(REG2)}$ falls below the reset threshold value.

8.5 Reset delay capacitor

A Reset Delay Capacitor (RDC) connected to pin RESCAP can be used to extend the delay period of the reset pulse and to ensure that a clean reset signal is sent to the microcontroller. The RDC is charged by a current source. The reset output (pin RST) will be released (pin RST goes HIGH) when the RDC voltage crosses the RDC threshold value.

8.6 Power switches

There are two power switches that provide an unregulated DC voltage output for amplifiers and an aerial motor respectively. The switches have internal protection for overtemperature conditions and are activated by setting bits IB1[D2] and IB1[D3] to logic 1.

In the ON state, the switches have a low impedance to the battery voltage. When the battery voltage is higher than 22 V, the switches are switched off. When the battery voltage is below 22 V the switches are set to their original condition.

The power switches have built-in surge protection to be able to absorb energy from switching inductive or capacitive external loads. This surge protection is implemented in such a way that in case no supply (V_P) is present, the supply line will not be charged from a possible external source connected to a power switch output.

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8.7 Protection

All regulator and switch outputs are fully protected against load dump and short-circuit (foldback current protection); see Figure 15. At load dump, all regulator outputs, except the output of regulator 2, will go LOW. The power switches can withstand 'loss of ground' which means that pin GND is disconnected and the switch output is connected to ground.

8.8 Temperature protection

The amplifier is switched off when the regulator junction temperature becomes too high to prevent undefined audio signals when the regulators are switched off while the amplifier is still on. A regulator junction temperature that is too high is indicated by pin DIAG and can be read out via the I²C-bus DB2[D6].

If the junction temperature still increases and the regulator reaches the maximum temperature protection level, all regulators and switches will be disabled except the outputs of regulator 2.

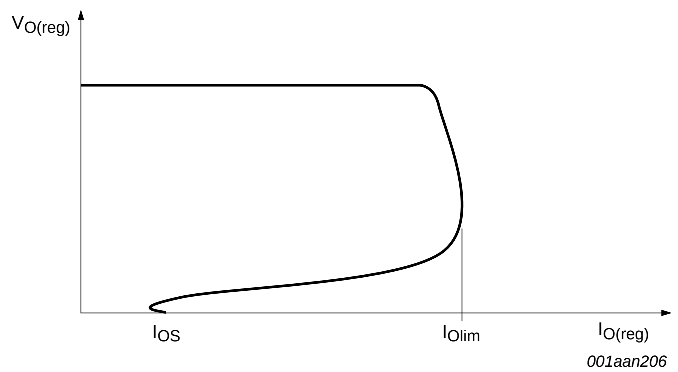

Fig 15. Foldback current protection

8.9 Switched regulator outputs

Switched outputs (regulator 1, 3, 4 and 5) can be programmed by the I²C-bus and have an internal protection for overtemperature conditions. The regulated outputs, supplying pulsed current loads, will contaminate the line with high frequency noise, so it is important to prevent any cross-coupling between the regulated outputs, particularly with the 8.3 V supply for audio.

9. I²C-bus specification

Table 8. TDF8554J hardware address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$	Hex
1	1	0	1	1	0	0	0 = write to TDF8554J; 1 = read from TDF8554J	D8

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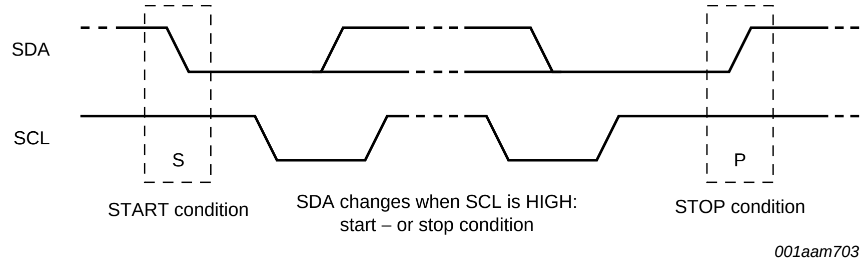

Fig 16. Definition of START and STOP conditions

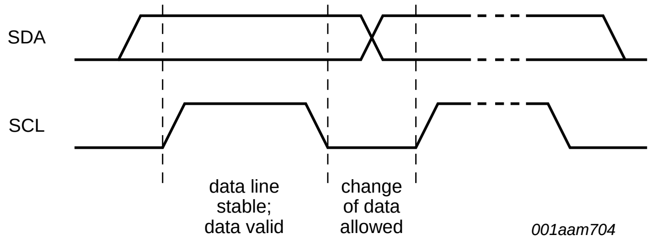

Fig 17. Bit transfer

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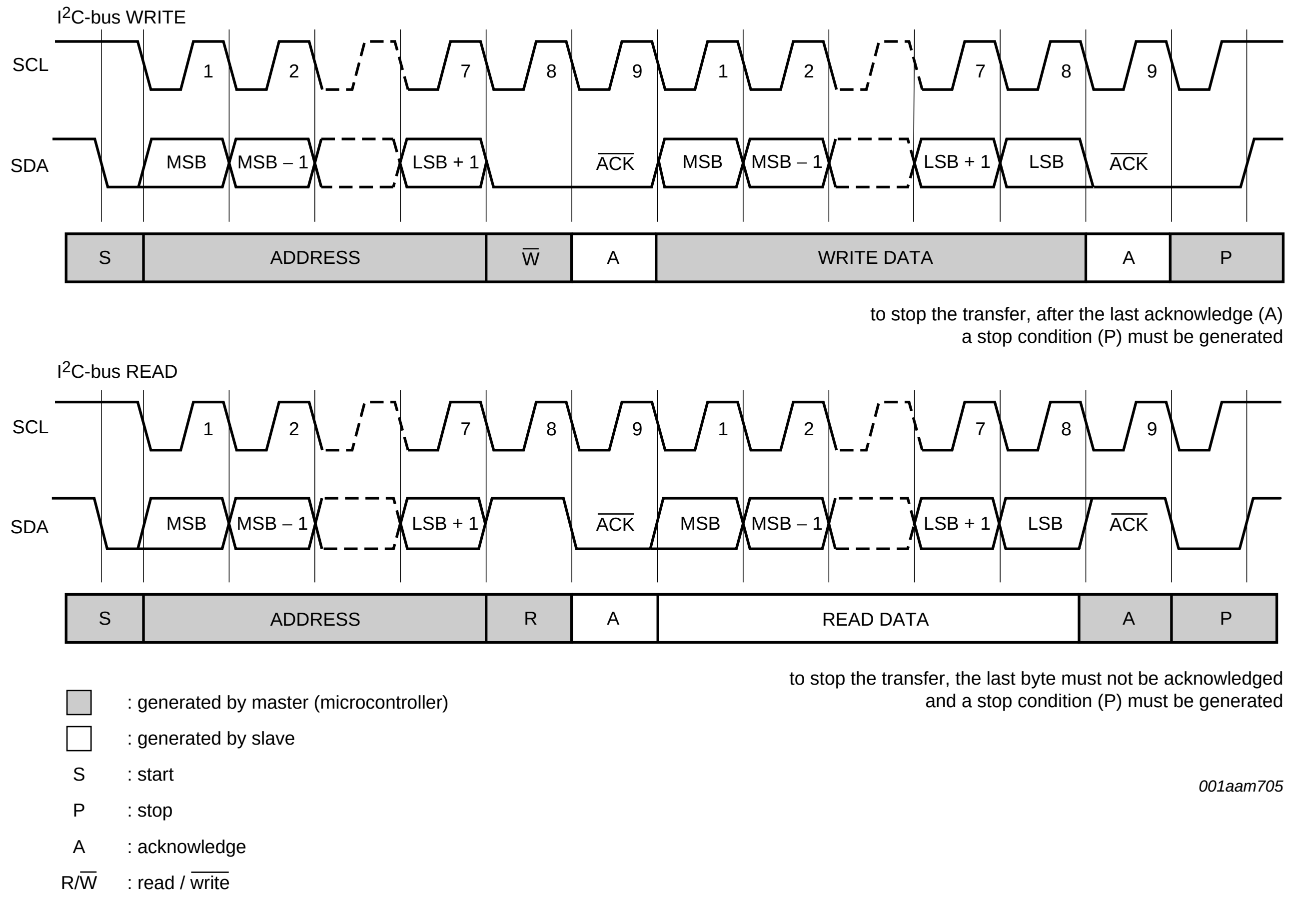

Fig 18. I²C-bus read and write modes

9.1 I²C-bus instruction bytes

I²C-bus mode:

- If R/$\overline{\text{W}}$ bit = 0, the TDF8554J expects five instruction bytes; IB1, IB2, IB3, IB4, IB5
- After a power-on reset, all instruction bits are set to zero

Table 9. Instruction byte IB1 bit description

Bit	Symbol	Description
7	D7	regulator 5 (display) output voltage control; see Table 10
6	D6	
5	D5	
4	D4	
3	D3	SW2 control
		0 = SW2 off
		1 = SW2 on
2	D2	SW1 control
		0 = SW1 off
		1 = SW1 on

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Table 9. Instruction byte IB1 bit description *...continued*

Bit	Symbol	Description
1	D1	enable or disable AC/DC-load detection/start-up diagnostic
		0 = AC-load or DC-load detection off/start-up diagnostic disabled
		1 = AC-load or DC-load detection on/start-up diagnostic enabled
0	D0	enable or disable amplifier start
		0 = amplifier off; pin DIAG remains LOW
		1 = amplifier on; when power-on occurs, DB2[D7] is reset and pin DIAG is released

Table 10. Regulator 5 (display) output voltage control

Bit				Output (V)
D7	D6	D5	D4	
0	0	0	0	0 (off)
0	0	0	1	6.0
0	0	1	0	7.0
0	0	1	1	8.2
0	1	0	0	9.0
0	1	0	1	9.5
0	1	1	0	10.0
0	1	1	1	10.4
1	0	0	0	12.5
1	0	0	1	$\leq V_P - 0.5$ (switch)
1	0	1	0	-
1	0	1	1	-
1	1	0	0	-
1	1	0	1	-
1	1	1	0	-
1	1	1	1	-

Table 11. Instruction byte IB2 bit description

Bit	Symbol	Description
7	D7	regulator 4 (mechanical drive) output voltage control; see Table 12
6	D6	
5	D5	
4	D4	regulator 3 (mechanical digital) control
		0 = regulator 3 off
		1 = regulator 3 on
3	D3	regulator 1 (audio) control; see Table 13
2	D2	
1	D1	enable or disable soft mute all amplifier channels
		0 = soft mute off
		1 = soft mute on

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Table 11. Instruction byte IB2 bit description *...continued*

Bit	Symbol	Description
0	D0	enable or disable fast mute all amplifier channels
		0 = fast mute off
		1 = fast mute on

Table 12. Regulator 4 (mechanical drive) output voltage control

Bit			Output (V)
D7	D6	D5	
0	0	0	0 (off)
0	0	1	5.0
0	1	0	6.0
0	1	1	7.0
1	0	0	8.6
1	0	1	-
1	1	0	-
1	1	1	-

Table 13. Regulator 1 (audio) output voltage control

Bit		Output (V)
D3	D2	
0	0	0 (off)
0	1	8.3
1	0	8.5
1	1	8.7

Table 14. Instruction byte IB3 bit description

Bit	Symbol	Description
7	D7	clip detection level (can be overruled by IB4[D7])
		0 = 5 % detection level
		1 = 2 % detection level
6	D6	front channels 1 and 3 gain select
		0 = 26 dB gain
		1 = 16 dB gain
5	D5	rear channels 2 and 4 gain select
		0 = 26 dB gain
		1 = 16 dB gain
4	D4	temperature pre-warning level
		0 = warning level at $T_{j(AV)(pwarn)}$ = 160 °C
		1 = warning level at $T_{j(AV)(pwarn)}$ = 135 °C
3	D3	enable or disable channel 1 (RF)
		0 = enable channel 1
		1 = disable channel 1

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Table 14. Instruction byte IB3 bit description *…continued*

Bit	Symbol	Description
2	D2	enable or disable channel 3 (LF)
		0 = enable channel 3
		1 = disable channel 3
1	D1	enable or disable channel 2 (RR)
		0 = enable channel 2
		1 = disable channel 2
0	D0	enable or disable channel 4 (LR)
		0 = enable channel 4
		1 = disable channel 4

Table 15. Instruction byte IB4 bit description

Bit	Symbol	Description
7	D7	clip detection level
		0 = detection level set by IB3[D7]
		1 = 10 % detection level
6	D6	undervoltage protection level
		0 = undervoltage protection level at 7.2 V
		1 = undervoltage protection level at 5.5 V (stop/start)
5	D5	AC-load detection measuring current
		0 = at high measuring current
		1 = at low measuring current
4	D4	low gain mode/line driver mode
		0 = low gain (16 dB) with $0.5V_P$ DC output voltage
		1 = line driver with 16 dB gain and $0.25V_P$ DC output voltage
3	D3	pin DIAG when supply voltage is above 16 V
		0 = disable pin DIAG
		1 = enable pin DIAG
2	D2	clip information on pin DIAG
		0 = enable
		1 = disable
1	D1	block clip diagnostics
		0 = below V_P = 10 V
		1 = below undervoltage level set by IB4[D6]
0	D0	diagnostic bits on DBx4 and DBx5
		0 = simple AC/DC-load diagnostic
		1 = advanced DC-load diagnostic

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Table 16. Instruction byte IB5 bit description

Bit	Symbol	Description
7	D7	-
6	D6	-
5	D5	-
4	D4	-
3	D3	diagnostics information in bits DBx[D3]
		0 = short load diagnostic
		1 = speaker fault diagnostic
2	D2	-
1	D1	-
0	D0	-

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9.2 I²C-bus data bytes

If address byte bit R/$\overline{W}$ = 1, the TDF8554J sends 4 data bytes to the microprocessor DB1, DB2, DB3 and DB4; see Table 17 to Table 22.

All bits are latched.

All data bits reset only after reading all 4 data bytes (clear after read), except D4 and D5. D2 is set after a read operation, see Section 7.5.2.

For explanation of AC and DC load detection bits, see Section 7.5.3.

Table 17. Data byte DB1 bit description

Bit	Symbol	Description
7	D7	amplifier thermal protection pre-warning
		0 = no warning
		1 = junction temperature above pre-warning level
6	D6	amplifier maximum thermal protection
		0 = no warning
		1 = amplifier temperature above pre-warning level
5	D5	channel 4 load detection results; see Table 18
4	D4	
3	D3	channel 4 diagnostic results; see Table 19
2	D2	channel 4 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 4 V_P short-circuit detection
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 4 short-circuit to ground detection
		0 = no short-circuit to ground
		1 = short-circuit to ground

Table 18. Channel load detection results

Bit		IB4[D0] = 1	IB4[D0] = 0
D5	D4		
0	0	normal load	normal load; no AC load
1	0	open load	no normal load; no AC load
1	1	invalid	no normal load; AC load
0	1	line driver load	normal load; AC load

Table 19. Channel diagnostic results

Bit	Symbol	IB5[D3] = 0	IB5[D3] = 1[1]
D3	D3	0 = no shorted load	0 = no speaker fault
		1 = shorted load	1 = speaker fault

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[1] When IB5[D3] = 1 (read out of the speaker fault), the shorted load protection still operates. If a shorted load occurs, the channel switches off for 15 ms, an internal latch is set and pin DIAG is pulled LOW. The shorted load internal latch (DBx[D3]) can be read when IB5[D3] = 0. Data bits are only reset (cleared after read) after reading all 4 data bytes.

Table 20. Data byte DB2 bit description

Bit	Symbol	Description
7	D7	enable or disable amplifier
		0 = amplifier on
		1 = POR has occurred; amplifier off
6	D6	regulator thermal protection pre-warning
		0 = no warning
		1 = regulator temperature too high; amplifier off
5	D5	channel 2 load detection results; see Table 18
4	D4	
3	D3	channel 2 diagnostic results; see Table 19
2	D2	channel 2 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 2 V_P short-circuit detection
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 2 short-circuit to ground detection
		0 = no short-circuit to ground
		1 = short-circuit to ground

Table 21. Data byte DB3 bit description

Bit	Symbol	Description
7	D7	supply undervoltage (level set by IB4[D6])
		0 = no supply undervoltage has occurred
		1 = supply undervoltage has occurred
6	D6	supply overvoltage
		0 = no supply overvoltage has occurred
		1 = supply overvoltage has occurred
5	D5	channel 3 load detection results; see Table 18
4	D4	
3	D3	channel 3 diagnostic results; see Table 19
2	D2	channel 3 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 3 V_P short-circuit detection
		0 = no short-circuit to V_P
		1 = short-circuit to V_P

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Table 21. Data byte DB3 bit description *…continued*

Bit	Symbol	Description
0	D0	channel 3 short-circuit to ground detection
		0 = no short-circuit to ground
		1 = short-circuit to ground

Table 22. Data byte DB4 bit description

Bit	Symbol	Description
7	D7	V_P = 16 V behavior
		0 = V_P not above 16 V
		1 = V_P has been above 16 V
6	D6	system status
		0 = system not busy with start-up diagnostic/start-up
		1 = system busy with start-up diagnostic cycle or amplifier start-up (if selected by IB1[D0])
5	D5	channel 1 load detection results; see Table 18
4	D4	
3	D3	channel 1 diagnostic results; see Table 19
2	D2	channel 1 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 1 short-circuit to V_P
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 1 short-circuit to ground
		0 = no short-circuit to ground
		1 = short-circuit to ground

10. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating	6	18	V
		not operating	−1	+50	V
		load dump protection for $t \leq 50$ ms and $t_r \geq 2.5$ ms	-	50	V
$V_{P(r)}$	reverse supply voltage	reverse polarity ≤ 10 minutes	-	−2	V
I_{OSM}	non-repetitive peak output current		-	13	A
I_{ORM}	repetitive peak output current		-	8	A
$T_{j(max)}$	maximum junction temperature		-	150	°C
T_{stg}	storage temperature		−55	+150	°C

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Table 23. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature	heatsink of sufficient size to ensure T_j does not exceed 150 °C		−40	+105	°C
$V_{(prot)}$	protection voltage	AC and DC short-circuit voltage of output pins and across the load		-	V_P	V
V_{SDA}	voltage on pin SDA	operating		0	6.5	V
V_{SCL}	voltage on pin SCL	operating		0	6.5	V
V_x	voltage on pin x	pins SVR, ACGND, DIAG; operating		0	10	V
		pin STB	[1]	0	24	V
$V_{i(max)}$	maximum input voltage	RMS value; before capacitor; R_S = 100 Ω		-	5	V
P_{tot}	total power dissipation	T_{case} = 70 °C		-	80	W
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R_S = 1.5 kΩ	[2]	-	2000	V
		CDM	[3]			
		corner pins		-	750	V
		non-corner pins		-	500	V

[1] 10 kΩ series resistance if connected to V_P.

[2] Human Body Model (HBM): all pins have passed all tests to 2500 V to guarantee 2000 V, according to class II.

[3] Charged-Device Model (CDM).

11. Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	DBS37; see Figure 19	0.75	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	DBS37	40	K/W

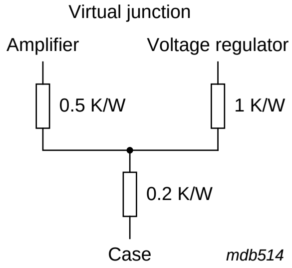

Fig 19. Equivalent thermal resistance network

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12. Characteristics

Table 25. Amplifier characteristics

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = –40 °C to +150 °C; functionality guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage behavior							
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω		6	14.4	18	V
		R_L = 2 Ω		6	14.4	16	V
I_q	quiescent current	no load		-	260	350	mA
		no load; V_P = 7 V		-	190	-	mA
I_{off}	off-state current	V_{STB} = 0.4 V		-	4	10	μA
V_O	output voltage	DC					
		amplifier on; high gain/low gain mode		6.6	7.1	7.6	V
		line driver mode; IB4[D4] = 1; IB3[D5:D6] = 1		3.0	3.4	3.8	V
$V_{P(low)(mute)}$	low supply voltage mute	rising supply voltage					
		IB4[D6] = 0		7.0	7.7	8.1	V
		IB4[D6] = 1		5.4	5.7	6.2	V
		falling supply voltage					
		IB4[D6] = 0		6.5	7.2	7.7	V
		IB4[D6] = 1		5.2	5.5	5.9	V
$\Delta V_{P(low)(mute)}$	low supply voltage mute hysteresis	IB4[D6] = 0		0.1	0.5	0.8	V
		IB4[D6] = 1		0.1	0.3	0.7	V
$V_{P(ovp)pwarn}$	pre-warning overvoltage protection supply voltage	rising supply voltage		15.2	16	16.9	V
		falling supply voltage		14.4	15.2	16.2	V
		hysteresis		-	0.8	-	V
$V_{th(ovp)}$	overvoltage protection threshold voltage	rising supply voltage		18	20	22	V
V_{POR}	power-on reset voltage	falling supply voltage		-	3.1	4.5	V
$V_{O(offset)}$	output offset voltage	amplifier on		–75	0	+75	mV
		amplifier mute		–25	0	+25	mV
		line driver mode		–45	0	+45	mV
Mode select (pin STB) second clip detection							
V_{STB}	voltage on pin STB	I²C-bus mode off		-	-	0.8	V
		I²C-bus mode on; operating mode selected		2.5	-	V_P	V
I_{STB}	current on pin STB	0 V < V_{STB} < 8.5 V	[1]	-	5	30	μA
Start-up, shut-down and mute timing							
t_{wake}	wake-up time	time after wake-up via pin STB before first I²C-bus transmission is recognized; see Figure 3		-	300	500	μs
$I_{LO(SVR)}$	output leakage current on pin SVR			-	-	5	μA

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Table 25. Amplifier characteristics *…continued*

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = –40 °C to +150 °C; functionality guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(mute\_off)}$	mute off delay time	time from amplifier start until 10 % of output signal; I_{LO} = 0 μA; I_{LO} = 5 μA → +15 ms; no DC-load (IB1[D1] = 0); see Figure 3	[2]	-	430	650	ms
t_{amp_on}	amplifier on time	time from amplifier start until 90 % of output signal; I_{LO} = 0 μA; I_{LO} = 5 μA → +30 ms; no DC-load (IB1[D1] = 0); see Figure 3	[2]	-	550	800	ms
t_{off}	amplifier switch-off time	time to DC output voltage < 0.1 V; I_{LO} = 0 μA; I_{LO} = 5 μA → +0 ms; see Figure 3	[2]	250	500	750	ms
$t_{d(mute-on)}$	delay time from mute to on	from 10 % to 90 % of output signal; V_i = 50 mV; IB2[D1] = 1 to 0		5	15	40	ms
$t_{d(soft\_mute)}$	soft mute delay time	from 90 % to 10 % of output signal; V_i = 50 mV; IB2[D1] = 0 to 1		5	15	40	ms
$t_{d(fast\_mute)}$	fast mute delay time	from 90 % to 10 % of output signal; V_i = 50 mV; V_{STB} from > 2.5 V to < 0.8 V in 1 μs; IB2[D0] = 0 to 1		-	0.4	1	ms
$t_{(start-Vo(off))}$	engine start to output off time	V_P from 14.4 V to 5 V in 1.5 ms; V_o < 0.5 V; see Figure 4		-	0.1	1	ms
$t_{(start-SVRoff)}$	engine start to SVR off time	V_P from 14.4 V to 5 V in 1.5 ms; V_{SVR} < 0.7 V; see Figure 4		-	40	75	ms
I²C-bus interface [3]							
V_{IL}	LOW-level input voltage	on pins SCL and SDA		-	-	1.5	V
V_{IH}	HIGH-level input voltage	on pins SCL and SDA		2.3	-	5.5	V
V_{OL}	LOW-level output voltage	on pin SDA; I_L = 5 mA		-	-	0.4	V
f_{SCL}	SCL clock frequency			-	400	-	kHz
Start-up diagnostics							
t_{sudiag}	start-up diagnostic time	from start-up diagnostic command via I²C-bus until completion of start-up diagnostic; V_o + < 0.1 V; V_o – < 0.1 V (no load) IB1[D1] = 1; see Figure 10		50	130	250	ms
$t_{d(sudiag-on)}$	start-up diagnostic to on delay time	at 90 % of output signal; IB1[D0:D1] = 11; see Figure 10		-	680	-	ms
V_{offset}	offset voltage	startup diagnostic offset voltage under no load condition		1.3	2	2.5	V
$R_{Ldet(sudiag)}$	start-up diagnostic load detection resistance	shorted load					
		high gain; IB3[D6:D5] = 00		-	-	0.5	Ω
		low gain; IB3[D6:D5] = 11		-	-	1.5	Ω
		normal load					
		high gain (IB3[D6:D5] = 00)		1.5	-	20	Ω
		low gain (IB3[D6:D5] = 11)		3.2	-	20	Ω
		line driver load		80	-	200	Ω
		open load		400	-	-	Ω

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Table 25. Amplifier characteristics *...continued*

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Diagnostics							
$V_{OL(DIAG)}$	LOW-level output voltage on pin DIAG	fault condition (pin LOW); I_{DIAG} = 1 mA		-	-	0.3	V
$V_{O(offset\_det)}$	output voltage at offset detection			±1.0	±1.3	±2.0	V
THD_{clip}	total harmonic distortion clip detection level	V_P > 10 V					
		IB4[D7] = 1		-	10	-	%
		IB3[D7] = 0; IB4[D7] = 0		-	5	-	%
		IB3[D7] = 1; IB4[D7] = 0		-	2	-	%
$T_{j(AV)(pwarn)}$	pre-warning average junction temperature	IB3[D4] = 0		150	160	170	°C
		IB3[D4] = 1		125	135	145	°C
$T_{j(AV)(G(-0.5dB))}$	average junction temperature for 0.5 dB gain reduction	V_i = 0.05 V		-	175	-	°C
$\Delta G_{(th\_fold)}$	gain reduction of thermal foldback	when all channels switch off		-	20	-	dB
I_o	output current	peak current:					
		AC-load detected; IB4[D5] = 0		500	-	-	mA
		AC-load detected; IB4[D5] = 1		275	-	-	mA
		no AC-load detected; IB4[D5] = 0		-	-	250	mA
		no AC-load detected; IB4[D5] = 1		-	-	110	mA
Amplifier							
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %		18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %		23	25	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 0.5 %		29	32	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %		40	44	-	W
$P_{o(max)}$	maximum output power	R_L = 4 Ω; V_P = 14.4 V; V_i = 2 V RMS square wave		37	40	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_i = 2 V RMS square wave		41	45	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_i = 2 V RMS square wave		58	64	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω		-	0.01	0.1	%
		P_o = 1 W to 12 W; f_i = 10 kHz		-	0.2	0.4	%
		line driver mode; V_o = 1 V (RMS) and 4 V (RMS)		-	0.02	0.05	%
		low gain mode; P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω		-	0.01	0.1	%
α_{cs}	channel separation	R_S = 1 kΩ; R_{ACGND} = 250 Ω	[4]				
		f_i = 1 kHz		65	80	-	dB
		f_i = 10 kHz		55	65	-	dB

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Table 25. Amplifier characteristics *…continued*

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz; V_P = 10.5 V; R_S = 1 kΩ; R_{ACGND} = 250 Ω	[4]	55	70	-	dB
CMRR	common mode rejection ratio	amplifier mode; V_{cm} = 0.3 V (p-p); f_i = 1 kHz to 3 kHz; R_S = 1 kΩ; R_{ACGND} = 250 Ω	[4]				
		common mode input to differential output ($V_{O(dif)}$ / $V_{I(cm)}$ + 26 dB)		55	65	-	dB
		common mode input to common mode output ($V_{O(cm)}$ / $V_{I(cm)}$ + 26 dB)		50	58	-	dB
ΔV_O	output voltage variation	plop during switch-on and switch-off	[5]				
		from off to mute and mute to off		-	-	7.5	mV
		from mute to on and on to mute (soft mute)		-	-	7.5	mV
		from off to on and on to off; start-up diagnostic enabled		-	-	7.5	mV
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz (6th order)					
		mute mode; R_S = 1 kΩ		-	15	23	μV
		line driver mode; R_S = 1 kΩ		-	25	33	μV
		line driver mode; R_S = 50 Ω		-	25	33	μV
		amplifier mode; R_S = 1 kΩ		-	43	65	μV
		amplifier mode; R_S = 50 Ω		-	40	60	μV
$G_{v(amp)}$	voltage gain amplifier mode	single-ended in to differential out		25.5	26	26.5	dB
$G_{v(ld)}$	voltage gain line driver mode	single-ended in to differential out		15.5	16	16.5	dB
Z_i	input impedance	T_{amb} = −40 °C to +105 °C		38	62	99	kΩ
		T_{amb} = 0 °C to 105 °C		55	62	99	kΩ
α_{mute}	mute attenuation	$V_{o(on)}$ / $V_{o(mute)}$; V_i = 50 mV		80	92	-	dB
$V_{o(mute)(RMS)}$	RMS mute output voltage	V_i = 1 V RMS; filter 20 Hz to 22 kHz		-	16	29	μV
B_p	power bandwidth	−1 dB		-	20 to 20000	-	Hz
$C_{L(crit)}$	critical load capacitance	no oscillation; open load and 2 Ω load, all outputs to GND or across the load		33	-	-	nF

[1] V_{STB} depends on the current into pin STB: minimum = (1429 × I_{STB}) + 5.4 V, maximum = (3143 × I_{STB}) + 5.6 V.

[2] The times are specified without leakage current. For a leakage current of 5 μA on pin SVR, the delta time is specified. If the capacitor value on pin SVR changes ± 30 %, the specified time will also change ± 30 %. The specified times include an ESR of 15 Ω for the capacitor on pin SVR.

[3] Standard I²C-bus specification: maximum LOW-level = $0.3V_{DD}$, minimum HIGH-level = $0.7V_{DD}$. To comply with 5 V and 3.3 V logic the maximum LOW-level is defined by V_{DD} = 5 V and the minimum HIGH-level by V_{DD} = 3.3 V.

[4] For optimum channel separation (α_{cs}), supply voltage ripple rejection (SVRR) and common mode rejection ratio (CMRR), a resistor $R_{ACGND} = \frac{R_S}{4}$ Ω must be in series with the ACGND capacitor.

[5] The plop noise during amplifier switch-on and switch-off is measured using an ITU-R 2K filter; see Figure 20.

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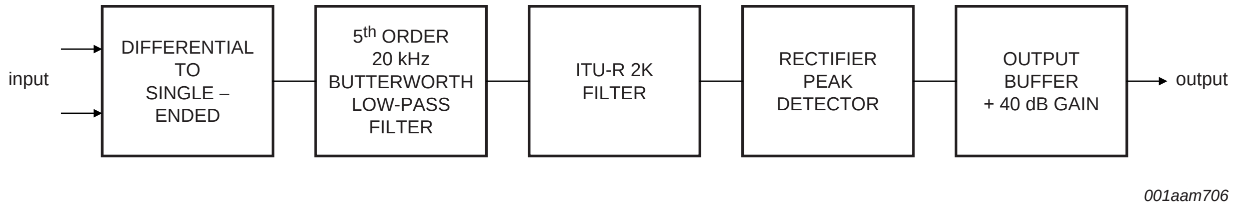
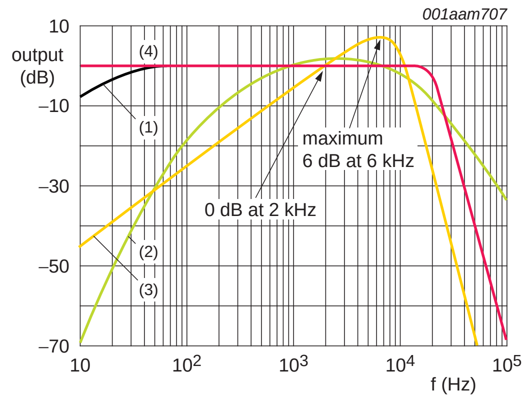


Fig 20. Location of ITU-R 2K filter



(1) 20 Hz.
(2) A-weighting.
(3) ITU-R arm.
(4) 20 kHz bandwidth limit.

Fig 21. Plop noise test using ITU-R 2K filter

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Table 26. Voltage regulator characteristics

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage	regulators 1, 3, 4 and 5 on		10.0	14.4	18	V
		standby regulator 2 switched on		4.0	-	-	V
		standby regulator 2 in regulation		6.3	-	50	V
$V_{th(dis)}$	disable threshold voltage	regulator 1, 3, 4 and 5 on; switches 1 and 2 on		18.1	22	-	V
$I_{q(tot)}$	total quiescent current	standby mode; V_P = 14.4 V	[1]	-	150	190	μA
Reset output (push-pull stage, pin RST)							
V_{th}	threshold voltage	regulator 2; V_P rising; $I_{o(reg2)}$ = 50 mA		$V_{O(reg2)}$ − 0.2	$V_{O(reg2)}$ − 0.1	$V_{O(reg2)}$ − 0.04	V
		regulator 2; V_P falling; $I_{o(reg2)}$ = 50 mA		$V_{O(reg2)}$ − 0.2	$V_{O(reg2)}$ − 0.15	$V_{O(reg2)}$ − 0.1	V
I_{sink}	sink current	LOW-level; V_{RST} ≤ 0.8 V		1	-	-	mA
I_{source}	source current	HIGH-level; V_{RST} = $V_{O(reg)}$ − 0.5 V; V_P = 14.4 V		200	600	-	μA
t_r	rise time		[2]	-	2	50	μs
t_f	fall time		[2]	-	10	50	μs
Reset delay (pin RESCAP)							
I_{ch}	charge current	V_{RESCAP} = 0 V		1	4	8	μA
I_{dch}	discharge current	V_{RESCAP} = 3 V V_P ≥ 4.3 V		1	7	-	mA
$V_{th(RST)}$	threshold voltage on pin RST	TDF8554J/N2		2.5	3	3.5	V
		TDF8554J/N4		1.6	2.1	2.6	V
$t_{d(rst)}$	reset delay time	without C_{RESCAP}	[3]	-	40	-	μs
		C_{RESCAP} = 47 nF; see Figure 22	[3]	15	35	100	μs
Regulator 1 audio supply: pin REG1; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 400 mA; 12 V < V_P < 18 V					
		IB2[D3:D2] = 01		7.9	8.3	8.7	V
		IB2[D3:D2] = 10		8.1	8.5	8.9	V
		IB2[D3:D2] = 11		8.3	8.7	9.1	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	60	-	dB
V_{do}	dropout voltage	V_P = 7.5 V	[4]				
		I_O = 200 mA		-	0.4	0.8	V
		I_O = 400 mA		-	0.6	2.5	V
I_O	output current	V_O ≥ 7 V	[5]	400	700	-	mA
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[6]	70	190	-	mA
Line regulation							
ΔV_O	output voltage variation	12 V ≤ V_P ≤ 18 V		-	-	50	mV
Load regulation							
ΔV_O	output voltage variation	5 mA ≤ I_O ≤ 400 mA		-	-	100	mV

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Table 26. Voltage regulator characteristics *...continued*

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Regulator 2 microprocessor supply: pin REG2; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 350 mA; 10 V ≤ V_P ≤ 18 V					
		TDF8554J/N2		4.75	5.0	5.25	V
		TDF8554J/N4		3.1	3.3	3.5	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		40	50	-	dB
V_{do}	dropout voltage	V_{BUCAP} = 4.75 V; I_O = 200 mA	[7]				
		TDF8554J/N2		-	0.5	0.8	V
		TDF8554J/N4		-	1.75	2.0	V
		V_{BUCAP} = 4.75 V; I_O = 350 mA	[7]				
		TDF8554J/N2		-	0.5	1.3	V
		TDF8554J/N4		-	0.75	2.7	V
I_O	output current	V_O ≥ 2.8 V	[5]	400	1000	-	mA
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[6]	160	300	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 300 mA		-	-	100	mV
Regulator 3 mechanical digital supply: pin REG3; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 300 mA; 10 V ≤ V_P ≤ 18 V		3.1	3.3	3.5	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	65	-	dB
V_{do}	dropout voltage	V_P = 4.75 V; I_O = 300 mA	[4]	-	1.45	1.65	V
I_O	output current	V_O ≥ 2.8 V	[5]	400	700	-	mA
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[6]	135	210	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 300 mA		-	-	100	mV

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Table 26. Voltage regulator characteristics *...continued*
Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Regulator 4 mechanical drive supply: pin REG4; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 800 mA; 10 V ≤ V_P ≤ 18 V					
		IB2[D7:D5] = 001		4.75	5.0	5.25	V
		IB2[D7:D5] = 010		5.7	6.0	6.3	V
		IB2[D7:D5] = 011		6.6	7.0	7.4	V
		IB2[D7:D5] = 100		8.1	8.6	9.1	V
SVRR	supply voltage ripple rejection	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	65	-	dB
V_{do}	dropout voltage	V_P = $V_{O(reg)}$ − 0.5 V	[4]				
		I_O = 800 mA		-	0.6	1.0	V
I_{OM}	peak output current	t ≤ 3 s; V_O = 4 V		1	1.5	-	A
I_O	output current	V_O ≥ 4 V; t ≤ 100 ms; V_P ≥ 11.5 V	[5]	1.5	2	-	A
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[6]	240	400	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 400 mA		-	-	100	mV
Regulator 5 display supply: pin REG5; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 400 mA					
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0001		5.7	6.0	6.3	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0010		6.65	7.0	7.37	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0011		7.8	8.2	8.6	V
		10.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0100		8.55	9.0	9.45	V
		11 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0101		9	9.5	10.0	V
		11.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0110		9.5	10.0	10.5	V
		13 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0111		9.9	10.4	10.9	V
		14.2 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1000		11.8	12.5	13.2	V
		12.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1001		V_P − 1.0	-	-	V
SVRR	supply voltage ripple rejection	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	60	-	dB
V_{do}	dropout voltage	V_P = $V_{O(reg)}$ − 0.5 V	[4]				
		I_O = 300 mA		-	0.4	0.8	V
		I_O = 400 mA		-	0.5	2.3	V
I_{Olim}	output current limit	V_O ≥ 5.5 V	[5]	400	950	-	mA

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Table 26. Voltage regulator characteristics *...continued*

Refer to test circuit (see Figure 30) at T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OS}	output short-circuit current	$R_L \leq 0.5\ \Omega$	[6]	100	200	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 400 mA		-	-	100	mV
Power switch 1 antenna: pin SW1							
V_{do}	dropout voltage	I_O = 300 mA		-	0.6	0.8	V
		I_O = 400 mA		-	0.6	1.1	V
I_O	output current	V_O ≥ 8.5 V		0.5	1	-	A
Power switch 2 amplifier: pin SW2							
V_{do}	dropout voltage	I_O = 300 mA		-	0.6	0.8	V
		I_O = 400 mA		-	0.6	1.1	V
I_O	output current	V_O ≥ 8.5 V		0.5	1	-	A
Backup mechanism							
I_{bu}	backup current (DC)	V_{BUCAP} ≥ 6 V		0.4	1.5	-	A
V_{CL}	clamping voltage	V_P = 30 V; $I_{O(reg2)}$ = 100 mA		-	24	28	V
V_{do}	dropout voltage	I_O = 500 mA; (V_P − V_{BUCAP})		-	0.6	0.8	V

[1] The quiescent current is measured in standby mode when $R_L = \infty$.

[2] The rise and fall times are measured with a 50 pF load capacitor.

[3] The reset delay time depends on the value of the reset capacitor: $t_{d(rst)} = \frac{C_{RESCAP}}{I_{ch}} \times V_{th(rst)} = C_{RESCAP} \times (750 \times 10^3)\ s$

[4] The dropout voltage of a regulator is the voltage difference between V_P and $V_{O(REG)}$.

[5] At current limit, $V_{O(REG)}$ is held constant; see Figure 15.

[6] The foldback current protection limits the dissipation power at short-circuit; see Figure 15.

[7] The dropout voltage of regulator 2 is the voltage difference between V_{BUCAP} and $V_{O(reg)}$.

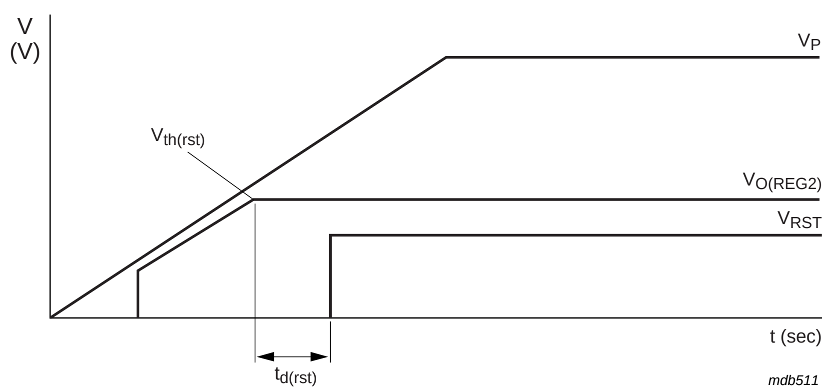

Fig 22. Reset delay function

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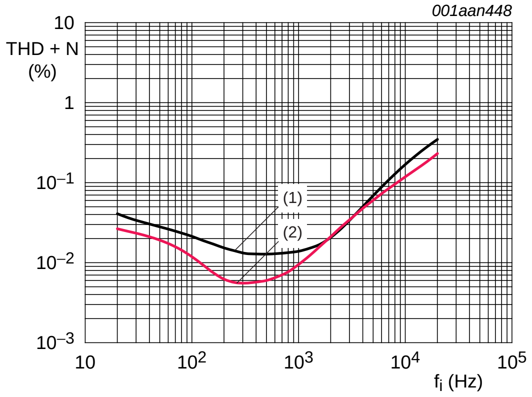
13. Performance diagrams

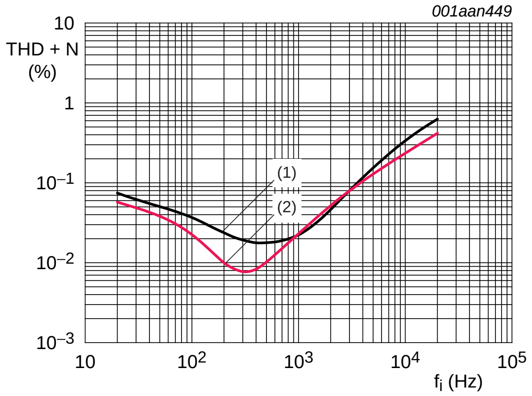


V_P = 14.4 V.

(1) P_o = 1 W

(2) P_o = 10 W

Fig 23. Total harmonic distortion plus noise as a function of input frequency; R_L = 4 Ω



V_P = 14.4 V.

(1) P_o = 1 W

(2) P_o = 10 W

Fig 24. Total harmonic distortion plus noise as a function of input frequency; R_L = 2 Ω

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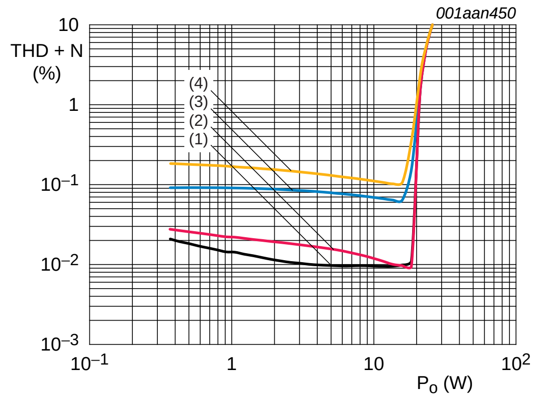


V_P = 14.4 V.

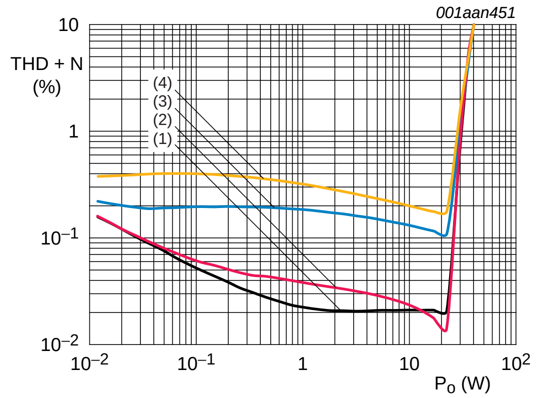
(1) f_i = 1 kHz

(2) f_i = 100 Hz

(3) f_i = 6 kHz

(4) f_i = 10 kHz

Fig 25. Total harmonic distortion plus noise as a function of output power; R_L = 4 Ω



V_P = 14.4 V.

(1) f_i = 1 kHz

(2) f_i = 100 Hz

(3) f_i = 6 kHz

(4) f_i = 10 kHz

Fig 26. Total harmonic distortion plus noise as a function of output power; R_L = 2 Ω

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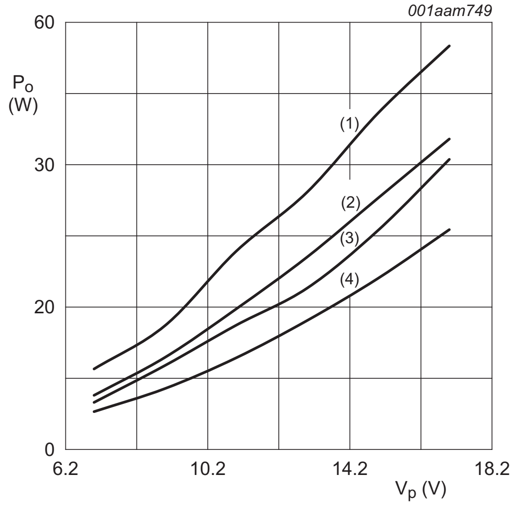


f_i = 1 kHz.

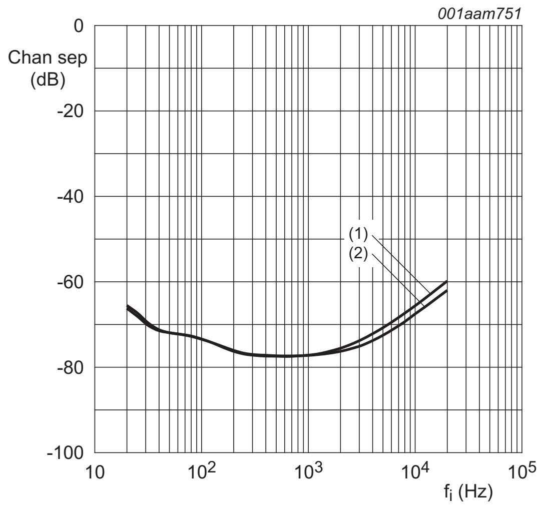
(1) THD = 10 %; 2 Ω.

(2) THD = 0.5 %; 2 Ω.

(3) THD = 10 %; 4 Ω.

(4) THD = 0.5 %; 4 Ω.

Fig 27. Output power as a function of supply voltage; R_L = 4 Ω and 2 Ω



(1) Channel 1 S/N (dB).

(2) Channel 2 S/N (dB).

Fig 28. Channel separation as a function of input frequency; R_L = 4 Ω and 2 Ω

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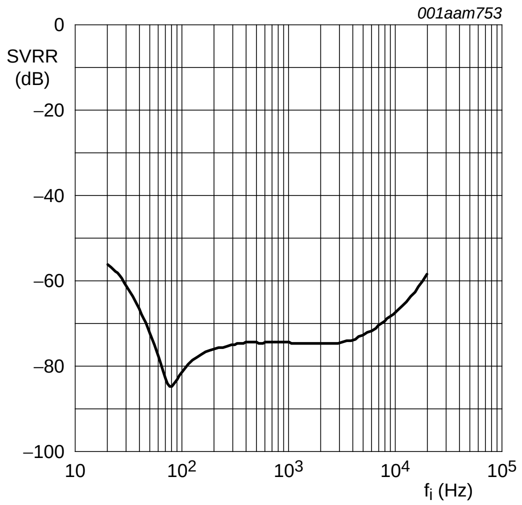

Fig 29. Supply voltage ripple rejection as a function of input frequency

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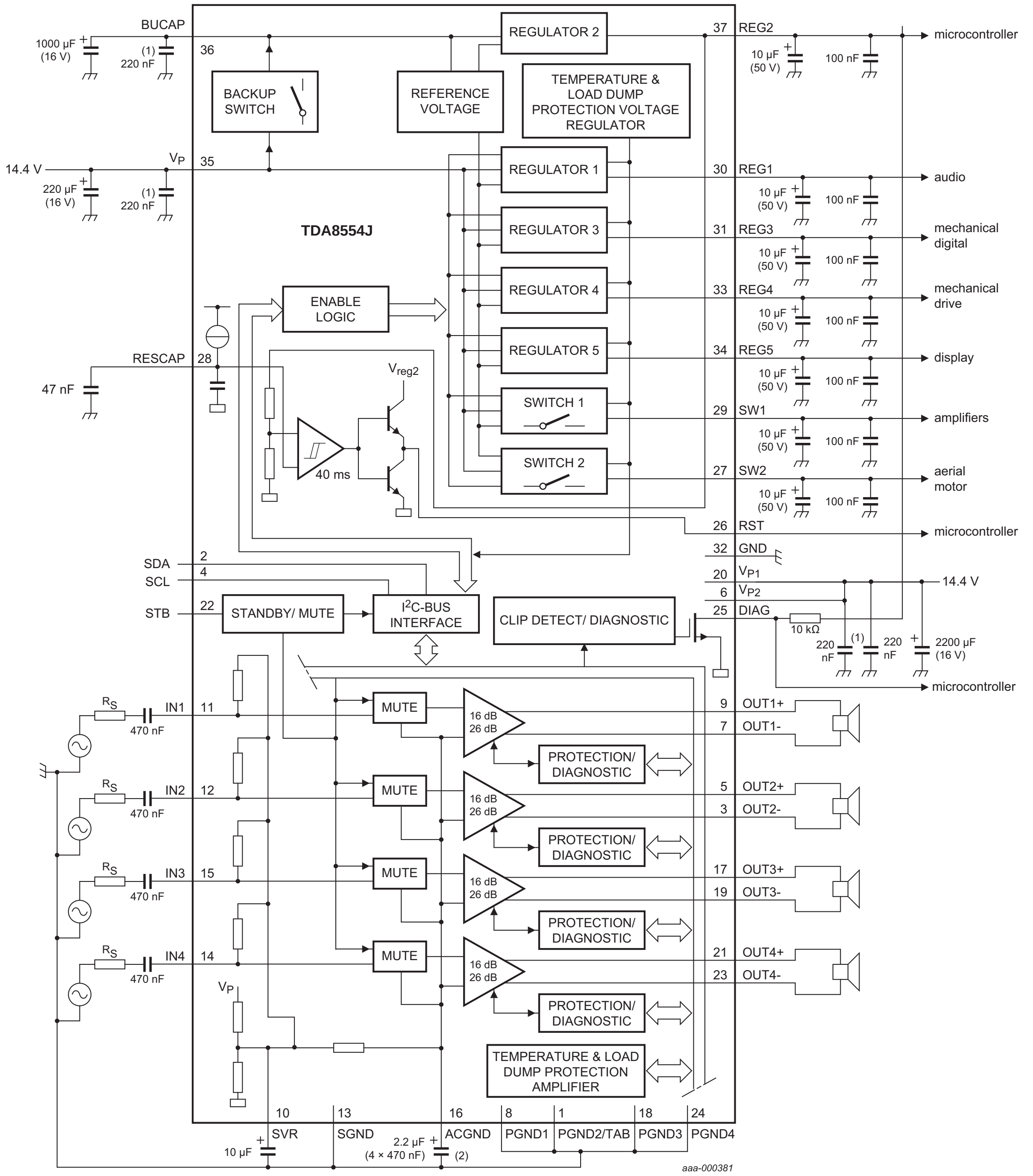
14. Application information



(1) Connect good quality decoupling capacitors close to supply pins to suppress peak voltages on the supply line which can occur if several channels are shorted to V_P simultaneously and protection activated. 0805 case size capacitors (X7R material, 220 nF) connected close to each of the supply pins have given good results.

(2) ACGND capacitor value must be close to 4 × input capacitance; 4 × 470 nF can be used instead of 2.2 µF.

(3) For EMC reasons, a 10 nF capacitor can be connected between each amplifier output and ground.

Fig 30. Test and application diagram

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14.1 Application PCB layout

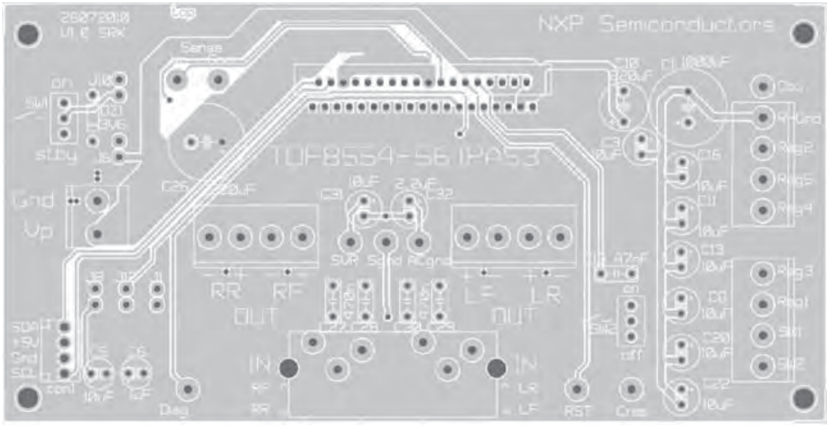

Fig 31. PCB top view

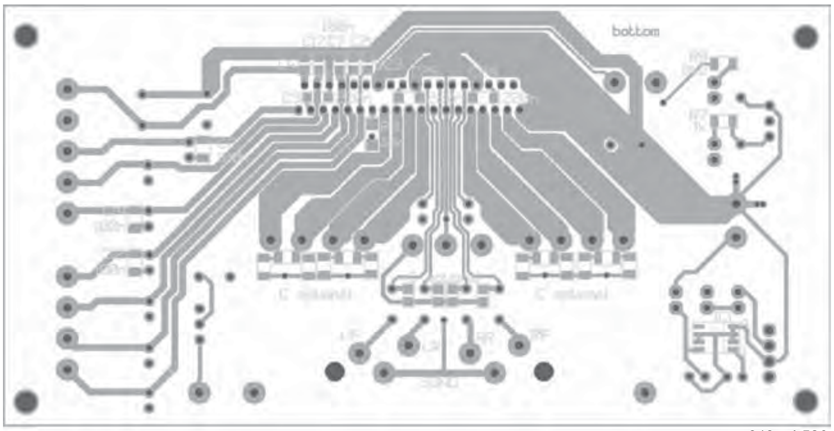

Fig 32. PCB bottom view

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14.2 Beep input circuit

Beep input circuit to amplify the beep signal from the microcontroller to all 4 amplifiers with gain set to 0 dB. Note that this circuit will not affect amplifier performance.

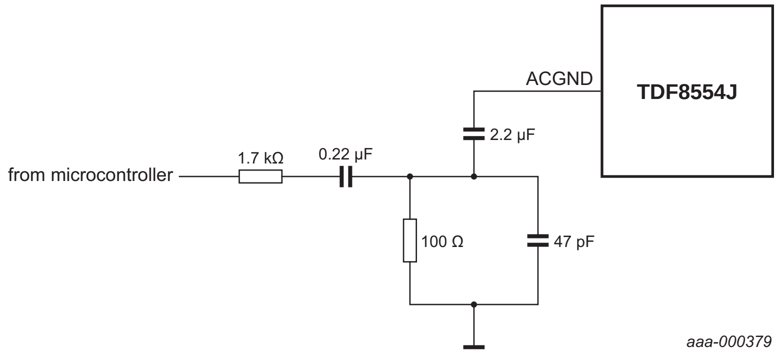

Fig 33. Application diagram for beep input

14.3 Regulator output noise

The outputs of regulators 1 to 5 are designed to give very low noise with good stability. The noise output voltage depends on output capacitor C_o. Table 27 shows the affect of the output capacitor on the noise figure.

Table 27. Regulator noise figures

Regulator	Noise figure (μV) [1]		
	C_o = 10 μF	C_o = 47 μF	C_o = 100 μF
1	225	195	185
2	750	550	530
3	120	100	95
4	225	195	185
5	320	285	270

[1] Measured in the frequency range 20 Hz to 80 kHz; at $I_{O(reg)}$ = 10 mA.

14.4 Regulator stability

The regulators are made stable by the external capacitors connected to the regulator outputs. The stability can be guaranteed with almost any output capacitor if its Equivalent Series Resistance (ESR) stays below the ESR curve shown in Figure 34. If an electrolytic capacitor is used, its behavior with temperature can cause oscillations at extremely low temperature. Oscillation problems can be avoided by adding a 47 nF capacitor in parallel with the electrolytic capacitor. The following example describes how to select the value of output capacitor.

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14.4.1 Example regulator 2

Regulator 2 is stabilized with an electrolytic output capacitor of 10 μF which has an ESR of 4 Ω. At T_{amb} = –30 °C the capacitor value decreases to 3 μF and its ESR increases to 28 Ω at which the regulator becomes unstable as shown in Figure 34. To avoid problems with stability at low temperatures, the recommended solution is to use tantalum capacitors. Either use a tantalum capacitor of 10 μF, or an electrolytic capacitor with a higher value.

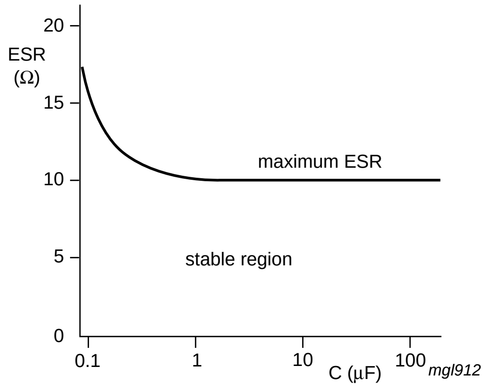

Fig 34. Curve for selecting the value of output capacitors for regulators 1 to 5

15. Test information

15.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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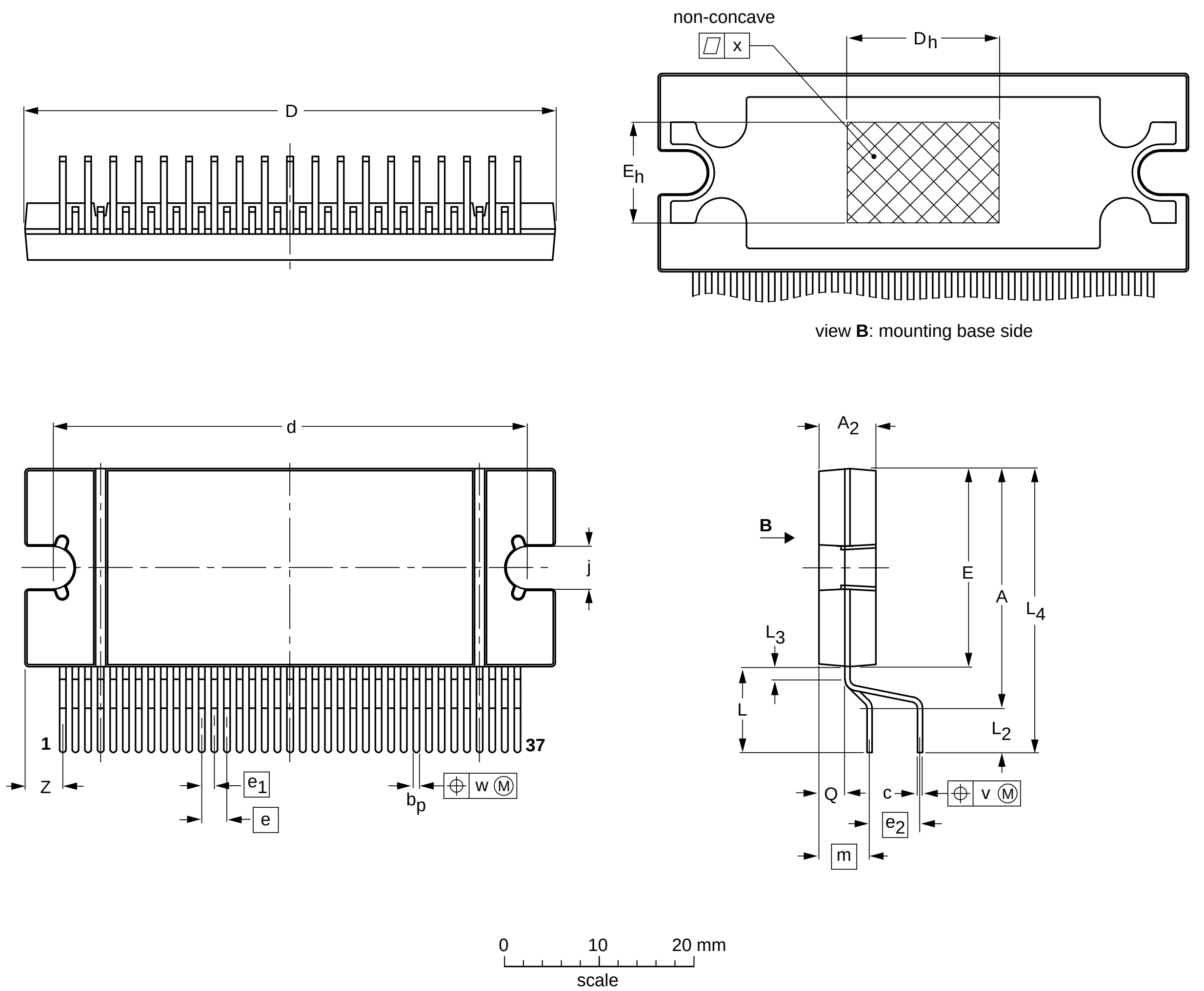
16. Package outline

DBS37P: plastic DIL-bent-SIL power package; 37 leads (lead length 6.8 mm) **SOT725-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_2	L_3	L_4	m	Q	v	w	x	$Z^{(1)}$
mm	19	4.65 4.35	0.60 0.45	0.5 0.3	42.2 41.7	37.8 37.4	12	15.9 15.5	2	1	4	8	3.4 3.1	6.8	3.9 3.1	1.15 0.85	22.9 22.1	4	2.1 1.8	0.6	0.25	0.03	3.30 2.65

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT725-1	- - -	- - -	- - -			~~01-11-14~~ 02-11-22

Fig 35. Package outline SOT725-1 (DBS37P)

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17. Soldering of through-hole mount packages

17.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

17.4 Package related soldering information

Table 28. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

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18. Abbreviations

Table 29. Abbreviations

Acronym	Description
BCDMOS	Bipolar Complementary Double-diffused Metal-Oxide Semiconductor
CMOS	Complementary Metal-Oxide Semiconductor
DMOS	Double-diffused Metal-Oxide Semiconductor
DSP	Digital Signal Processor
EMC	ElectroMagnetic Compatibility
IPAS	Integrated Power Amplifier and Stabilizer
NDMOS	Negative channel DMOS
PDMOS	Positive channel DMOS
POR	Power-On Reset

19. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8554J v.1	20110831	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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