

BTA201 series B, E and ER

1 A Three-quadrant triacs high commutation Rev. 04 — 4 February 2008

Product data sheet

Product profile

1.1 General description

Passivated, guaranteed commutation triacs in a plastic package. The 'sensitive gate' E and ER series are intended for interfacing with low power drivers, including microcontrollers. The high commutation B series are designed to commutate the full RMS current at the maximum junction temperature without the aid of a snubber.

1.2 Features

- Suitable for interfacing with low power drivers, including microcontrollers
- Reverse pinning option (ER type)

1.3 Applications

Motor controls

Solenoid drivers

1.4 Quick reference data

- $I_{TSM} \le 12.5 A$
- $I_{T(RMS)} \le 1 A$
- $V_{DRM} \le 600 \text{ V (BTA201-600B/E)}$
- $V_{DRM} \le 800 \text{ V (BTA201-800B/E/ER)}$
- $I_{GT} \le 50 \text{ mA (BTA201-600B/800B)}$
- $I_{GT} \le 10 \text{ mA (BTA201-600E/800E/ER)}$
- $I_{GT} \ge 5 \text{ mA (BTA201-600B/800B)}$
- $I_{GT} \ge 1 \text{ mA (BTA201-600E/800E/ER)}$

Pinning information

Table 1 Pinning

Table I. Fill	iiig		
Pin	Description	Simplified outline	Graphic symbol
B and E series			
1	main terminal 2 (T2)		N 1
2	gate (G)		T2—T1
3	main terminal 1 (T1)	<u>", ", ", "</u>	`G sym051
ER series			
1	main terminal 1 (T1)		
2	gate (G)	321	
3	main terminal 2 (T2)	SOT54 (TO-92)	



3. Ordering information

Table 2. Ordering information

Type number	Package	Package							
	Name	Description	Version						
BTA201-600B	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54						
BTA201-600E									
BTA201-800B									
BTA201-800E									
BTA201-800ER									

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
		BTA201-600B	<u>[1]</u> -	600	V
		BTA201-600E	<u>[1]</u> _	600	V
		BTA201-800B	-	800	V
		BTA201-800E	-	800	V
		BTA201-800ER	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{lead} \le 54.3$ °C; see Figure 4 and 5	-	1	Α
I _{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3			
		t = 20 ms	-	12.5	Α
		t = 16.7 ms	-	13.7	Α
l ² t	I ² t for fusing	$t_p = 10 \text{ ms}$	-	0.78	A ² s
dI _T /dt	rate of rise of on-state current	$I_{TM} = 1.5 \text{ A}; I_G = 0.2 \text{ A};$ $dI_G/dt = 0.2 \text{ A}/\mu\text{s}$	-	100	A/μs
I _{GM}	peak gate current		-	2	А
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	+150	°C
Tj	junction temperature		-	125	°C

^[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/μs.

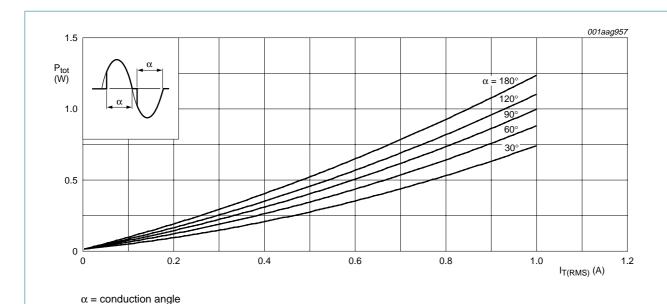
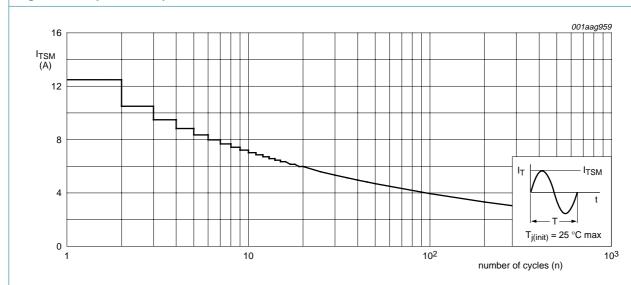
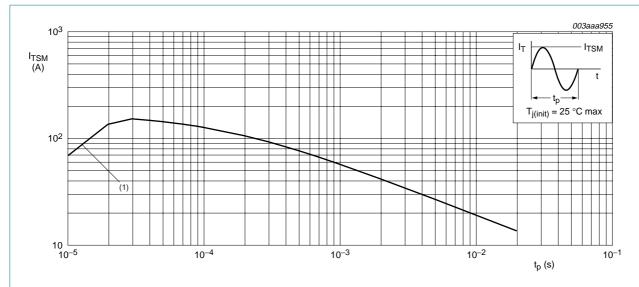


Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



 $t_p \le 20 \text{ ms}$

(1) dl_T/dt limit

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

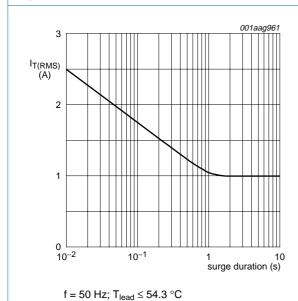


Fig 4. RMS on-state current as a function of surge duration; maximum values

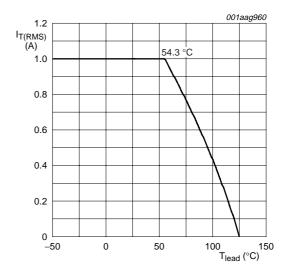


Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to	full cycle; see Figure 6	-	-	60	K/W
	lead	half cycle; see Figure 6	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W

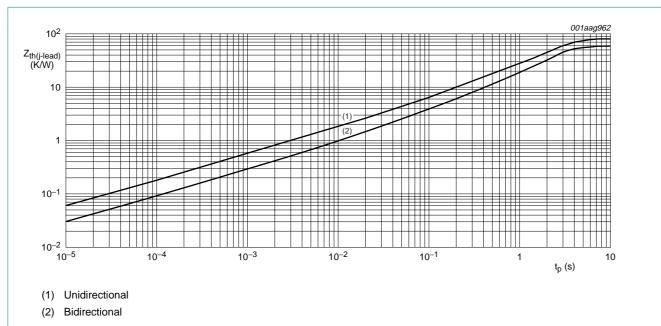


Fig 6. Transient thermal impedance from junction to lead as a function of pulse width

6. Static characteristics

Table 5. Static characteristics

 $T_i = 25 \,^{\circ}C$ unless otherwise specified.

Parameter	Conditions		BTA201-600B BTA201-800B			BTA201-600E BTA201-800E BTA201-800ER			
		Min	Тур	Max	Min	Тур	Max		
gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ see } \frac{\text{Figure 8}}{}$		'	·					
	T2+ G+	5	-	50	1	-	10	mΑ	
	T2+ G-	5	-	50	1	-	10	mΑ	
	T2- G-	5	-	50	1	-	10	mΑ	
I _L latching current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}; \text{ see } \frac{\text{Figure } 10}{}$								
	T2+ G+	-	-	30	-	-	12	mΑ	
	T2+ G-	-	-	50	-	-	20	mΑ	
	T2- G-	-	-	30	-	-	12	mΑ	
holding current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}; \text{ see } \frac{\text{Figure } 11}{}$	-	-	30	-	-	12	mΑ	
on-state voltage	I _T = 1.4 A; see <u>Figure 9</u>	-	1.2	1.5	-	1.2	1.5	V	
gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ see } \frac{\text{Figure 7}}{}$	-	0.7	1.5	-	0.7	1.5	V	
	$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_j = 125 ^{\circ}\text{C}$	0.2	0.3	-	0.2	0.3	-	V	
off-state current	$V_D = V_{DRM(max)}$; $T_j = 125 ^{\circ}C$	-	0.1	0.5	-	0.1	0.5	mA	
	gate trigger current latching current holding current on-state voltage gate trigger voltage	$ \text{gate trigger current} \begin{array}{l} V_D = 12 \text{ V; } I_T = 0.1 \text{ A; see } \underline{\text{Figure 8}} \\ \hline T2 + G + \\ \hline T2 + G - \\ \hline T2 - G - \\ \hline \\ \text{latching current} & V_D = 12 \text{ V; } I_{GT} = 0.1 \text{ A; see } \underline{\text{Figure 10}} \\ \hline T2 + G + \\ \hline T2 + G - \\ \hline T2 - G - \\ \hline \\ \text{holding current} & V_D = 12 \text{ V; } I_{GT} = 0.1 \text{ A; see } \underline{\text{Figure 11}} \\ \hline \text{on-state voltage} & I_T = 1.4 \text{ A; see } \underline{\text{Figure 9}} \\ \hline \text{gate trigger voltage} & V_D = 12 \text{ V; } I_T = 0.1 \text{ A; see } \underline{\text{Figure 7}} \\ \hline V_D = 400 \text{ V; } I_T = 0.1 \text{ A; } T_j = 125 \text{ °C} \\ \hline \end{array} $	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{ c c c c c c } \textbf{Min} & \textbf{Typ} \\ \hline \textbf{gate trigger current} & V_D = 12 \ V; \ I_T = 0.1 \ A; \ see \ \underline{Figure 8} \\ \hline T2+ \ G+ & 5 & - \\ \hline T2+ \ G- & 5 & - \\ \hline T2- \ G- & 5 & - \\ \hline \textbf{Idtching current} & V_D = 12 \ V; \ I_{GT} = 0.1 \ A; \ see \ \underline{Figure 10} \\ \hline T2+ \ G+ & - & - \\ \hline T2+ \ G- & - & - \\ \hline T2- \ G- & - & - \\ \hline T2- \ G- & - & - \\ \hline \textbf{Nolding current} & V_D = 12 \ V; \ I_{GT} = 0.1 \ A; \ see \ \underline{Figure 11} & - & - \\ \hline \textbf{Non-state voltage} & I_T = 1.4 \ A; \ see \ \underline{Figure 9} & - & 1.2 \\ \hline \textbf{Sate trigger voltage} & V_D = 12 \ V; \ I_T = 0.1 \ A; \ see \ \underline{Figure 7} & - & 0.7 \\ \hline \textbf{V}_D = 400 \ V; \ I_T = 0.1 \ A; \ T_j = 125 \ ^{\circ}\text{C} & 0.2 & 0.3 \\ \hline \end{array} $	$ \begin{array}{ c c c c c } & BT $				

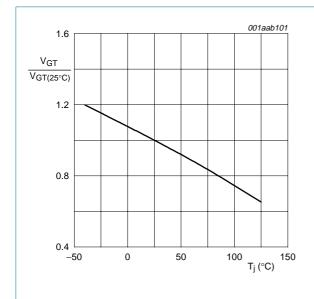
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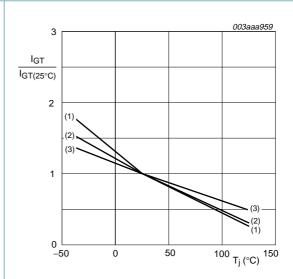
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7. Dynamic characteristics

Table 6. Dynamic characteristics

Symbol	Parameter	Conditions		BTA201-600B BTA201-800B			BTA201-600E BTA201-800E BTA201-800ER		
			Min	Тур	Max	Min	Тур	Max	
dV _D /dt	rate of rise of off-state voltage	$V_{DM} = 67 \% V_{DRM(max)};$ $T_j = 125 °C;$ exponential waveform; gate open circuit	1000	-	-	600	-	-	V/μs
dl _{com} /dt rate of change of commutating current	•	V_{DM} = 400 V; T_j = 125 °C; dV_{com}/dt = 20 V/ μ s; gate open circuit	12	-	-	2.5	-	-	A/ms
		$V_{DM} = 400 \text{ V; T}_j = 125 ^{\circ}\text{C;}$ $dV_{com}/dt = 10 \text{ V/}\mu\text{s; gate}$ open circuit	16	-	-	3.5	-	-	A/ms
t _{gt}	gate-controlled turn-on time	$\begin{split} I_{TM} &= 20 \text{ A;} \\ V_D &= V_{DRM(max)}; \\ I_G &= 0.1 \text{ A;} \\ dI_G/dt &= 5 \text{ A/}\mu\text{s} \end{split}$	-	2	-	-	2	-	μs



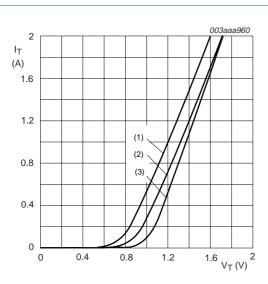


- (1) T2-G-
- (2) T2+ G-
- (3) T2+ G+

Fig 7. Normalized gate trigger voltage as a function of junction temperature

Fig 8. Normalized gate trigger current as a function of junction temperature

BTA201_SER_B_E_ER_4



 $V_0 = 1.02 \text{ V}; R_s = 0.358 \Omega$

- (1) $T_j = 125$ °C; typical values
- (2) T_i = 125 °C; maximum values
- (3) $T_i = 25 \,^{\circ}C$; maximum values

Fig 9. On-state current as a function of on-state voltage

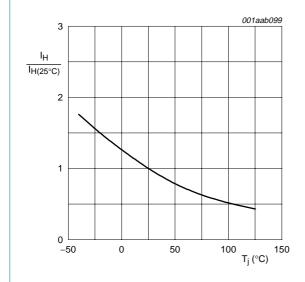


Fig 11. Normalized holding current as a function of junction temperature

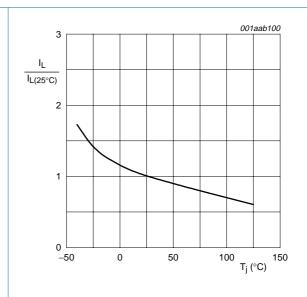
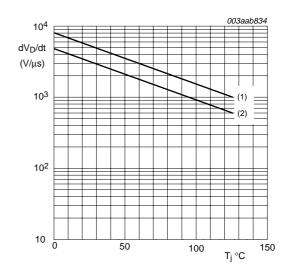


Fig 10. Normalized latching current as a function of junction temperature



Gate open circuit

- (1) BTA201 series B
- (2) BTA201 series E and ER

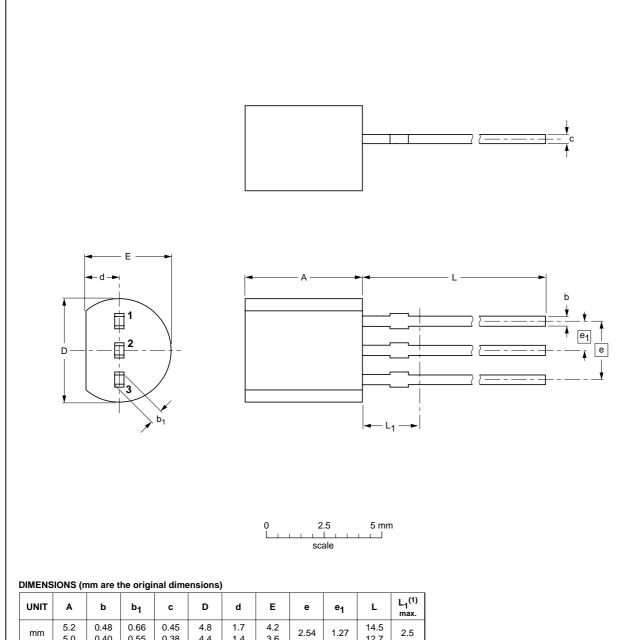
Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

BTA201_SER_B_E_ER_4

Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



UNIT	Α	b	b ₁	С	D	d	E	е	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT54		TO-92	SC-43A			04-06-28 04-11-16

Fig 13. Package outline SOT54 (TO-92)

BTA201_SER_B_E_ER_4

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9. Revision history

Table 7. Revision history

R_3						
dded.						
R_2						
 Table 6 "Dynamic characteristics" on page 7: dV_D/dt uprated. 						
ture;						
R_1						
F						

BTA201 series B, E and ER

1 A Three-quadrant triacs high commutation

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10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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BTA201 series B, E and ER

1 A Three-quadrant triacs high commutation

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