IS89C54/58/64

CMOS SINGLE CHIP
8-BIT MICROCONTROLLER
with 16/32/64-Kbytes of FLASH

FEATURES

- 80C52 based architecture
- 16K/32K/64K Byte Flash Memory with fast-pulse programming algorithm
- 256 x 8 RAM
- Three 16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability
  – 64K Program Memory and 64K Data Memory
- Program memory lock
  – Lock bits (3)
- Power save modes:
  – Idle and power-down
- Eight interrupt sources
- Most instructions execute in 0.3 μs
- CMOS and TTL compatible
- Maximum speed: 40 MHz @ Vcc = 5V
- Packages available:
  – 40-pin DIP
  – 44-pin PLCC
  – 44-pin PQFP

GENERAL DESCRIPTION

IS89C54, IS89C58, IS89C64 are members of *ICSI* embedded microcontroller family. The IS89C54/58/64 uses the same powerful instruction set, has the same architecture, and is pin-to-pin compatible with standard 80C52 controller devices. IS89C54/58/64 are just changed internal Flash size, other features are same as standard IS89C52.

The IS89C54/58/64 contains a 16K/32K/64K x 8 Flash; a 256 x 8 RAM; 32 I/O lines for either multi-processor communications; I/O expansion or full duplex UART; three 16-bit timers/counters; an eight-source, two-priority-level, nested interrupt structure; and on chip oscillator and clock circuit. The IS89C54/58/64 can be expanded using standard TTL compatible memory.

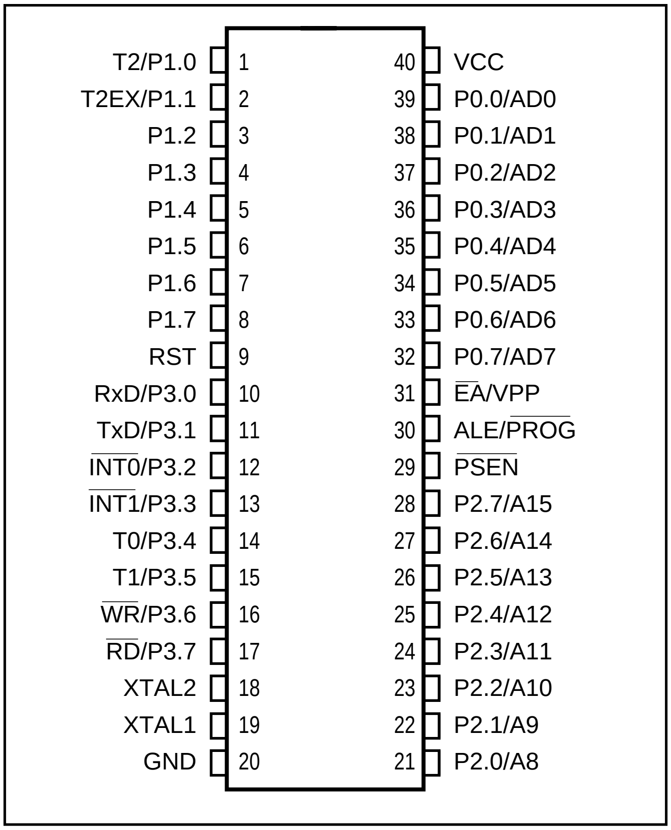


Figure 1. IS89C54/58/64 Pin Configuration: 40-pin DIP

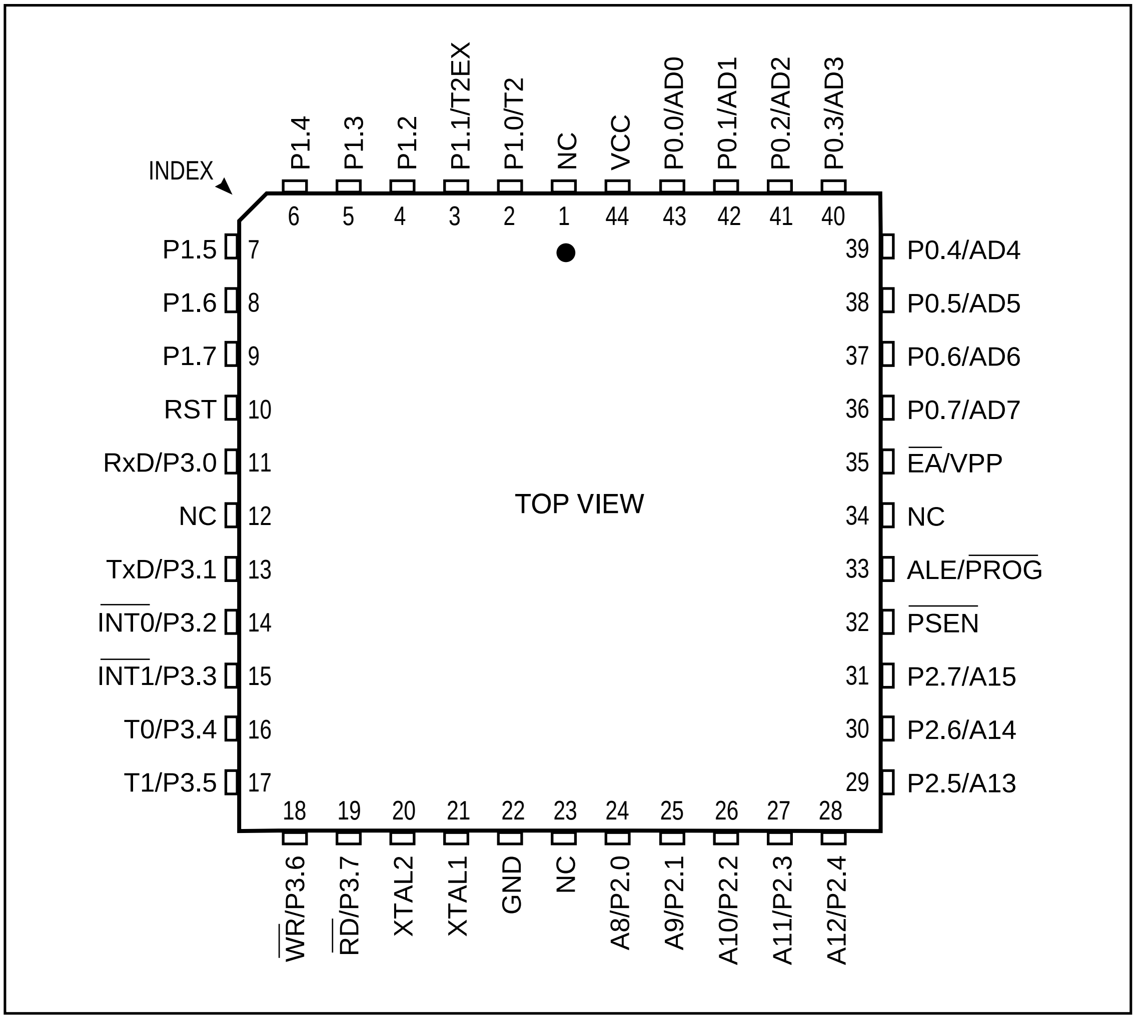


Figure 2. IS89C54/58/64 Pin Configuration: 44-pin PLCC

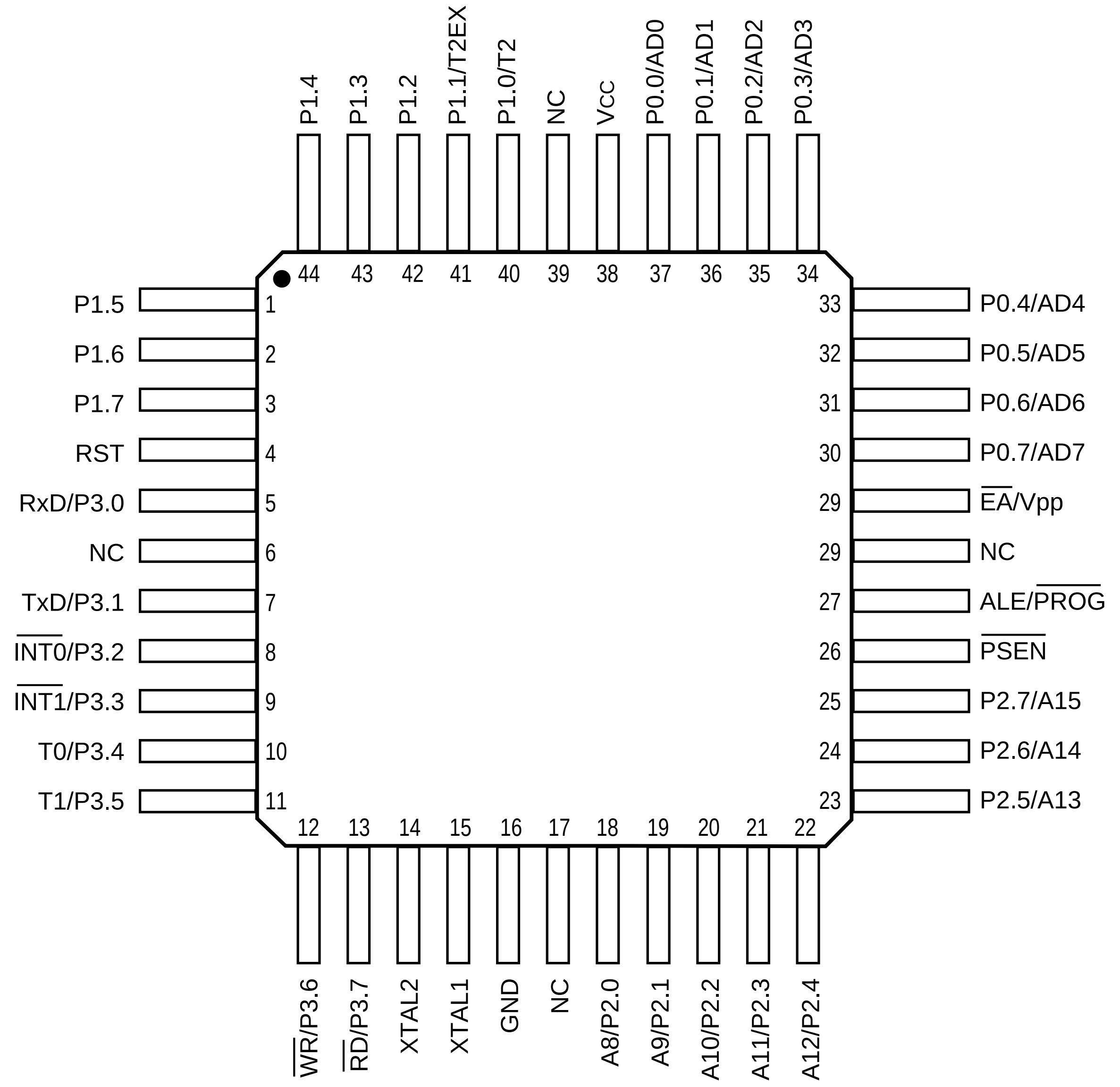


Figure 3. IS89C54/58/64 Pin Configuration: 44-pin PQFP

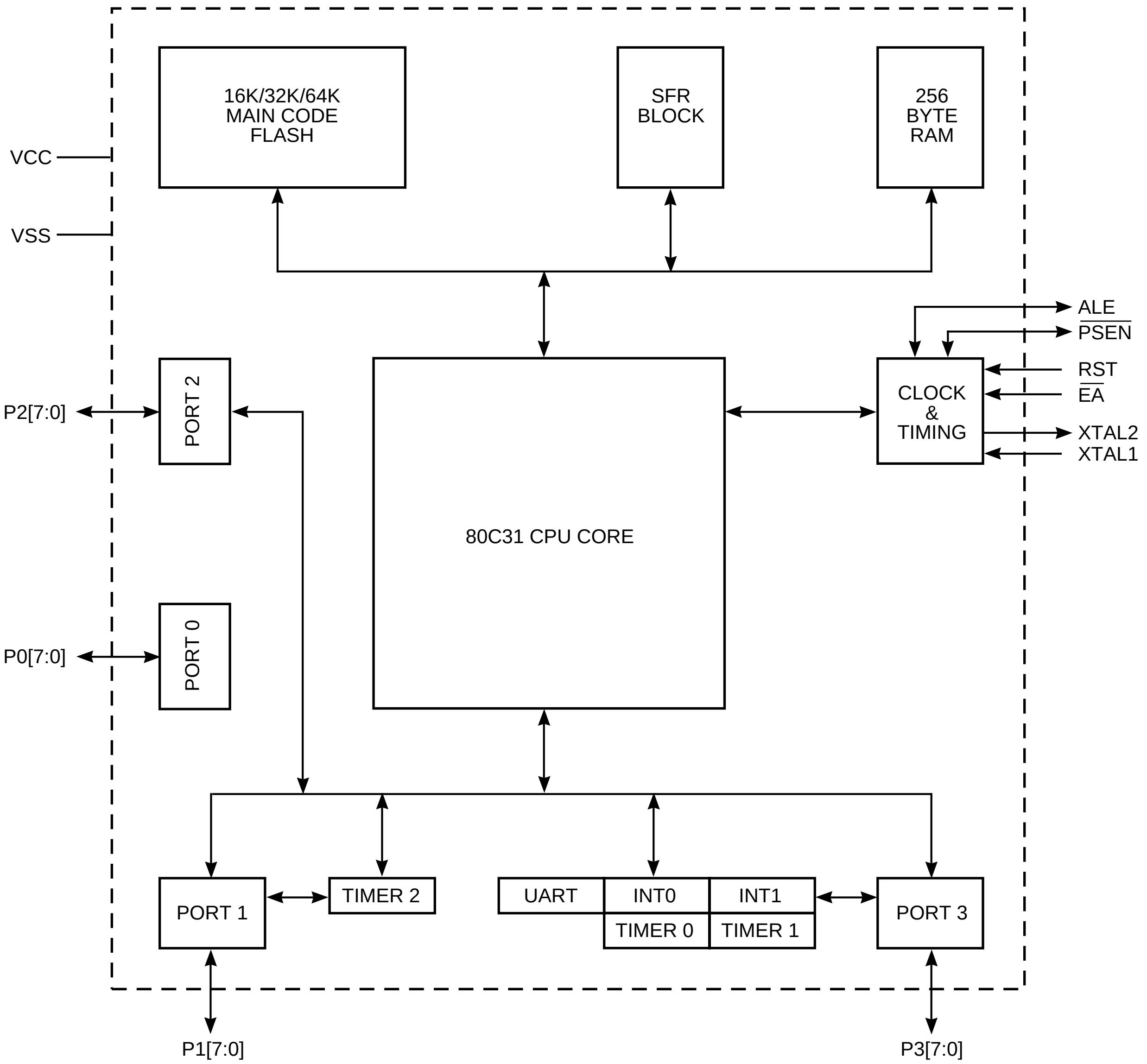


Figure 4. IS89C54/58/64 Block Diagram

Table 1. Detailed Pin Description

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
ALE/$\overline{\text{PROG}}$	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the Program Pulse input ($\overline{\text{PROG}}$) during Flash programming.
$\overline{\text{EA}}$/V_{PP}	31	35	29	I	**External access enable:** EA# must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH. If EA# is held high, the device executes from internal program memory unless the program counter contains an address grater than 3FFFH/7FFFH respecting to IS89C54/58 and the device always executes internal program memory in IS89C64. This is also receives the 12 V programming enable voltage (Vpp) during Flash programming, when 12 V programming is selected.
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is an open-drain, bi-directional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s. Port 0 also receives the command and code bytes during memory program and verification, and outputs the code bytes during program verification. External pullups are required during program verification.
P1.0-P1.7	1-8	2-9	40-44	I/O	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pullups. Port 1 also receives the low-order address byte during memory program and verification.
	1	2	40	I	**T2(P1.0) :** Timer/counter 2 external count input.
	2	3	41	I	**T2EX(P1.1):** Timer/counter 2 trigger input.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the internal pullups. Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses. In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses, port 2 emits the contents of the P2 special function register. Port 2 also receives the high-order address bits from A13 to A8 and some control signals during Flash programming and verification. P2.6, P2.7 are the control signals while the chip programs and erases. P2.6 is a program command strobe signal. P2.7 is a data output enable signal.

Table 1. Detailed Pin Description *(continued)*

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the internal pullups. Port 3 also serves the special features, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port.
	11	13	7	O	**TxD (P3.1):** Serial output port.
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt. Serve as A14 during memory program and verification.
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt. Serve as A15 during memory program and verification.
	14	16	10	I	**T0 (P3.4):** Timer 0 external input.
	15	17	11	I	**T1 (P3.5):** Timer 1 external input.
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):**External data memory write strobe. Control signal during memory program, verification and erase.
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe. Control signal during memory program, verification and erase.
$\overline{\text{PSEN}}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.$\overline{\text{PSEN}}$ is an input control signal while memory program and verification.
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running resets the device. An internal resistor to VSS permits a power-on reset using only an external capacitor. A small internal resistor permits power-on reset using only a capacitor connected to VCC. RST is an input control signal during memory program and verification.
XTAL 1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL 2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.
GND	20	22	16	I	**Ground:** 0V reference.
Vcc	40	44	38	I	**Power Supply:** This is the power supply voltage for operation.

OPERATION DESCRIPTPION

The detail desription of the IS89C54/58/64 included in this desription are:

- **Memory Map and Registers**
- **Flash Memory**

Other informations refer to IS80C52/32 data sheet except flash memory.

MEMORY MAP AND REGISTERS

Table 1 shows program memory and data memory size versus three products. The IS89C54/58/64 series includes a standard IS80C32 and a 16K/32K/64K Flash Memory. The program memory and data memory access ranges are listed table 2.

Table 2. Program memory and Data memory sizes

	Main Flash	RAM Size
IS89C54	16K Bytes : [0H~3FFFH]	256 Bytes : [0-FFH]
IS89C58	32K Bytes : [0H~7FFFH]	256 Bytes : [0-FFH]
IS89C64	64K Bytes : [0H~FFFFH]	256 Bytes : [0-FFH]

FLASH MEMORY PROGRAMMING

The Flash architecture of IS89C54/58/64 is shown in Figure 5. IS89C54/58 include block 1 and lock bits block. The signature bytes are fixed value reside in MCU, they are read only. Block 2 resides in IS89C64 only.

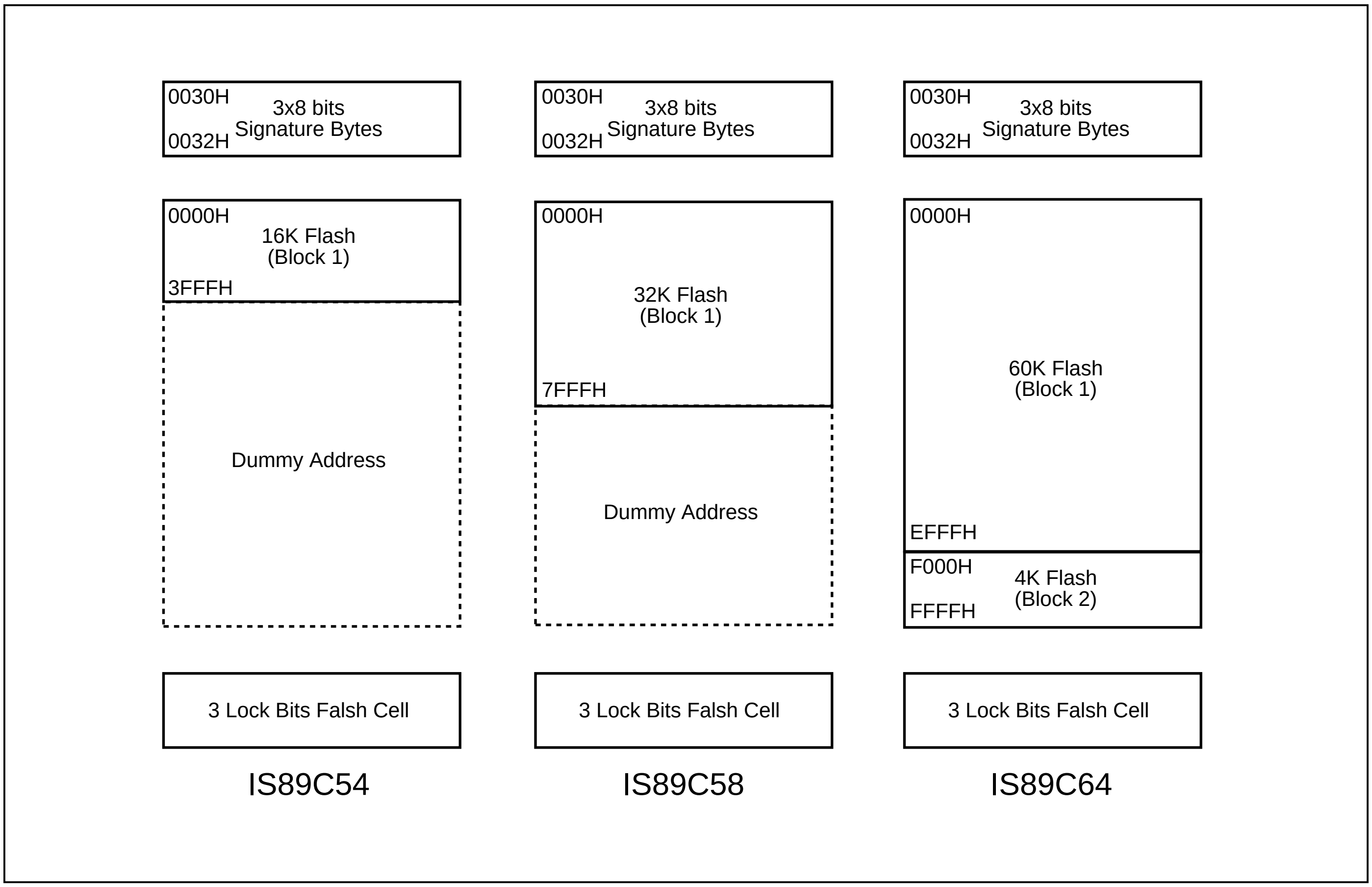


Figure 5. The Flash Architecture of IS89C54/58/64

The IS89C54/58/64 provide the user with a direct flash memory access that can be used for programming into the flash memory without using the CPU. The direct flash memory access is entered using the External Host Mode. While the reset input (RST) is continually held active (high), if the $\overline{\text{PSEN}}$ pin is forced by an input with low state, the device enters the External Host Mode arming state at this time. The CPU core is stopped from running and all the chip I/O pins are reassigned and become flash memory access and control pins. At this time, the external host should initiate a “Read Signature Bytes” operation. After the completion of the “Read Signature Bytes” operation, the device is armed and enters the External Host Mode. After the device enters into the External Host Mode, the internal flash memory blocks are accessed through the re-assigned I/O port pins by an external host, such as a printed circuit board tester, a PC controlled development board or an MCU programmer.

When the chip is in the external host mode, Port 0 pins are assigned to be the parallel data input and output pins. Port 1 pins are assigned to be the low order address bus signals for the internal flash memory (A0-A7). The first six bits of Port 2 pins (P2[0:5]) are assigned to be the upper order address bus signals for the internal flash memory (A8-A13) along with two of the Port 3 pins (P3.2 as A14 and P3.3 as A15). Two upper order Port 2 pins (P2.6 and P2.7) and two upper order Port 3 pins (P3.6 and P3.7) along with RST, $\overline{\text{PSEN}}$, $\overline{\text{PROG}}$/ALE, $\overline{\text{EA}}$ pins are assigned as the control signal pins. The P3.4 is assigned to be the ready/busy status signal, the P3.5 is assigned to be the timeout signal, which can be used for handshaking with the external host during a flash memory programming operation. The flash memory programming operation (Erase, Program, Verify, etc.) is internally self-timed and can be controlled by an external host asynchronously or synchronously.

The insertion of an “arming” command prior to entering the External Host Mode by utilizing the “Read Signature Bytes” operation provides additional protection for inadvertent writes to the internal flash memory cause by a noisy or unstable system environment during the power-up or power unstable conditions.

The External Host Mode uses hardware setup mode, which are decoded from the control signal pins, to facilitate the internal flash memory erase, test and programming process. The External Host Mode Commands are enabled on the falling edge of ALE/$\overline{\text{PROG}}$. The list in Table 3 outlines all the setup conditions of normal mode. Before entering these written modes must have read 3 signature bytes.

Programming Interface

Some conditions must be satisfied before entering the programming mode. The conditions are listed in table 3. The interface-controlled signals are matched these conditions, then the IS89C54/58/64 will enter received command mode. The flash command is accepted by the flash command decoder in command received mode. The programming interface is listed in figure 6.

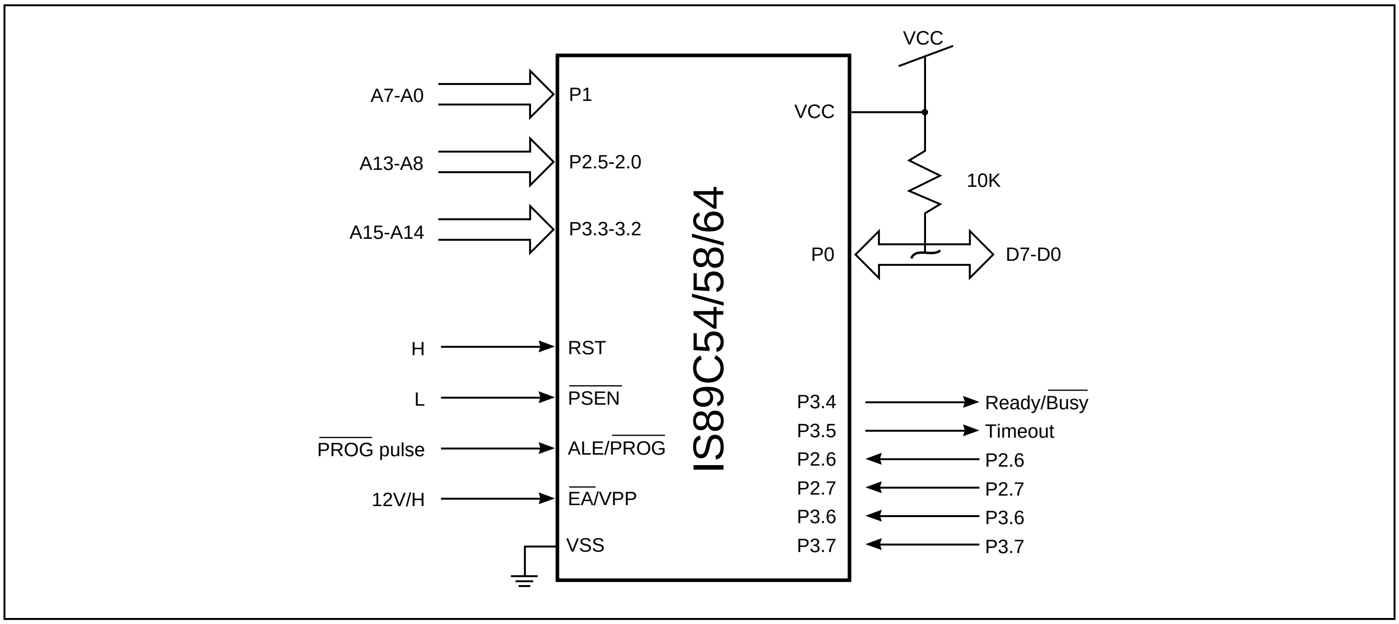


Figure 6. IS89C52/54/64 External Host Programming Signals

Table 3. Flash Programming Mode

Mode(1)	RST	PSEN#	PROG#	EA#	P2.6	P2.7	P3.6	P3.7	P0[7:0]	P1[7:0]	P3[3:2] P2[5:0]	COM HEX(3)
Read Signature Byte	H	L	H	H	L	L	L	L	DO	AL	AH	0
Chip Erase	H	L	⊔	12V/H	H	L	L	L	X	X	X	1
Block 1 (2) Erase	H	L	⊔	12V/H	L	H	L	L	X	X	X	2
Block 2 (2) Erase	H	L	⊔	12V/H	L	L	H	L	X	X	X	4
Program Main code	H	L	⊔	12V/H	L	H	H	H	DI	AL	AH	E
Program Lock Bit 1	H	L	⊔	12V/H	H	H	H	H	X	X	X	F
Program Lock Bit 2	H	L	⊔	12V/H	H	H	L	L	X	X	X	3
Program Lock Bit 3	H	L	⊔	12V/H	H	L	H	L	X	X	X	5
Verify Lock Bits	H	L	H	H	H	L	L	H	DO[3:1]	X	X	9
Verify Main Code	H	L	H	H	L	L	H	H	DO	AL	AH	C

1. To read the signature bytes 30H, 31H, 32H are needed before any written command. To read signature bytes is needed after any new mode changed. This operation provides additional protection for inadvertent writes to the internal flash memory cause by a noisy or unstable system environment during the power-up or unstable power condition. If any unstable power condition has happened while written operation proceeds, to read signature bytes again will re-enable written command. (Power-on reset voltage is about 2.7V.)
2. Block 1 includes flash address from 0000H to 3FFFH in IS89C54, from 0000H to 7FFFH in IS89C58, from 0000H to EFFFH in IS89C64. Block 2 includes F000H to FFFFH. Block 2 is resident in IS89C64 only.
3. "COM HEX" presents the combination value of [P3.7, P3.6, P2.7, P2.6].

Product Identification

The "Read Signature Bytes" command accesses the Signature Bytes that identify the device as IS89C54/58/64 and the manufacturer code. External programmers primarily use these Signature Bytes, shown in Table 4, in the selection of programming algorithms. The Read Signature Bytes command is selected by the byte code of 00h on P3[7:6] and P2[7:6]. Manufacturer code of ICSI is "D5H" that reside in address 30H of signature. The flash memory sizes of MCU are shown in address 31H, code value 04H respect to 16K main flash memory, code value 08H respect to 32K main flash memory, code value 10H respect to 64K main flash memory. The address 32H value of signature byte respect to written operation VPP value, code value FFH respects to 12V and 55H respects to 5V.

Table 4. Signature Bytes Information

	Addr 30H	Addr 31H	Addr 32H
IS89C54 (VPP=12V)	D5H	04H	FFH
IS89C54 (VPP=5V)	D5H	04H	05H
IS89C58 (VPP=12V)	D5H	08H	FFH
IS89C58 (VPP=5V)	D5H	08H	05H
IS89C64 (VPP=12V)	D5H	10H	FFH
IS89C64 (VPP=5V)	D5H	10H	05H

Arming Command

An arming command must take place before a Written Mode will be recognized by the IS89C54/58/64. This is to prevent accidental triggering of written operation due to noise or programmer error. The arming command is as follows:

A Read Signature Bytes command is issued. This is actually a natural step for the programmer, but will also serve as the arming command. After the above sequence, all other Written Mode commands are enabled. Before the Read Signature Bytes command is received, all other Written Mode commands received are ignored. The IS89C54/8/64 will exit Written Mode if power off, so arming command is needed every power on for entering External Host Command Mode.

External Host Mode Commands

The following is a brief description of the commands. See Table 3 for all signal logic assignments for the External Host Mode Commands. The critical timing for all Erase and Program commands, is self-generated by the flash memory controller on-chip.

The high-to-low transition of the $\overline{\text{PROG}}$ signal initiates the Erase and Program commands, which are synchronized internally. All the data in the memory array will be erased to FFH. Memory addresses that are to be programmed must be in the erased state prior to programming. There are two erase commands in IS89C64, Block 1 erase and Block 2 erase. Selection of the Erase command to use, prior to programming the device, will be dependent upon the contents already in the array and the desired programming field block.

The “Chip Erase” command erases all bytes in both memory blocks (16K/32K/64K) of the IS89C54/58/64.This command ignores the “Lock bits” status and will erase the Security Byte. The “Chip Erase” command is selected by the byte code of 01H on P3[7:6] and P2[7:6]. The “Block 1 Erase” command erases all bytes in one of the memory blocks 1 (16/32/60K) of the IS89C54/58/64. The “Block 2 Erase” command erases all bytes in one of the memory blocks 2 (Address range is from F000H to FFFFH) of the IS89C64. These block erase commands will not enable if the Lock Bit 2 or Lock Bit 3 is enabled.

Flash Operation Status Detection (Ext. Host Handshake)

The IS89C54/58/64 provide two signals mean for an external host to detect the completion of a flash memory operation, therefore the external host can optimize the system Program or Erase cycle of the embedded flash memory. The end of a flash memory operation cycle (Erase or Program) can be detected by: 1) monitoring the Ready/$\overline{\text{Busy}}$ bit at Port 3.4; 2) monitoring the Timeout Polling bit at Port 3.5. The following two Program commands are for programming new data into the memory array. Selection of which Program command to use for programming will be dependent upon the desired programming field size. The Program commands will not enable if Lock Bit 2 or Lock Bit 3 is enabled on the selected memory block. The “Program Main Code” command program data into a single byte. Ports P0[0:7] are used for data in. The memory location is selected by P1[0:7], P2[0:5], and P3[2:3] (A0-A15).

The “Verify Main Code” command allows the user to verify that the IS89C54/58/64 correctly performed an Erase or Program command. Ports P0[0:7] are used for data out. The memory location is selected by P1[0:7], P2[0:5], and P3 [2:3] (A0-A15). These commands will not enable if any lock bit is enabled on the selected memory block.

Ready/$\overline{\text{BUSY}}$

The progress of the flash memory programming can be monitored by the Ready/$\overline{\text{BUSY}}$ output signal. The Ready/$\overline{\text{BUSY}}$ indicates whether an Embedded Algorithm in Written State Machine (WSM) is in progress or complete. The RY/$\overline{\text{BY}}$ status is valid after the falling edge of the programming or erase controlled signal. If the output is low (Busy), the device is in an erasing/programming state with an internal verification. If the output is high, the device is ready to read data. While the RY/$\overline{\text{BY}}$ signal is at low level (Busy) and Timeout is high level, the programming or erasing procedure is failed.

Timeout

Timeout indicates whether the program or erase time has exceeded a specified internal timer limit. Under these conditions Timeout go to high and Ready/$\overline{\text{BUSY}}$ remains a low. This is a failed condition that indicates the program or erase cycle was not successful completed. If there are any program or erase failure in erasing operation, Timeout go to high and Ready/$\overline{\text{BUSY}}$ remains low.

It is cleared by any rising edge of written signal (like Program Main Code, Chip Erase, …etc.). The time from written signal to Timeout=1 is re-initiated at every written signal's rising edge. It is high when the program or erase operations don't complete and have no newly written signal in the expected time.

Programming a IS89C54/58/64

To program new data into the memory array, supply 5 volts to VDD and RST, and perform the following steps.

1. Set RST to high and $\overline{\text{PSEN}}$ to low.
2. Raise $\overline{\text{EA}}$ High (either 12V or 5V).
3. Read the "Read Signature Bytes" command to ensure the correct programming algorithm.
4. Verify that the memory blocks for programming are in the erased state, FFH. If they are not erased, then erase them using the appropriate Erase command.
5. Set P2.6, P2.7, P3.6, P3.7 to a properly programming combination.
6. Select the memory location using the address lines (P1 [0:7], P2[0:5], P3[2:3]).
7. Present the data in on P0[0:7].
8. Pulse ALE/$\overline{\text{PROG}}$.
9. Wait for low to high transition on Ready/$\overline{\text{Busy}}$(P3.4) or Timeout pin(P3.5). If Ready/$\overline{\text{Busy}}$ is from low to high, this address is programmed completely. If the Timeout signal is from low to high before Ready/$\overline{\text{Busy}}$ goes high, this byte is failed in programming.
10. Repeat steps 6~9 until programming is finished.

Lock bits Features

The IS89C54/58/64 provide three lock bits to protect the embedded program against software piracy. These three bytes are user programmable. The relation between lock bits status and protection type are listed in table 5.

Table 5. Lock Bits Features

Program Lock bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock feature enabled.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, #EA is sampled and latched on reset, and Data verification is disabled. ("Verify Signature Byte" and "Verify Lock Bits are still enabled.)
3	P	P	U	Same as 2, also further written operation of the Flash is disabled
4	P	P	P	Same as 3, also external execution is disabled

Absolute Maximum Ratings

Parameter	Rating	Unit
Operating temperature under bias	0 to +70	°C (1)
Storage temperature range	-65 to +125	°C
Voltage on any other pin to VSS	-2.0 to +7.0	V (2)
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

Notes :

1. Operating temperature is for commercial product defined by this spec.
2. Minimum D.C. input voltage is -0.5 V. During transitions, inputs may undershoot, to -2.0 V for periods less than 20 ns. Maximum D.C. voltage on output pins is VCC+0.5 V, which may overshoot to VCC + 2.0 V for periods less than 20 ns.

Warning:

Stressing the device beyond the “Absolute Maximum Rating” may cause permanent damage. This is stress rating only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “operating conditions” may affect device reliability.

Operating Range

Commercial devices case temperature	0 to +70 °C
VCC supply voltage	+4.5 to 5.5 V
Oscillator frequency	3.5 to 40 MHz

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(Ta=0°C to 70°C; VCC=5V+10%; VSS=0V)

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{IL}	Input low voltage (All except $\overline{EA}$)		–0.5	0.2Vcc – 0.1	V
$V_{IL}1$	Input low voltage ($\overline{EA}$)		–0.5	0.2Vcc – 0.3	V
V_{IH}	Input high voltage (All except XTAL 1, RST)		0.2Vcc + 0.9	Vcc + 0.5	V
$V_{IH}1$	Input high voltage (XTAL 1)		0.7Vcc	Vcc + 0.5	V
$V_{SCH}+$	RST positive schmitt-trigger threshold voltage		0.7Vcc	Vcc + 0.5	V
$V_{SCH}–$	RST negative schmitt-trigger threshold voltage		0	0.3Vcc	V
V_{OL}(1)	Output low voltage (Ports 1, 2, 3)	Iol = 100 µA	—	0.3	V
		I_{OL} = 1.6 mA	—	0.45	V
		I_{OL} = 3.5 mA	—	1.0	V
$V_{OL}1$(1)	Output low voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 200 µA	—	0.3	V
		I_{OL} = 3.2 mA	—	0.45	V
		I_{OL} = 7.0 mA	—	1.0	V
V_{OH}	Output high voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = –10 µA Vcc = 4.5V-5.5V	0.9Vcc	—	V
		I_{OL} = –25 µA	0.75Vcc	—	V
		I_{OL} = –60 µA	2.4	—	V
$V_{OH}1$	Output high voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OH} = –80 µA Vcc = 4.5V-5.5V	0.9Vcc	—	V
		I_{OH} = –300 µA	0.75Vcc	—	V
		I_{OH} = –800 µA	2.4	—	V
I_{IL}	Logical 0 input current (Ports 1, 2, 3)	V_{IN} = 0.45V	—	–50	µA
I_{LI}	Input leakage current (Port 0)	0.45V < V_{IN} < Vcc	–10	+10	µA
I_{TL}	Logical 1-to-0 transition current (Ports 1, 2, 3)	V_{IN} = 2.0V	—	–650	µA
R_{RST}	RST pulldown resister	V_{IN}=0v	50	300	KΩ

Note:

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink greater than the listed test conditions.
2. The Icc test conditions are shown below. Minimum VCC for Power Down is 2 V.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Max	Unit
Icc	Power supply current[1]	Vcc = 5.0V			
	Active mode	12 MHz	—	20	mA
		16 MHz	—	26	mA
		20 MHz	—	32	mA
		24 MHz	—	38	mA
		32 MHz	—	50	mA
		40 MHz	—	62	mA
	Idle mode	12 MHz	—	5	mA
		16 MHz	—	6	mA
		20 MHz	—	7.6	mA
		24 MHz	—	9	mA
		32 MHz	—	12	mA
		40 MHz	—	15	mA
	Power-down mode	Vcc = 5V	—	50	µA

Note:
1. See Figures7,8,9, and 10 for Icc test conditiions.

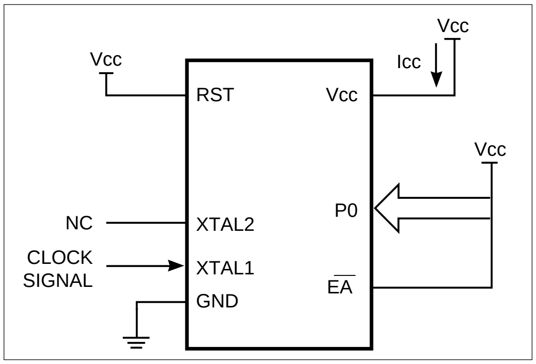


Figure 7. Active Mode

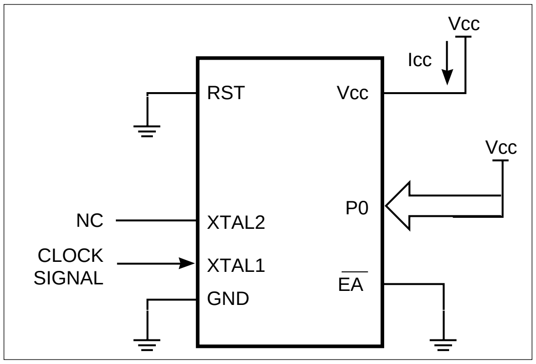


Figure 8. Active Mode

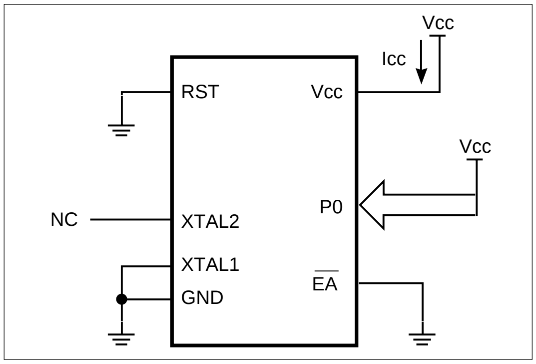


Figure 9. Active Mode

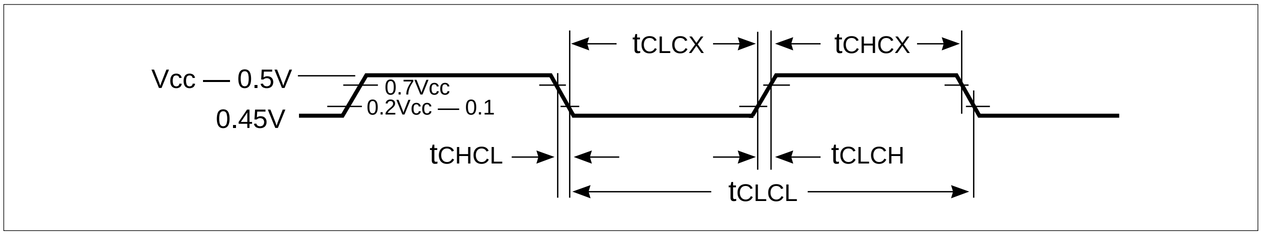


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode (t_{CLCH}=t_{CHCL}=5 ns)

AC CHARACTERISTICS

(Ta=0°C to 70°C; VCC=5V+10%; V_{SS}=0V; C1 for port 0, ALE and $\overline{PSEN}$ Outputs=100pF; C1 for other outputs=80pF)

EXTERNAL MEMORY CHARACTERISTICS

		24 MHz Clock		40 MHz Clock		Variable Oscillator (3.5 - 40 MHz)		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
$1/t_{CLCL}$	Oscillator frequency	—	—	—	—	3.5	40	MHz
t_{LHLL}	ALE pulse width	68	—	35	—	$2t_{CLCL}-15$	—	ns
t_{AVLL}	Address valid to ALE low	26	—	10	—	$t_{CLCL}-15$	—	ns
t_{LLAX}	Address hold after ALE low	31	—	15	—	$t_{CLCL}-10$	—	ns
t_{LLIV}	ALE low to valid instr in	—	147	—	80	—	$4t_{CLCL}-20$	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	31	—	15	—	$t_{CLCL}-10$	—	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	110	—	60	—	$3t_{CLCL}-15$	—	ns
t_{PLIV}	$\overline{PSEN}$ low to valid instr in	—	105	—	55	—	$3t_{CLCL}-20$	ns
t_{PXIX}	Input instr hold after $\overline{PSEN}$	0	—	0	—	0	—	ns
t_{PXIZ}	Input instr float after $\overline{PSEN}$	—	37	—	20	—	$t_{CLCL}-5$	ns
t_{AVIV}	Address to valid instr in	—	188	—	105	—	$5t_{CLCL}-20$	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float	—	10	—	10	—	10	ns
t_{RLRH}	$\overline{RD}$ pulse width	230	—	130	—	$6t_{CLCL}-20$	—	ns
t_{WLWH}	$\overline{WR}$ pulse width	230	—	130	—	$6t_{CLCL}-20$	—	ns
t_{RLDV}	$\overline{RD}$ low to valid data in	—	157	—	90	—	$4t_{CLCL}-10$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	—	0	—	0	—	ns
t_{RHDZ}	Data float after $\overline{RD}$	—	78	—	45	—	$2t_{CLCL}-5$	ns
t_{LLDV}	ALE low to valid data in	—	282	—	165	—	$7t_{CLCL}-10$	ns
t_{AVDV}	Address to valid data in	—	323	—	190	—	$8t_{CLCL}-10$	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	105	145	55	95	$3t_{CLCL}-20$	$3t_{CLCL}+20$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ low	146	—	80	—	$4t_{CLCL}-20$	—	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	26	—	10	—	$t_{CLCL}-15$	—	ns
t_{WHQX}	Data hold after $\overline{WR}$	31	—	15	—	$t_{CLCL}-10$	—	ns
t_{RLAZ}	$\overline{RD}$ low to address float	—	0	—	0	—	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	26	57	10	40	$t_{CLCL}-15$	$t_{CLCL}+15$	ns

SERIAL PORT TIMING: SHIFT REGISTER MODE

Symbol	Parameter	24 MHz Clock Min	24 MHz Clock Max	40 MHz Clock Min	40 MHz Clock Max	Variable Oscillator (3.5-40 MHz) Min	Variable Oscillator (3.5-40 MHz) Max	Unit
t_{XLXL}	Serial port clock cycle time	490	510	290	310	$12t_{CLCL}-10$	$12t_{CLCL}+10$	ns
t_{QVXH}	Output data setup to clock rising edg1	406	—	240	—	$10t_{CLCL}-10$	—	ns
t_{XHQX}	Output data hold after clock rising edge	73	—	40	—	$2t_{CLCL}-10$	—	ns
t_{XHDX}	Input data hold after clock rising edge	0	—	0	—	0	—	ns
t_{XHDV}	Clock rising edge to input data valid	—	417	—	250	—	$10t_{CLCL}$	ns

EXTERNAL CLOCK DRIVE CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
$1/t_{CLCL}$	Oscillator Frequency	3.5	40	MHz
t_{CHCX}	High time	10	—	ns
t_{CLCX}	Low time	10	—	ns
t_{CLCH}	Rise time	—	10	ns
t_{CHCL}	Fall time	—	10	ns

Flash Program/Erase and Verification Characteristics

Symbol	Parameter	Min	Max	Unit
Vpph	Programming and Erase Enable Voltage	11.5	12.5	V
Vppl	Programming and Erase Enable Voltage	4.5	6.0	V
Ipph	Programming and Erase Enable Current while VPP=Vpph	-	2.0	mA
Ippl	Programming and Erase Enable Current while VPP=Vppl	-	1.0	mA
tWSCV	Power Setup to Command Setup Low	10	-	ms
tCVQV	Command Valid to Data Output Valid	-	60	ns
tAVQV	Address Valid to Data Output Valid	-	60	ns
tCVPL	Command Valid to PROG# Low	30	-	ns
tSHPL	VPP Setup to PROG# Low	30	-	ns
tAVPL	Address Setup to PROG# Low	30	-	ns
tDVPL	Data Setup to PROG# Low	30	-	ns
tPLBL	PROG# Low to Busy# Low	1	10	us
tPLTL	PROG# Low to Timeout Low	-	30	ns
tBLCX	Command Hold after Busy# Low	30	-	ns
tBLAX	Address Hold after Busy# Low	30	-	ns
tBLPH	Busy# Low to PROG# high	30	-	ns
tBLDX	Data Hold after Busy# Low	30	-	us
tBLBH	Busy# Low to Busy# High	15	480	us
tBLTH	Busy# Low to Timeout High	180	720	us
tBHSL	VPP Hold after Busy# High	1	-	us
tAXQX	Output Hold after Address Release	0	-	ns
tCXQX	Output Hold after Command Release	0	-	ns
tBLBHE	Busy# Time while Chip Erase	-	4.5	Sec
tBLBHE1	Busy# Time while Block 1 Erase (IS89C54)	-	1.2	Sec
tBLBHE2	Busy# Time while Block 1 Erase (IS89C58)	-	2.4	Sec
tBLBHE3	Busy# Time while Block 1 Erase (IS89C64)	-	4.0	Sec
tBLBHE4	Busy# Time while Block 2 Erase (IS89C64)	-	0.7	Sec
tBLTHE	Busy# Low to Timeout High while Chip Erase	0.00018	6.75	Sec
tBLTHE1	Busy# Low to Timeout High while Block 1 Erase (IS89C54)	0.00018	1.8	Sec
tBLTHE2	Busy# Low to Timeout High while Block 1 Erase (IS89C58)	0.00018	3.6	Sec
tBLTHE3	Busy# Low to Timeout High while Block 1 Erase (IS89C64)	0.00018	6.0	Sec
tBLTHE4	Busy# Low to Timeout High while Block 2 Erase (IS89C64)	0.00018	1.05	Sec

TIMING WAVEFORMS

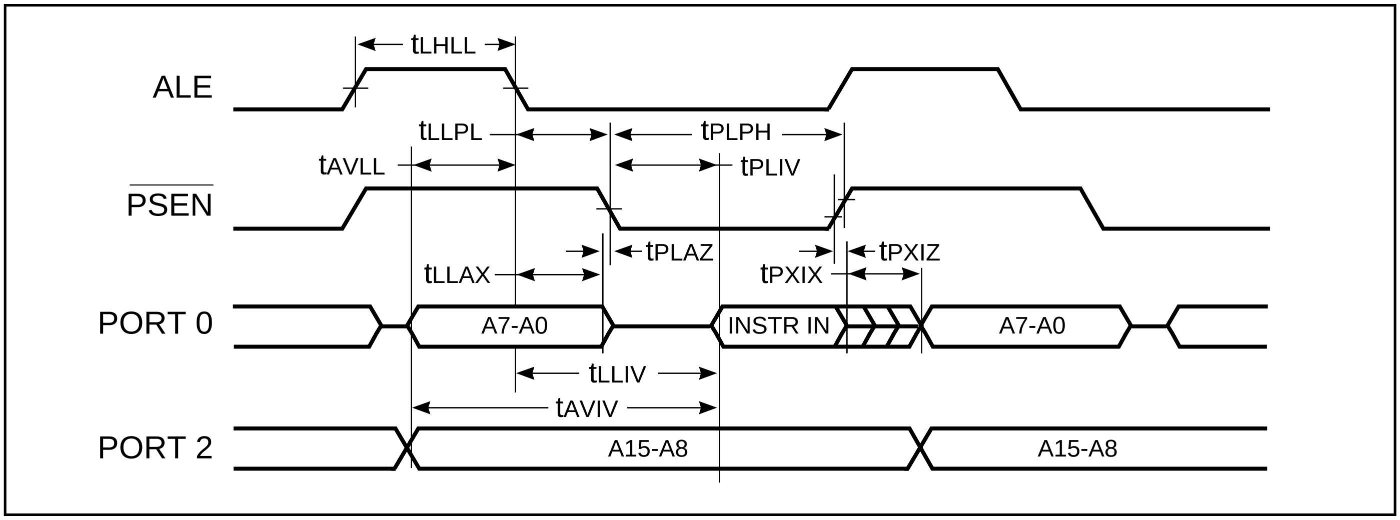


Figure 11. External Program Memory Read Cycle

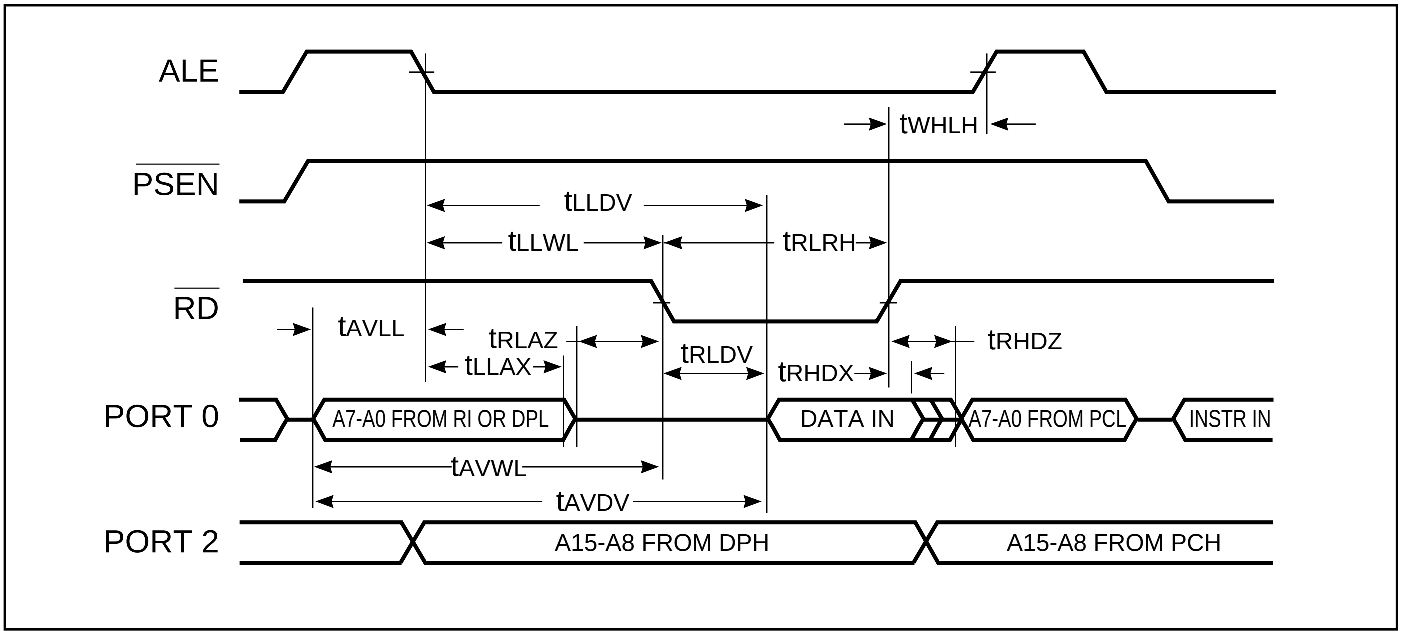


Figure 12. External Data Memory Read Cycle

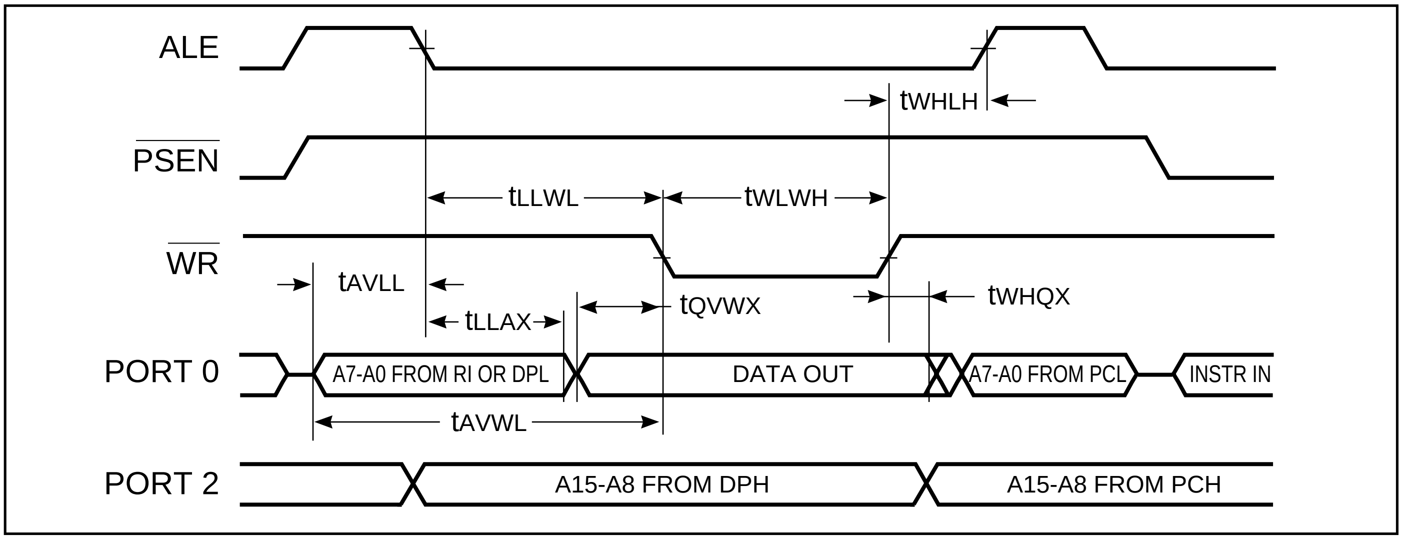


Figure 13. External Data Memory Write Cycle

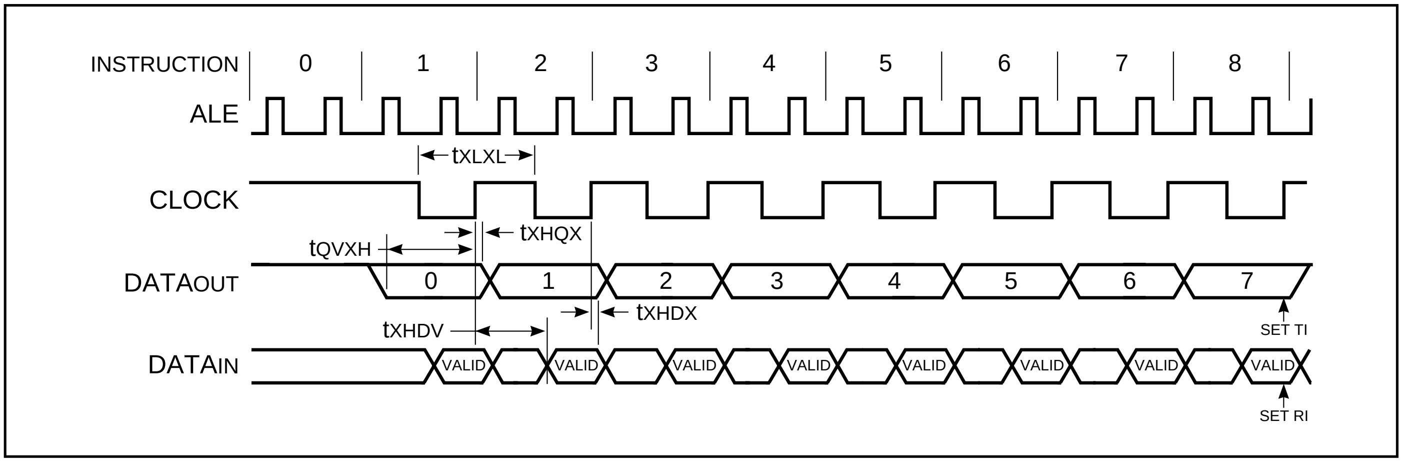


Figure 14. Shift Register Mode Timing Waveform

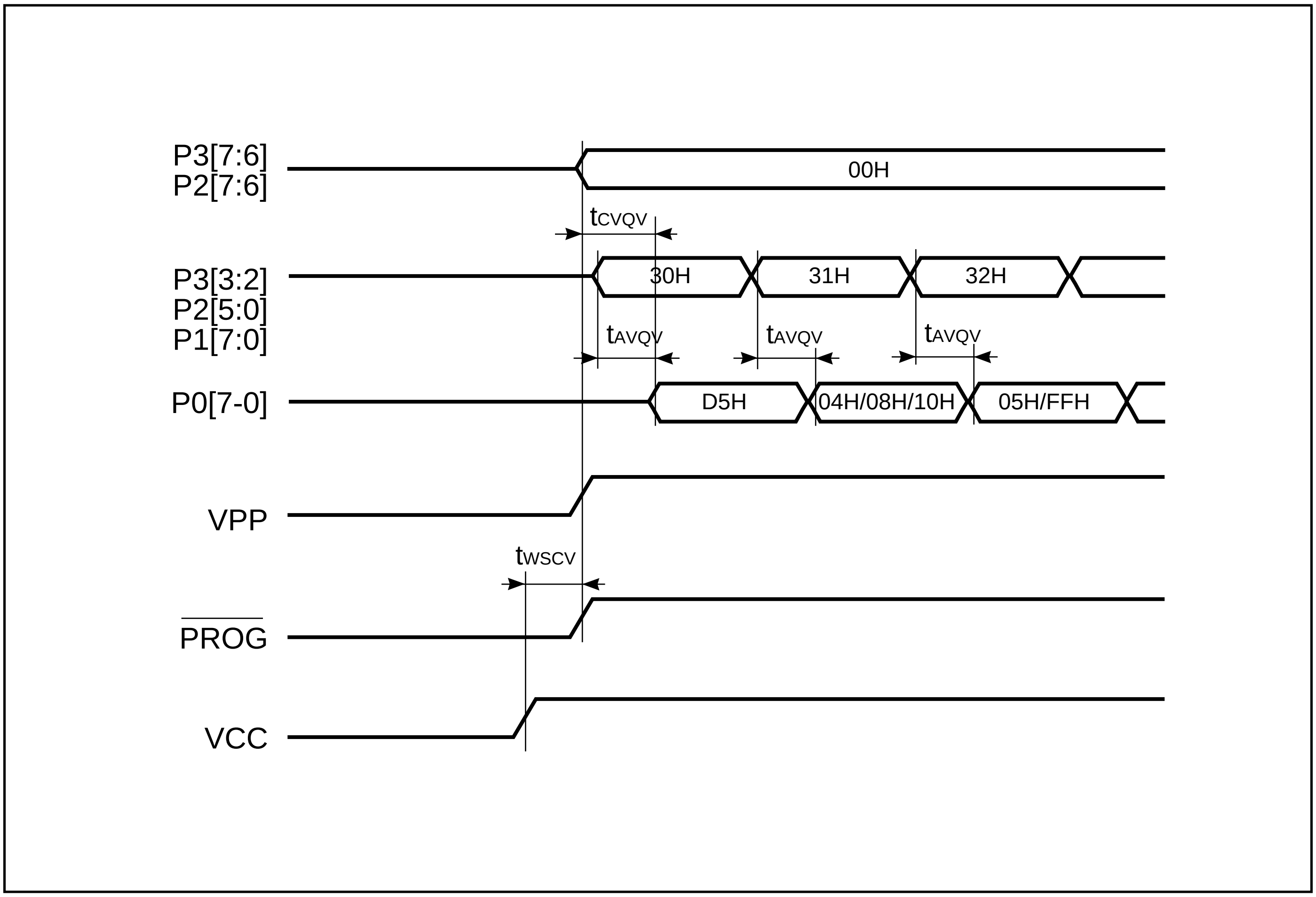
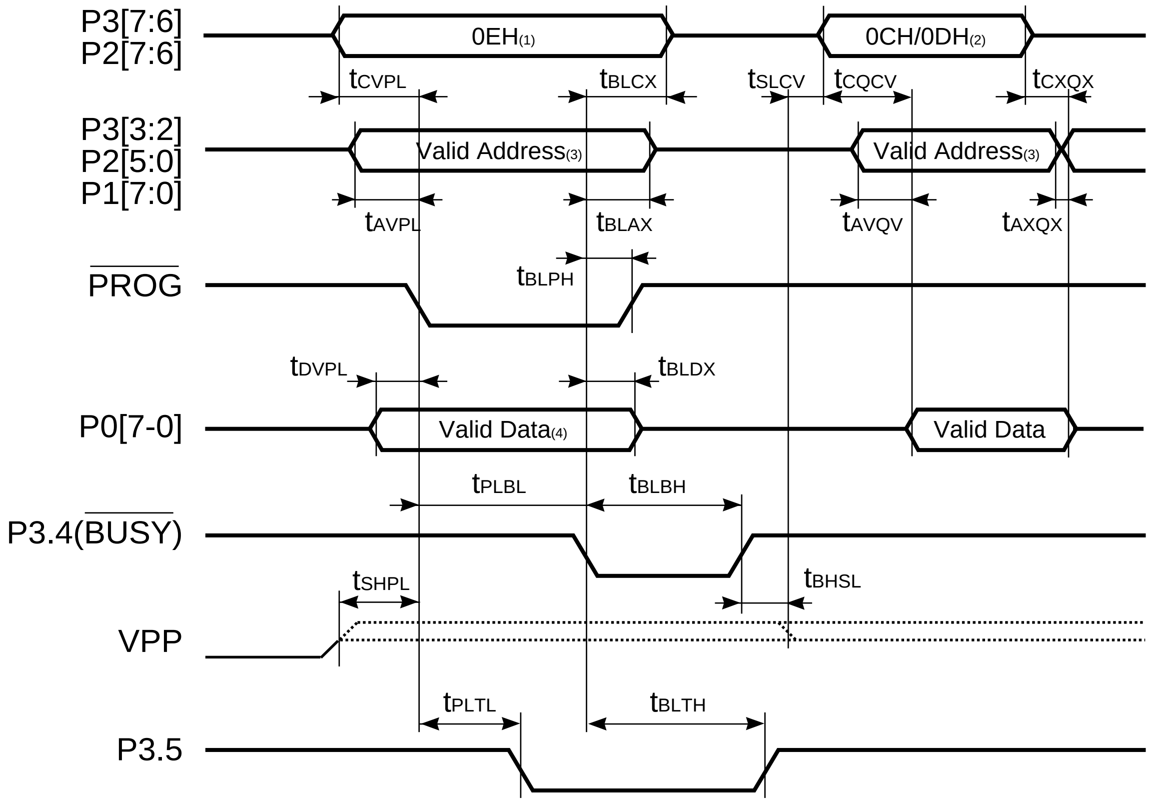
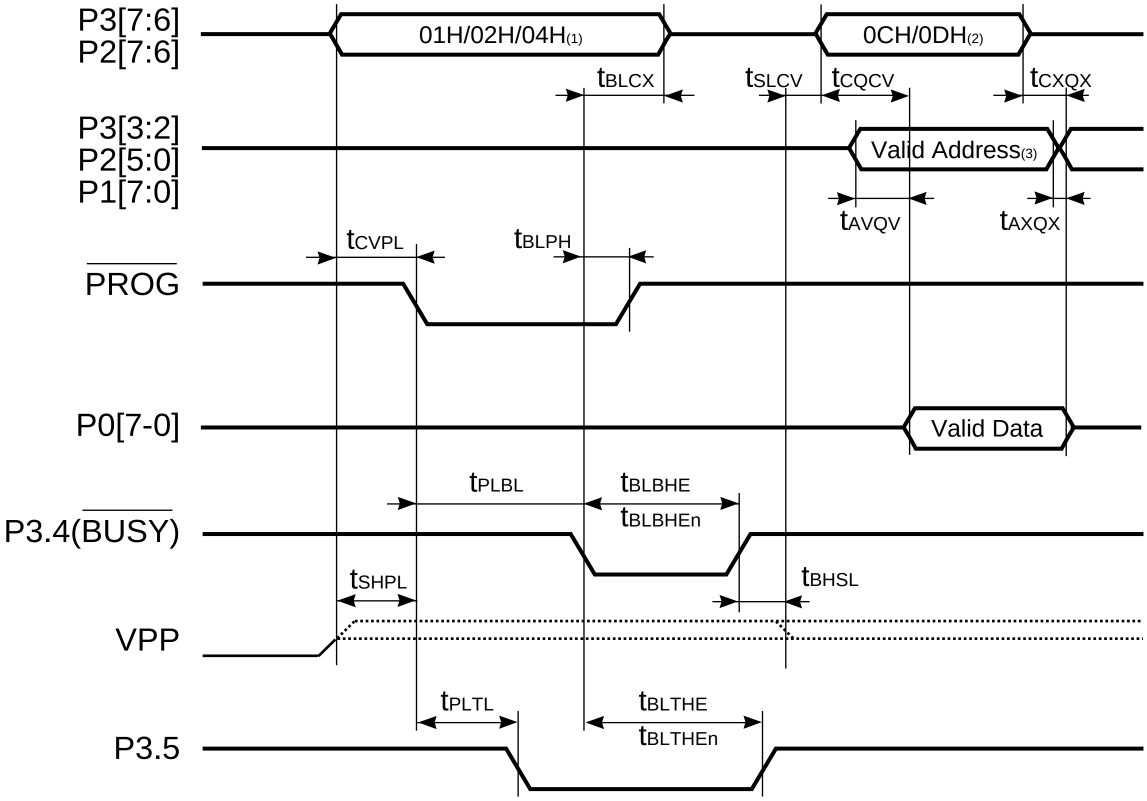


Figure 15. Read Signature bytes Timing(Arming Command)



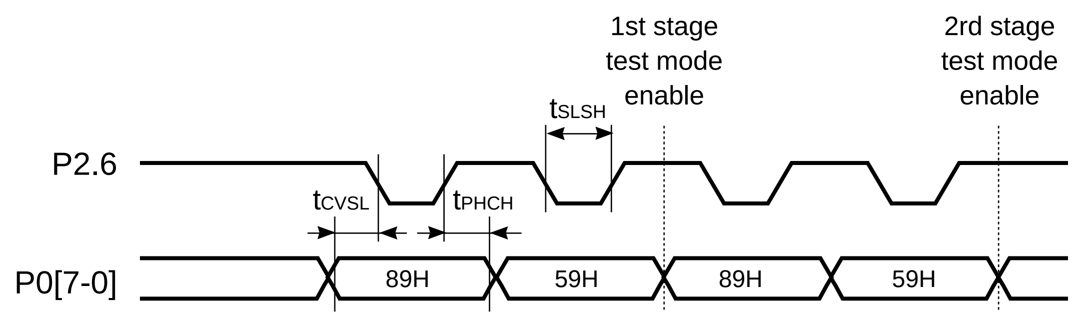
1. 0EH is for code memory programming. In lock bits programming, 0FH, 03H, 05H, respect to lock bits 1, 2, 3.
2. 0CH is for code memory verification and 0DH is for concurrent memory verification. 09H is for Lock bits verification.
3. Address don't care while lock bits' programming or verification.
4. Data don't care while lock bits' programming.

Figure 16. Programming Timing



1. 01H/02H/04H are for Chip Erase/Block 1 Erase/Block 2 Erase.
2. 0CH is for code memory verification and 0DH is for concurrent memory verification. 09H is for Lock bits verification.

Figure 17. Erasing Timing



1. EA#, PROG#, P3.7, P2.7 are high level; P3.6 is low level.

Figure 18. Test Mode Entering Timing

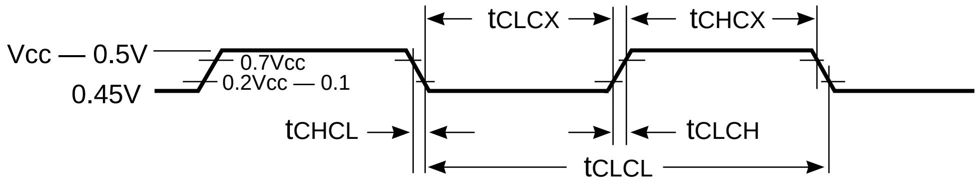


Figure 19. External Clock Drive Waveform

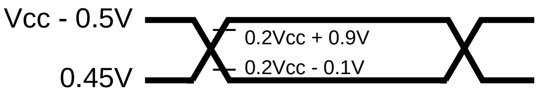


Figure 20. AC Test Point

Note:

1.AC inputs during testing are driven at Vcc-0.5v for logic “1” and 0.45V for logic “0”. Timing measurements are made at Vih min for logic “1” and max for logic “0”.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
12 MHz	IS89C54/58/64-12PL	PLCC
	IS89C54/58/64-12W	600mil DIP
	IS89C54/58/64-12PQ	PQFP
24 MHz	IS89C54/58/64-24PL	PLCC
	IS89C54/58/64-24W	600mil DIP
	IS89C54/58/64-24PQ	PQFP
40 MHz	IS89C54/58/64-40PL	PLCC
	IS89C54/58/64-40W	600mil DIP
	IS89C54/58/64-40PQ	PQFP

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