Micro PMU with 1.2 A Buck, Two 300 mA LDOs, Supervisory, Watchdog, and Manual Reset

Data Sheet

ADP5041

FEATURES

- Input voltage range: 2.3 V to 5.5 V
- One 1.2 A buck regulator
- Two 300 mA LDOs
- 20-lead, 4 mm × 4 mm LFCSP package
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Open-drain processor reset with externally adjustable threshold monitoring
- Guaranteed reset output valid to V_{AVIN} = 1 V
- Manual reset input
- Watchdog refresh input
- Buck key specifications
  - Output voltage range: 0.8 V to 3.8 V
  - Current mode topology for excellent transient response
  - 3 MHz operating frequency
  - Peak efficiency up to 96%
  - Uses tiny multilayer inductors and capacitors
  - Mode pin selects forced PWM or auto PWM/PSM mode
  - 100% duty cycle low dropout mode
- LDOs key specifications
  - Output voltage range: 0.8 V to 5.2 V
  - Low input supply voltage from 1.7 V to 5.5 V
  - Stable with 2.2 µF ceramic output capacitors
  - High PSRR
  - Low output noise
  - Low dropout voltage
  - −40°C to +125°C junction temperature range

FUNCTIONAL BLOCK DIAGRAM

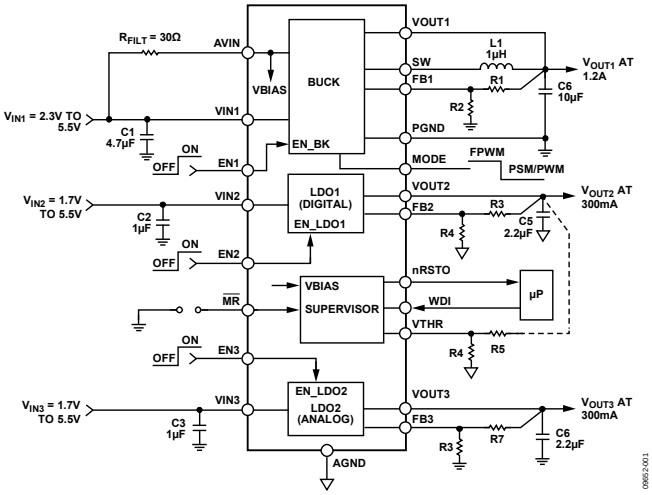

Figure 1.

GENERAL DESCRIPTION

The ADP5041 combines one high performance buck regulator and two low dropout regulators (LDO) in a small 20-lead LFCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulator enables use of tiny multilayer external components and minimizes board space.

When the MODE pin is set to logic high, the buck regulator operates in forced PWM mode. When the MODE pin is set to logic low, the buck regulator operates in PWM mode when the load is around the nominal value. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM), improving the light load efficiency. The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5041 LDOs extend the battery life of portable devices. The ADP5041 LDOs maintain a power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Each regulator in the ADP5041 is activated by a high level on the respective enable pin. The output voltages of the regulators and the reset threshold are programmed through external resistor dividers to address a variety of applications. The ADP5041 contains supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. They also provide power-on reset signals. An on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period.

Rev. 0

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REVISION HISTORY

12/11—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; AVIN, VIN1 ≥VIN2, VIN3; VIN2, VIN3 = 1.7 V to 5.5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AVIN UNDERVOLTAGE LOCKOUT	$UVLO_{AVIN}$					
Input Voltage Rising	$UVLO_{AVINRISE}$					
Option 0					2.275	V
Option 1					3.9	V
Input Voltage Falling	$UVLO_{AVINFALL}$					
Option 0			1.95			V
Option 1			3.1			V
SHUTDOWN CURRENT	I_{GND-SD}	ENx = GND		0.1	2	µA
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			20		°C
START-UP TIME[1]						
Buck	t_{START1}			250		µs
LDO1, LDO2	t_{START2}	V_{OUT2}, V_{OUT3} = 3.3 V		85		µs
ENx, WDI, MODE, $\overline{MR}$ INPUTS						
Input Logic High	V_{IH}	2.5 V ≤ AVIN ≤ 5.5 V	1.2			V
Input Logic Low	V_{IL}	2.5 V ≤ AVIN ≤ 5.5 V			0.4	V
Input Leakage Current	$V_{I-LEAKAGE}$	ENx = AVIN or GND		0.05	1	µA
OPEN-DRAIN OUTPUT						
nRSTO Output Voltage	V_{OL1V}	AVIN ≥ 1.0 V, I_{SINK} = 50 µA			0.3	V
	V_{OL1V2}	AVIN ≥ 1.2 V, I_{SINK} = 100 µA			0.3	V
	V_{OL2V7}	AVIN ≥ 2.7 V, I_{SINK} = 1.2 mA			0.3	V
	V_{OL4V5}	AVIN ≥ 4.5 V, I_{SINK} = 3.2 mA			0.4	V
Open-Drain Reset Output Leakage Current		AVIN = 5.5 V			1	µA

[1] Start-up time is defined as the time from the moment EN1 = EN2 = EN3 transfers from 0 V to VAVIN to the moment VOUT1, VOUT2, and VOUT3 are reaching 90% of their nominal levels. Start-up times are shorter for individual channels if another channel is already enabled. See the Typical Performance Characteristics section for more information.

SUPERVISORY SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
Supply Current (Supervisory Circuit Only)		45	55	µA	AVIN = VIN1 = EN1 = EN2 = EN3 = 5.5 V
		43	52	µA	AVIN = VIN1 = EN1 = EN2 = EN3 = 3.6 V
THRESHOLD VOLTAGE	0.495	0.500	0.505	V	
RESET TIMEOUT PERIOD					
Option 0	24	30	36	ms	
Option 1	160	200	240	ms	
V_{CC} TO RESET DELAY (t_{RD})		80		µs	VIN falling at 1 mV/µs

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT					
Watchdog Timeout Period					
Option 0	81.6	102	122.4	ms	
Option 1	1.28	1.6	1.92	sec	
WDI Pulse Width	80			ns	V_{IL} = 0.4 V, V_{IH} = 1.2 V
WDI Input Threshold	0.4		1.2	V	
WDI Input Current (Source)	8	15	20	µA	$V_{WDI} = V_{CC}$, time average
WDI Input Current (Sink)	−30	−25	−15	µA	V_{WDI} = 0 V, time average
MANUAL RESET INPUT					
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		220		ns	
$\overline{MR}$ Pull-Up Resistance	25	52	90	kΩ	
$\overline{MR}$ to Reset Delay		280		Ns	V_{CC} = 5 V

BUCK SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; V_{OUT1} = 1.8 V; L = 1 µH; C_{IN} = 10 µF; C_{OUT} = 10 µF; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Voltage Range	V_{IN1}		2.3		5.5	V
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	V_{OUT1}	PWM mode, I_{LOAD} = 0 mA to 1200 mA	−3		+3	%
Line Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta V_{IN1}$	PWM mode		−0.05		%/V
Load Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta I_{OUT1}$	I_{LOAD} = 0 mA to 1200 mA, PWM mode		−0.1		%/A
VOLTAGE FEEDBACK	V_{FB1}		0.485	0.5	0.515	V
PWM TO POWER SAVE MODE CURRENT THRESHOLD	I_{PSM_L}			100		mA
INPUT CURRENT CHARACTERISTICS		MODE = ground				
DC Operating Current	I_{NOLOAD}	I_{LOAD} = 0 mA, device not switching, all other channels disabled		21	35	µA
Shutdown Current	I_{SHTD}	EN1 = 0 V, $T_A = T_J$ = −40°C to +125°C		0.2	1.0	µA
SW CHARACTERISTICS						
SW On Resistance	R_{PFET}	PFET, AVIN = VIN1 = 3.6 V		180	240	mΩ
		PFET, AVIN = VIN1 = 5 V		140	190	mΩ
	R_{NFET}	NFET, AVIN = VIN1 = 3.6 V		170	235	mΩ
		NFET, AVIN = VIN1 = 5 V		150	210	mΩ
Current Limit	I_{LIMIT}	PFET switch peak current limit	1600	1950	2300	mA
ACTIVE PULL-DOWN		EN1 = 0 V		85		Ω
OSCILLATOR FREQUENCY	f_{OSC}		2.5	3.0	3.5	MHz

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

LDO1, LDO2 SPECIFICATIONS

V_{IN2}, V_{IN3} = (V_{OUT2},V_{OUT3} + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V; AVIN, VIN1 ≥ VIN2, VIN3; C_{IN} = 1 µF, C_{OUT} = 2.2 µF; T_J= −40°C to +125°C for minimum/maximum specifications and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN2}, V_{IN3}	T_J = −40°C to +125°C	1.7		5.5	V
OPERATING SUPPLY CURRENT						
Bias Current per LDO[2]	$I_{VIN2BIAS}$/$I_{VIN3BIAS}$	I_{OUT3} = I_{OUT4} = 0 µA		10	30	µA
		I_{OUT2} = I_{OUT3} = 10 mA		60	100	µA
		I_{OUT2} = I_{OUT3} = 300 mA		165	245	µA
Total System Input Current	I_{IN}	Includes all current into AVIN, VIN1, VIN2, and VIN3				
LDO1 or LDO2 Only		I_{OUT2} = I_{OUT3} = 0 µA, all other channels disabled		53		µA
LDO1 and LDO2 Only		I_{OUT2} = I_{OUT3} = 0 µA, buck disabled		74		µA
OUTPUT VOLTAGE ACCURACY	V_{OUT2}, V_{OUT3}	100 µA < I_{OUT2} < 300 mA, 100 µA < I_{OUT3} < 300 mA VIN2 = (VOUT2 + 0.5 V) to 5.5 V VIN3 = (VOUT3 + 0.5 V) to 5.5 V	−3		+3	%
REFERENCE VOLTAGE	V_{FB2},V_{FB3}		0.485	0.500	0.515	V
REGULATION						
Line Regulation	(ΔV_{OUT2}/V_{OUT2})/ΔV_{IN2} (ΔV_{OUT3}/V_{OUT3})/ΔV_{IN3}	VIN2 = (VOUT2 + 0.5 V) to 5.5 V VIN3 = (VOUT3 + 0.5 V) to 5.5 V I_{OUT2} = I_{OUT3} = 1 mA	−0.03		+0.03	%/V
Load Regulation[3]	(ΔV_{OUT2}/V_{OUT2})/ΔI_{OUT2} (ΔV_{OUT3}/V_{OUT3})/ΔI_{OUT3}	I_{OUT2} = I_{OUT3} = 1 mA to 300 mA		0.002	0.0075	%/mA
DROPOUT VOLTAGE[4]	$V_{DROPOUT}$					
		V_{OUT2} = V_{OUT3} = 5.0 V, I_{OUT2} = I_{OUT3} = 300 mA		72		mV
		V_{OUT2} = V_{OUT3} = 3.3 V, I_{OUT2} = I_{OUT3} = 300 mA		86	140	mV
		V_{OUT2} = V_{OUT3} = 2.5 V, I_{OUT2} = I_{OUT3} = 300 mA		107		mV
		V_{OUT2} = V_{OUT3} = 1.8 V, I_{OUT2} = I_{OUT3} = 300 mA		180		mV
ACTIVE PULL-DOWN	R_{PDLDO}	EN2/EN3 = 0 V		600		Ω
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}	T_J = −40°C to +125°C	335	470		mA
OUTPUT NOISE	$OUT_{LDO2NOISE}$	10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 3.3 V		123		µV rms
		10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 2.8 V		110		µV rms
		10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 1.5 V		59		µV rms
	$OUT_{LDO1NOISE}$	10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 3.3 V		140		µV rms
		10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 2.8 V		129		µV rms
		10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 1.5 V		66		µV rms
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2}, V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		66		dB
		100 kHz, V_{IN2},V_{IN3} = 3.3 V, V_{OUT2},V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		57		dB
		1 MHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2},V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		60		dB

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] This is the input current into VIN2 and VIN3 that is not delivered to the output load.
[3] Based on an end-point calculation using 1 mA and 300 mA loads.
[4] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 1.7 V.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CAPACITANCE (BUCK)[1]	C_{MIN1}	T_J = −40°C to +125°C	4.7		40	µF
OUTPUT CAPACITANCE (BUCK)[2]	C_{MIN2}	T_J = −40°C to +125°C	7		40	µF
INPUT AND OUTPUT CAPACITANCE[3] (LDO1, LDO2)	C_{MIN34}	T_J = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_J = −40°C to +125°C	0.001		1	Ω

[1] The minimum input capacitance should be greater than 4.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with the buck.

[2] The minimum output capacitance should be greater than 7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with the buck.

[3] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with LDOs.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVIN to AGND	−0.3 V to +6 V
VIN1 to AVIN	−0.3 V to +0.3 V
PGND to AGDN	−0.3 V to +0.3 V
VIN2, VIN3, VOUTx, ENx, MODE, $\overline{MR}$, WDI, nRSTO, FBx, VTHR, SW to AGND	−0.3 V to (AVIN + 0.3 V)
SW to PGND	−0.3 V to (VIN1 + 0.3 V)
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020
ESD Human Body Model	3000 V
ESD Charged Device Model	1500 V
ESD Machine Model	200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead, 0.5 mm pitch LFCSP	38	4.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

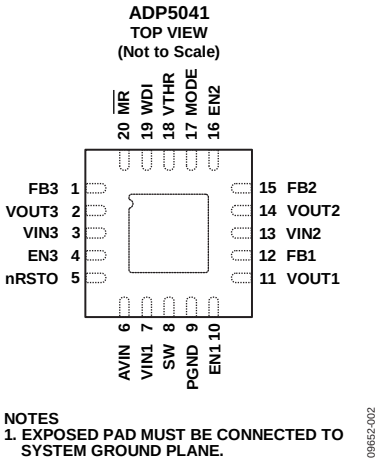


Figure 2. Pin Configuration—View from Top of the Die

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB3	LDO2 Feedback Input.
2	VOUT3	LDO2 Output Voltage.
3	VIN3	LDO2 Input Supply (1.7 V to 5.5 V).
4	EN3	Enable LDO2. EN3 = high: turn on LDO2; EN3 = low: turn off LDO2.
5	nRSTO	Open-Drain Reset Output, Active Low.
6	AVIN	Housekeeping and Supervisory Input Supply (2.3 V to 5.5 V).
7	VIN1	Buck Input Supply (2.3 V to 5.5 V).
8	SW	Buck Switching Node.
9	PGND	Dedicated Power Ground for Buck Regulator.
10	EN1	Enable Buck. EN1 = high: turn on buck; EN1 = low: turn off buck.
11	VOUT1	Buck Output Sensing Node.
12	FB1	Buck Feedback Input.
13	VIN2	LDO1 Input Supply (1.7 V to 5.5 V).
14	VOUT2	LDO1 Output Voltage.
15	FB2	LDO1 Feedback Input.
16	EN2	Enable LDO1. EN2 = high: turn on LDO1; EN2 = low: turn off LDO1.
17	MODE	Buck Mode. MODE = high; buck regulator operates in fixed PWM mode; MODE = low; buck regulator operates in power saving mode (PSM) at light load and in constant PWM at higher load.
18	VTHR	Reset Threshold Programming.
19	WDI	Watchdog Refresh Input from Processor. If WDI is in high-Z, watchdog is disabled.
20	$\overline{\text{MR}}$	Manual Reset Input, Active Low.
0	EPAD	Exposed Pad (Analog Ground). The exposed pad must be connected to the system ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN1 = VIN2 = VIN3 = AVIN = 5.0 V, T_A = 25°C, unless otherwise noted.

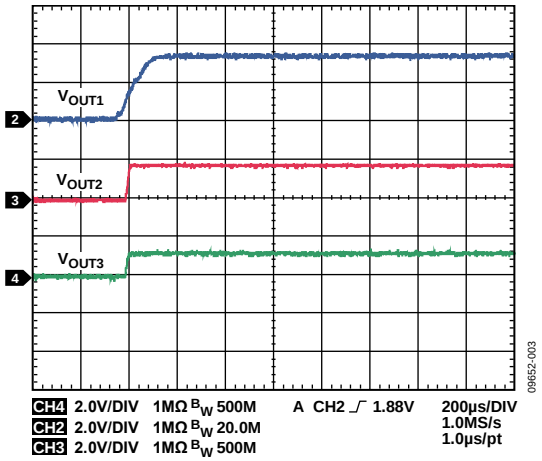


Figure 3. 3-Channel Start-Up Waveforms

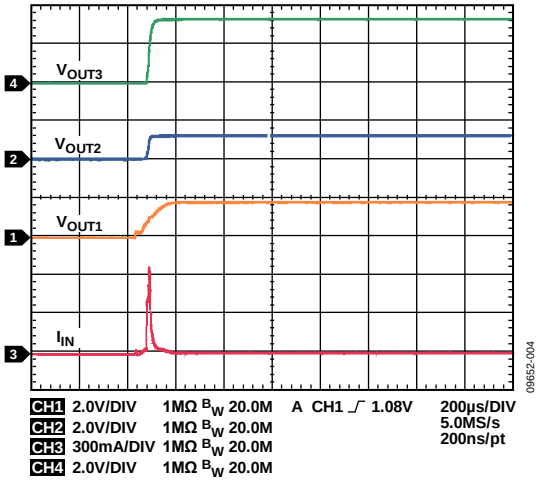


Figure 4. Total Inrush Current, All Channels Started Simultaneously

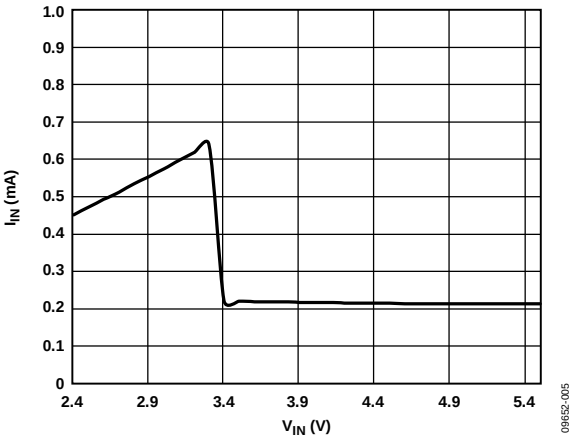


Figure 5. System Quiescent Current (Sum of All the Input Currents) vs. Input Voltage
V_{OUT1} = 1.8 V, V_{OUT2} = V_{OUT3} = 3.3 V, (UVLO = 3.3 V)

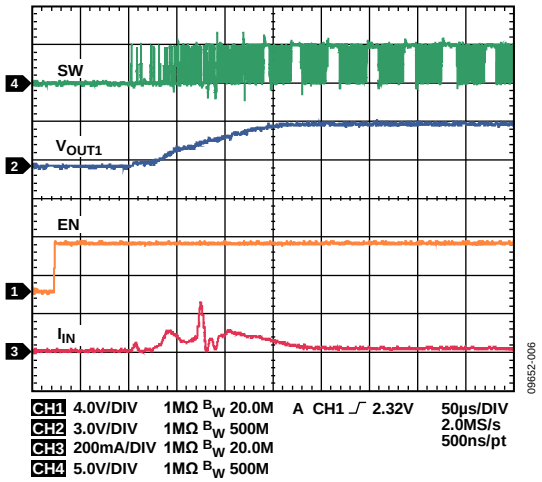


Figure 6. Buck Startup, V_{OUT1} = 3.3 V, I_{OUT2} = 20 mA

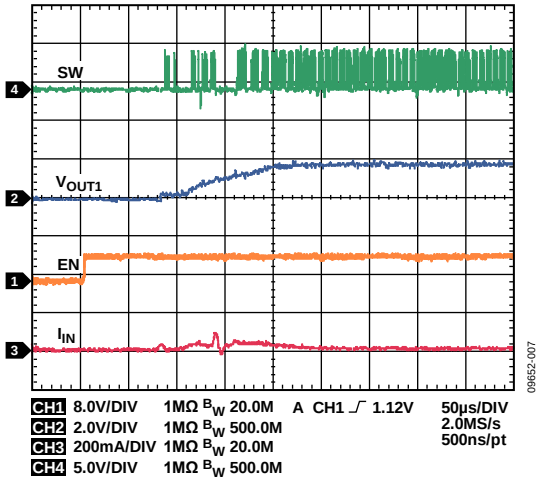


Figure 7. Buck Startup, V_{OUT1} = 1.8 V, I_{OUT} = 20 mA

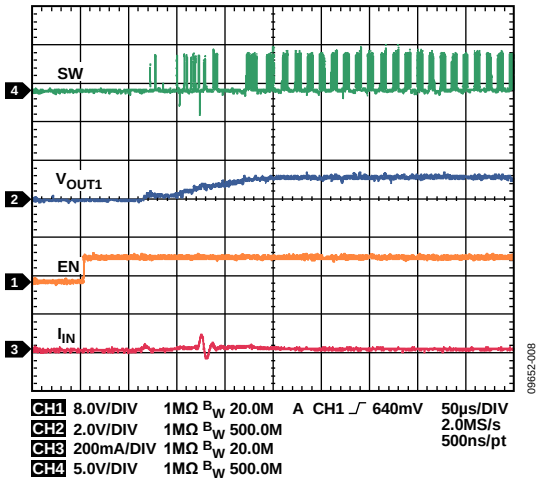


Figure 8. Buck Startup, V_{OUT1} = 1.2 V, I_{OUT} = 20 mA

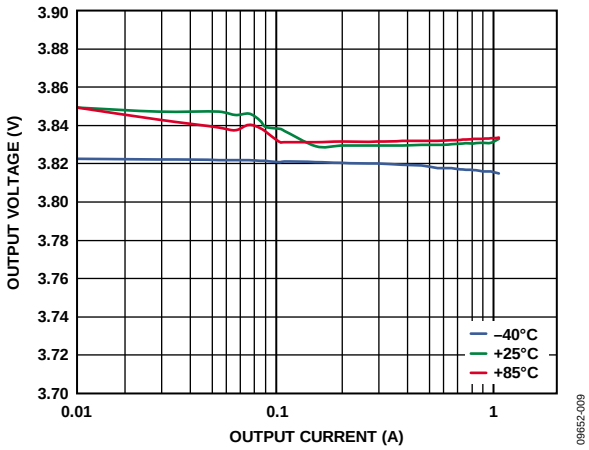


Figure 9. Buck Load Regulation Across Temperature, V_{OUT1} = 3.8 V, Auto Mode

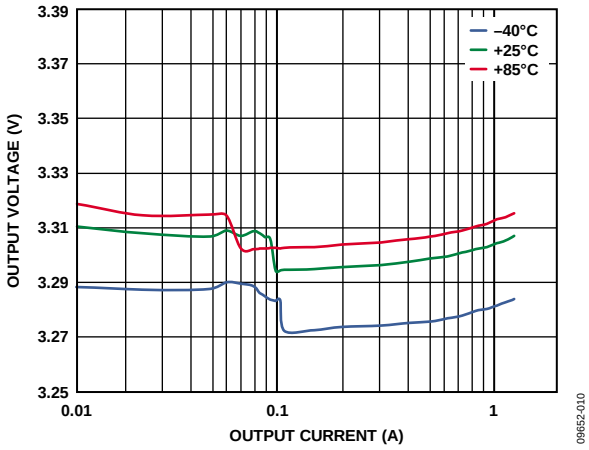


Figure 10. Buck Load Regulation Across Temperature, V_{OUT1} = 3.3 V, Auto Mode

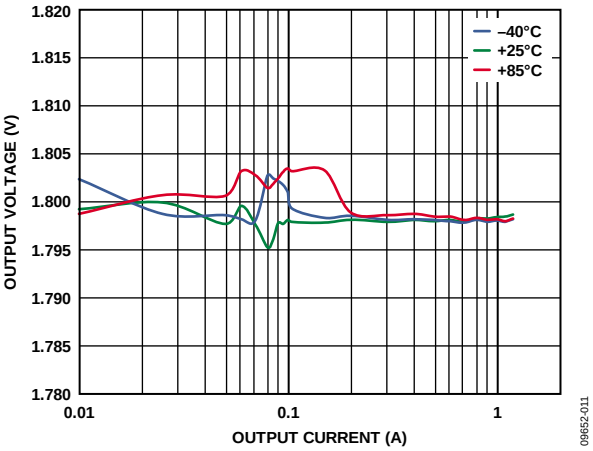


Figure 11. Buck Load Regulation Across Temperature, V_{OUT1} = 1.8 V, Auto Mode

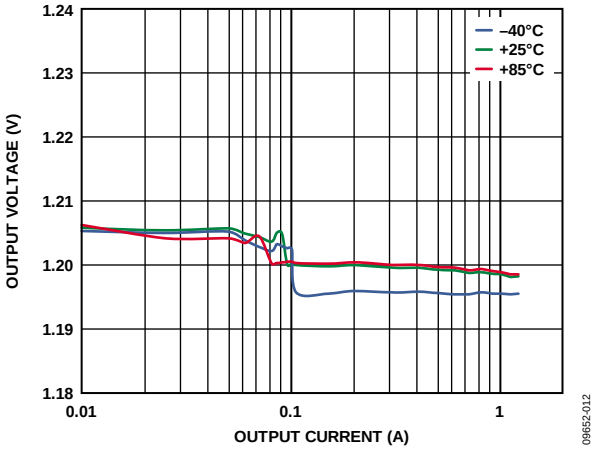


Figure 12. Buck Load Regulation Across Temperature, V_{OUT1} = 1.2 V, Auto Mode

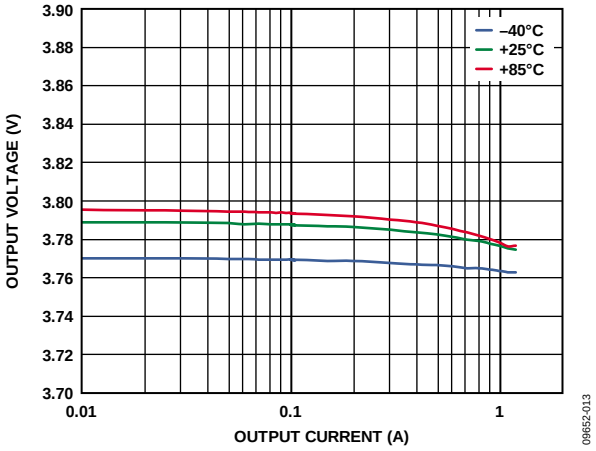


Figure 13. Buck Load Regulation Across Temperature, V_{OUT1} = 3.8 V, PWM Mode

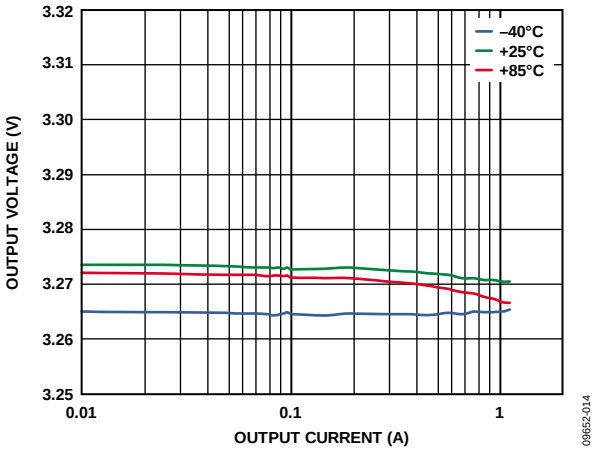


Figure 14. Buck Load Regulation Across Temperature, V_{OUT1} = 3.3 V, PWM Mode

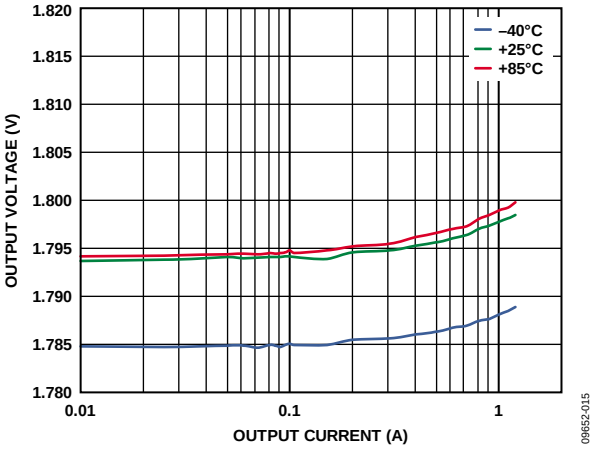


Figure 15. Buck Load Regulation Across Temperature, V_{OUT1} = 1.8 V, PWM Mode

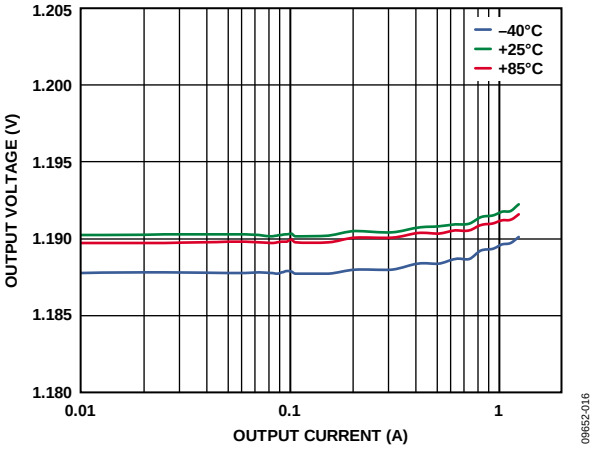


Figure 16. Buck Load Regulation Across Temperature, V_{OUT1} = 1.2 V, PWM Mode

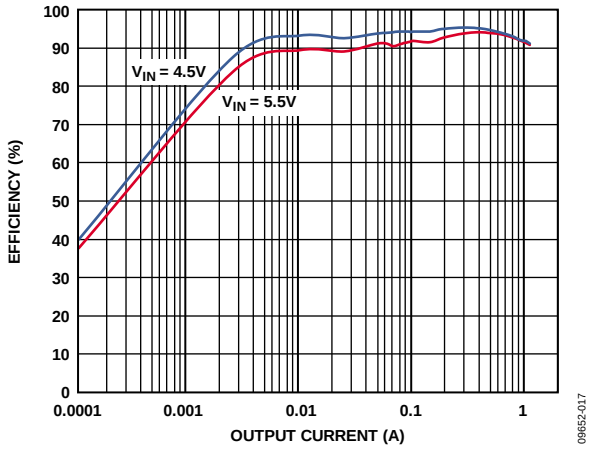


Figure 17. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.8 V, Auto Mode

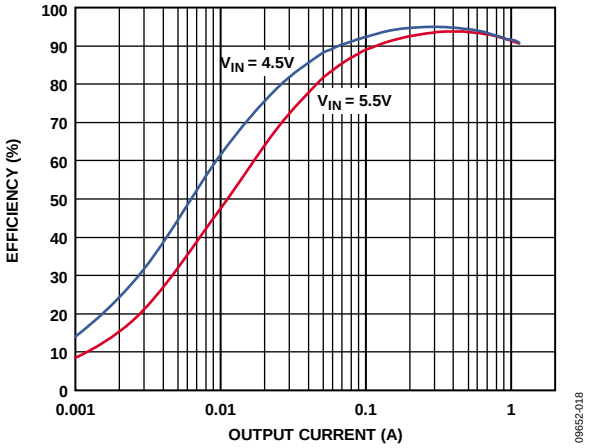


Figure 18. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.8 V, PWM Mode

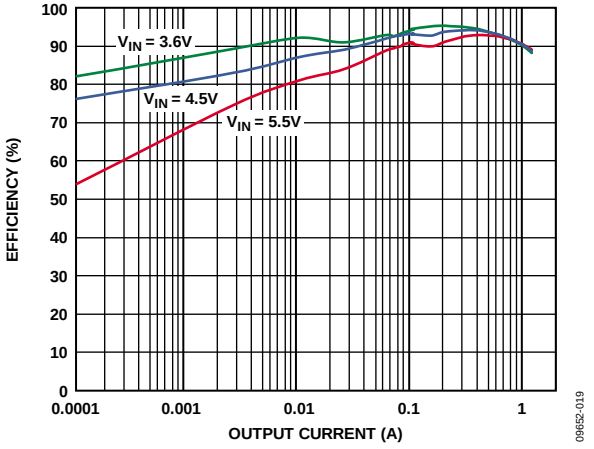


Figure 19. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, Auto Mode

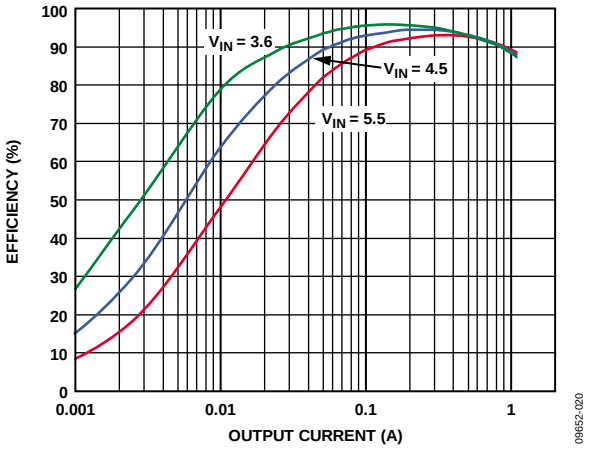


Figure 20. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, PWM Mode

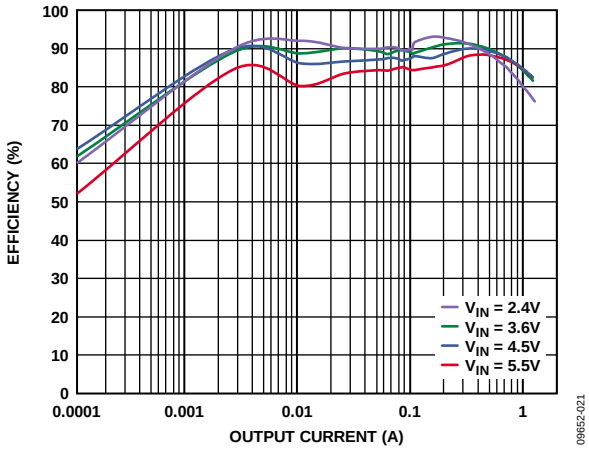


Figure 21. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.8 V, Auto Mode

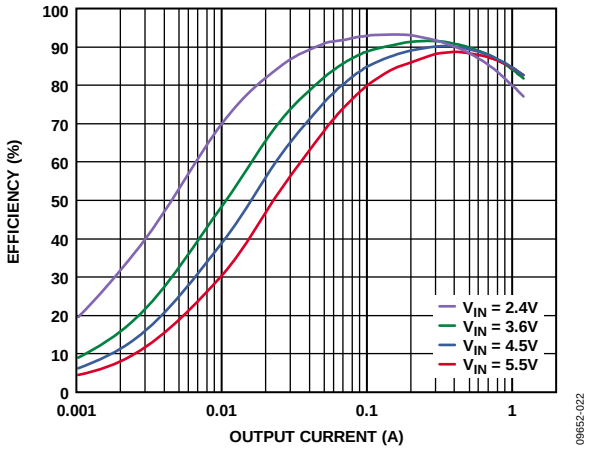


Figure 22. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.8 V, PWM Mode

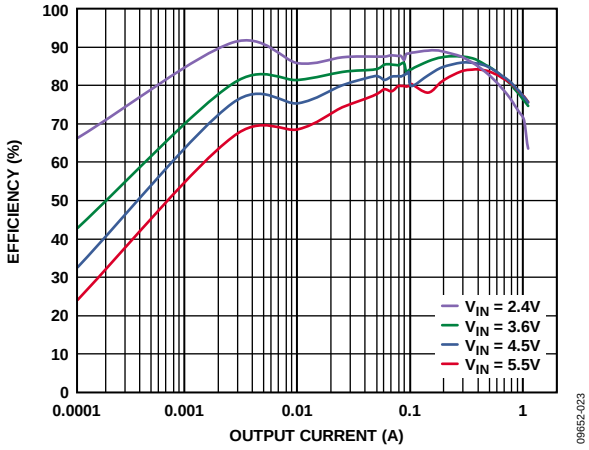


Figure 23. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.2 V, Auto Mode

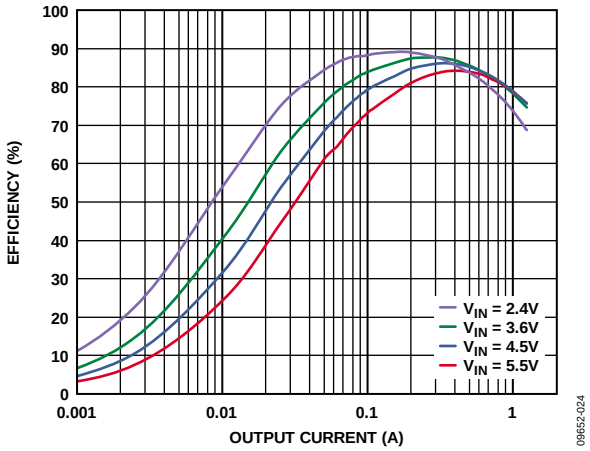


Figure 24. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.2 V, PWM Mode

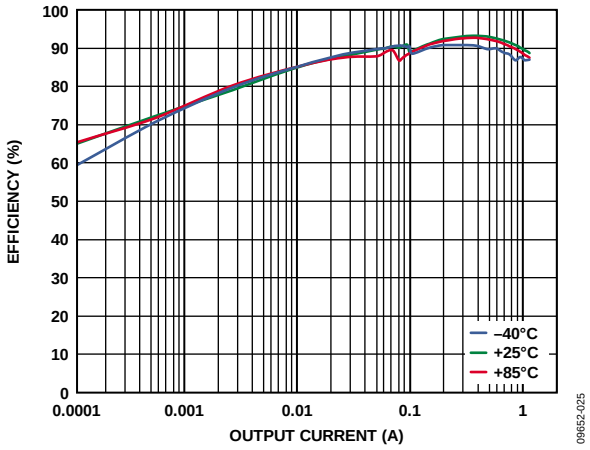


Figure 25. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 3.3 V, Auto Mode

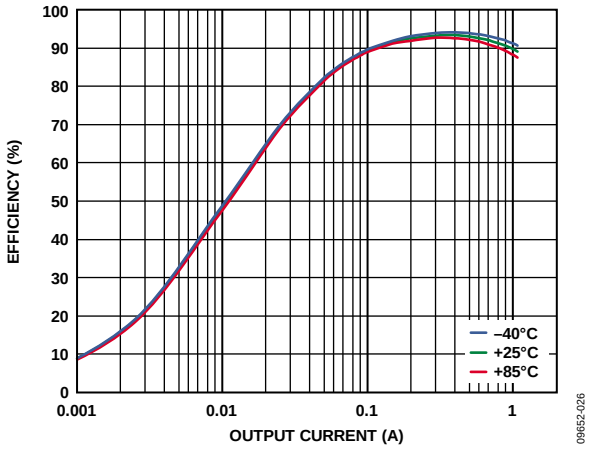


Figure 26. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 3.3 V, PWM Mode

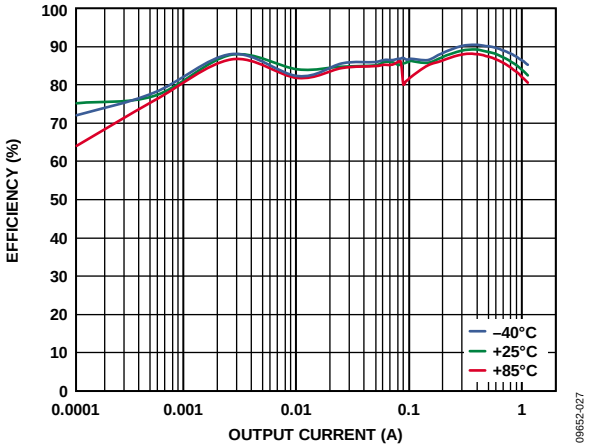


Figure 27. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.8 V, Auto Mode

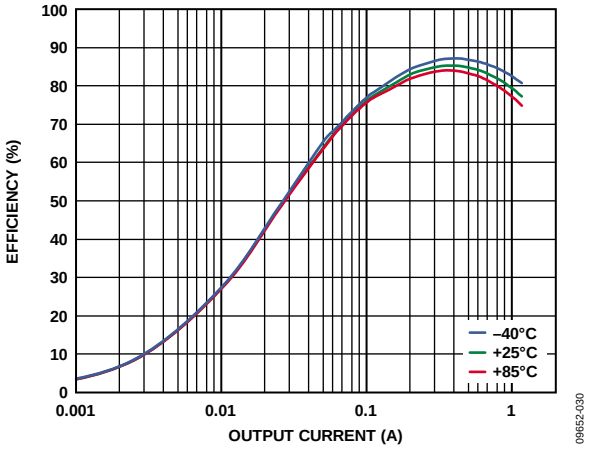


Figure 30. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.2 V, PWM Mode

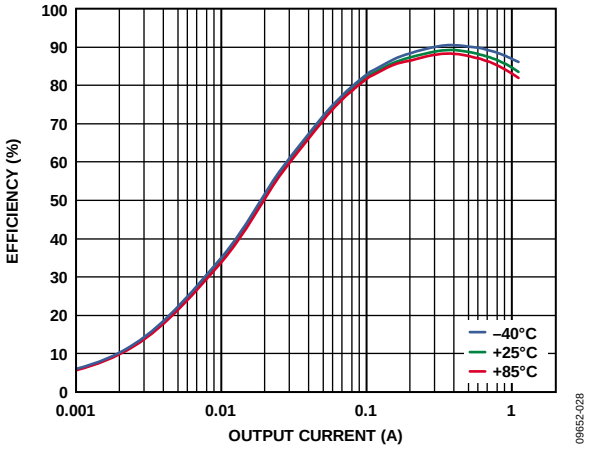


Figure 28. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.8 V, PWM Mode

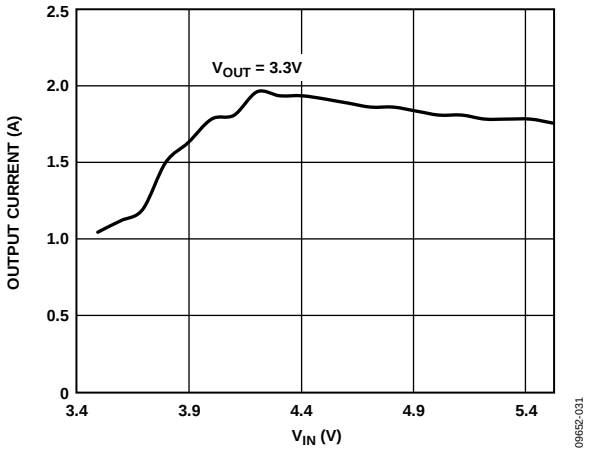


Figure 31. Buck DC Current Capability vs. Input Voltage

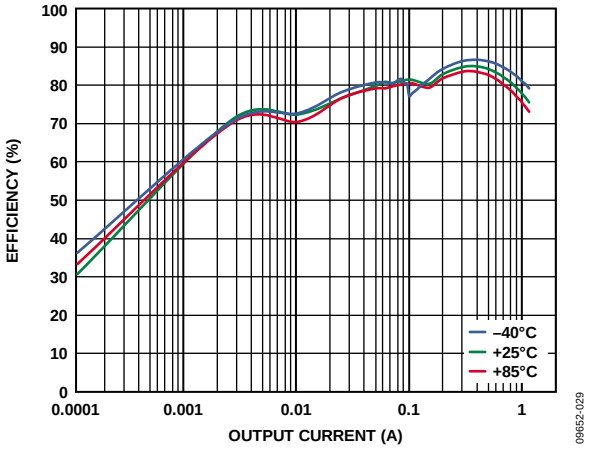


Figure 29. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.2 V, Auto Mode

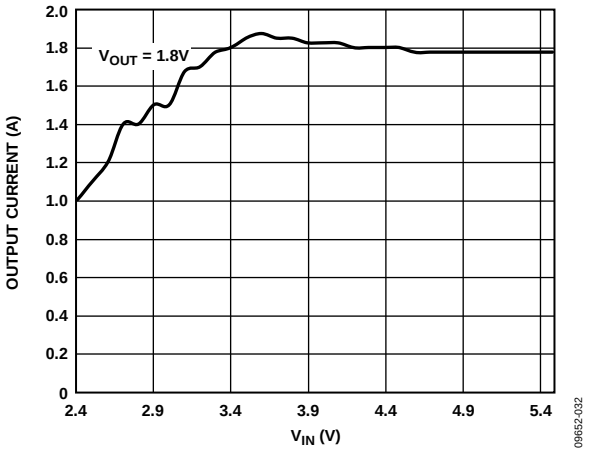


Figure 32. Buck DC Current Capability vs. Input Voltage

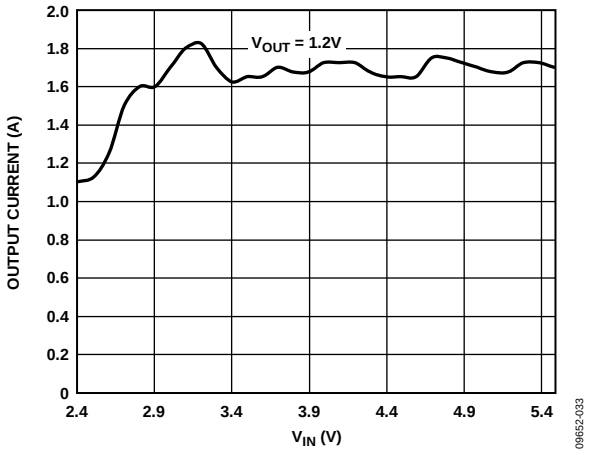


Figure 33. Buck DC Current Capability vs. Input Voltage

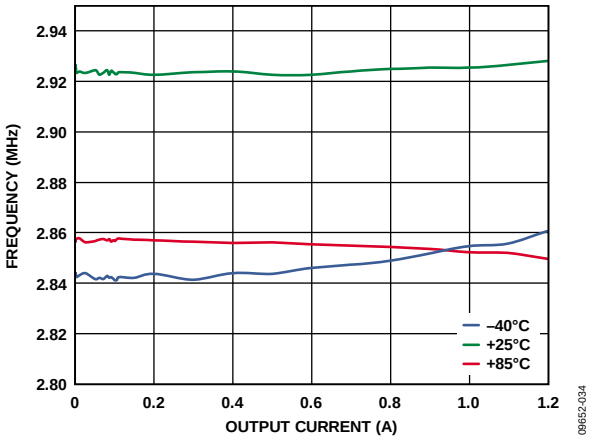


Figure 34. Buck Switching Frequency vs. Output Current, Across Temperature, V_{OUT1} = 1.8 V, PWM Mode

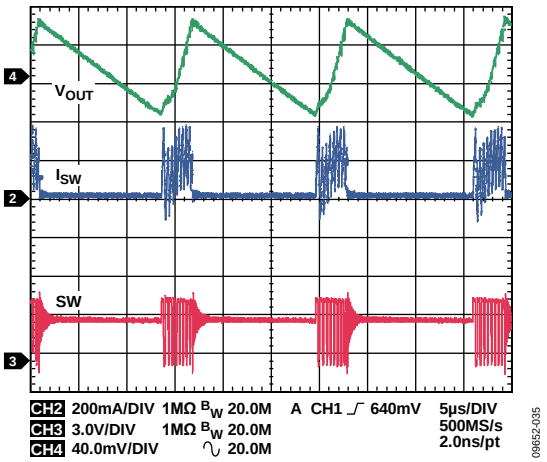


Figure 35. Typical Waveforms, V_{OUT1} = 3.3 V, I_{OUT1} = 30 mA, Auto Mode

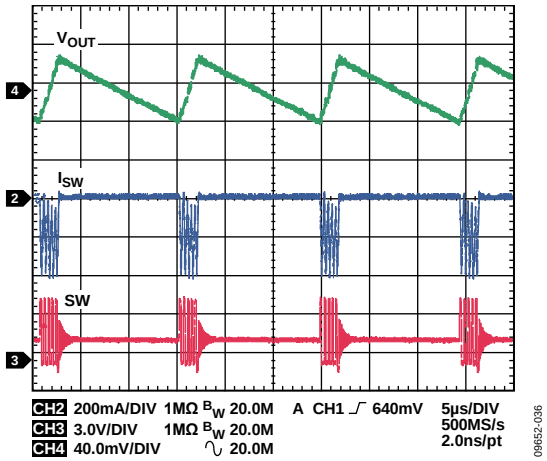


Figure 36. Typical Waveforms, V_{OUT1} = 1.8 V, I_{OUT1} = 30 mA, Auto Mode

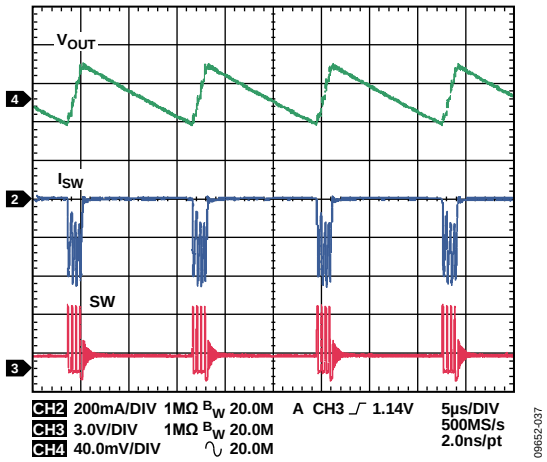


Figure 37. Typical Waveforms, V_{OUT1} = 1.2 V, I_{OUT1} = 30 mA, Auto Mode

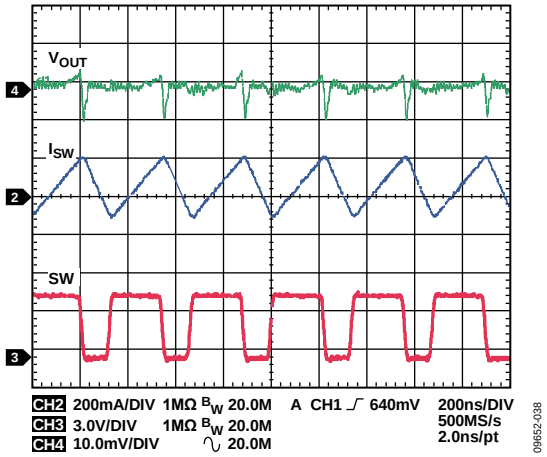


Figure 38. Typical Waveforms, V_{OUT1} = 3.3 V, I_{OUT1} = 30 mA, PWM Mode

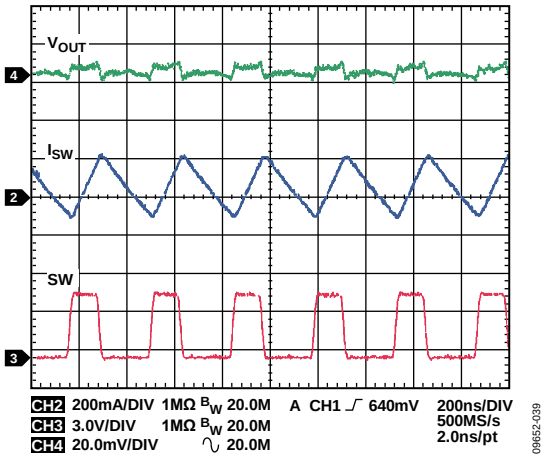


Figure 39. Typical Waveforms, V_{OUT1} = 1.8 V, I_{OUT1} = 30 mA, PWM Mode

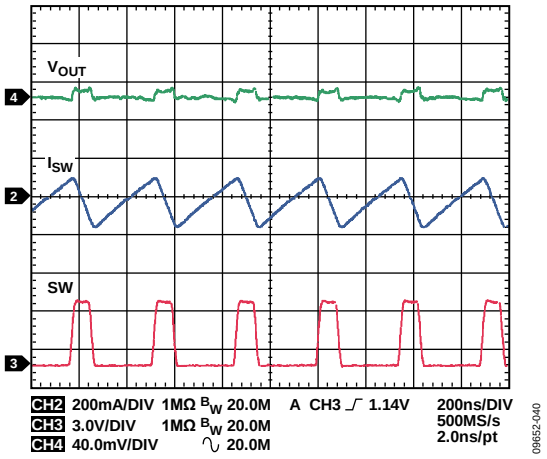


Figure 40. Typical Waveforms, V_{OUT1} = 1.2 V, I_{OUT1} = 30 mA, PWM Mode

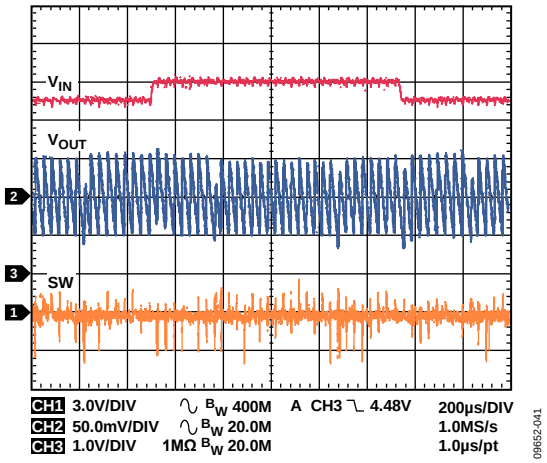


Figure 41. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 3.3 V, I_{OUT1} = 5 mA, Auto Mode

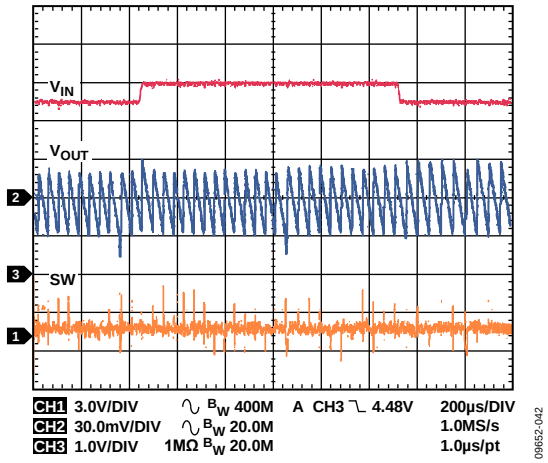


Figure 42. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.8 V, I_{OUT1} = 5 mA, Auto Mode

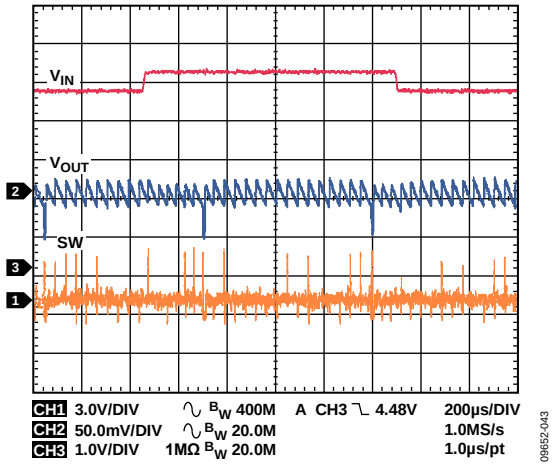


Figure 43. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.2 V, I_{OUT1} = 5 mA, Auto Mode

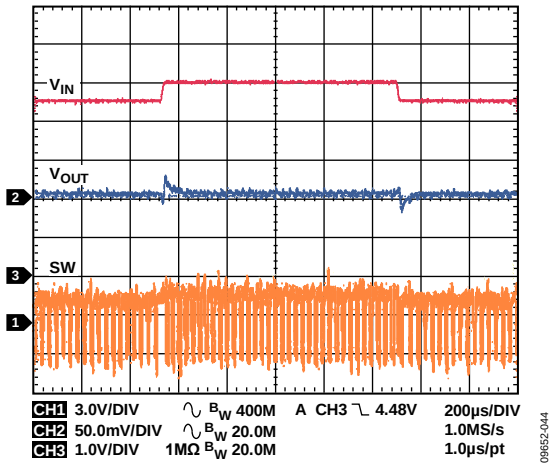


Figure 44. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 3.3 V, PWM Mode

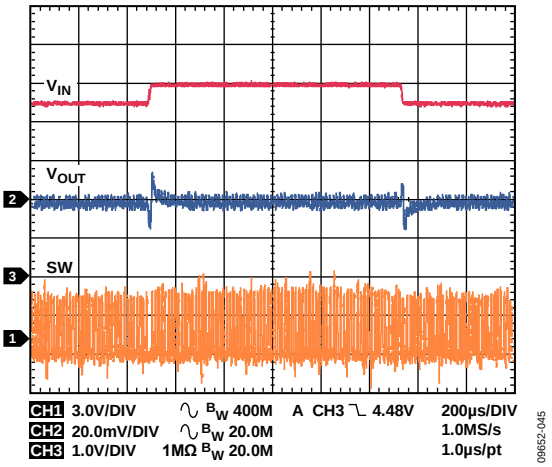


Figure 45. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.8 V, PWM Mode

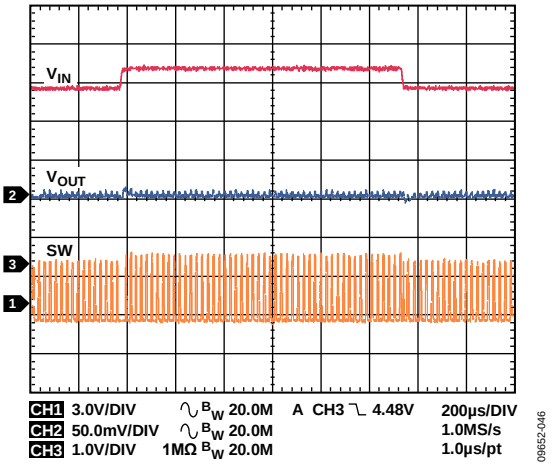


Figure 46. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.2 V, PWM Mode

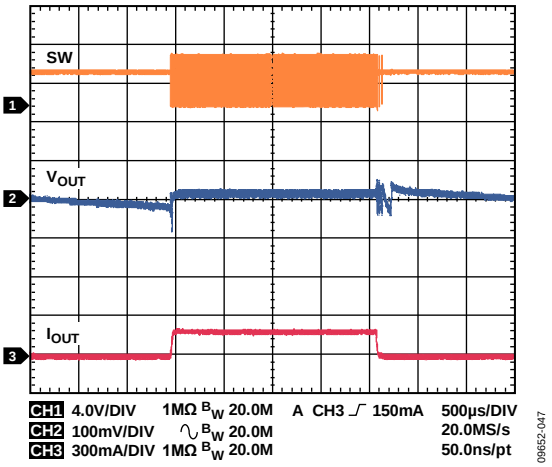


Figure 47. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 3.3 V, Auto Mode

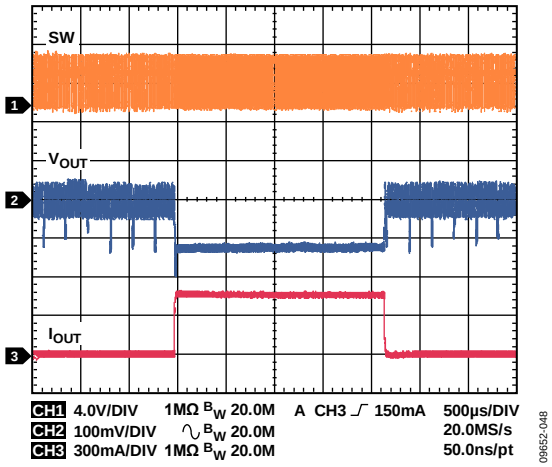


Figure 48. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 3.3 V, Auto Mode

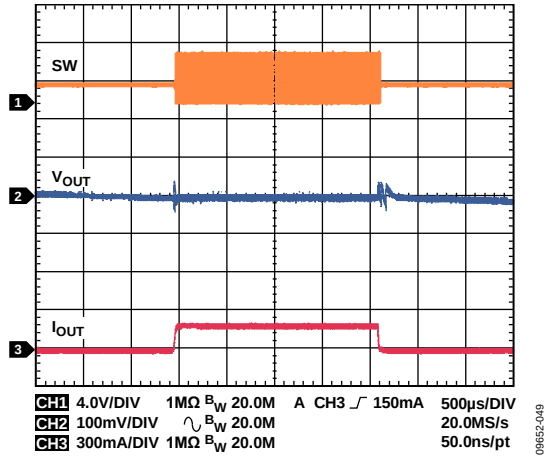


Figure 49. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.8 V, Auto Mode

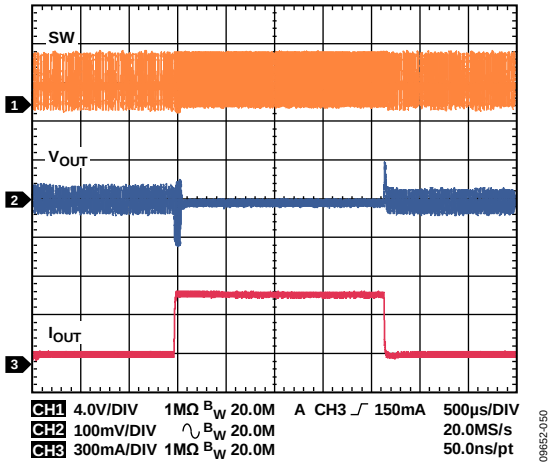


Figure 50. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.8 V, Auto Mode

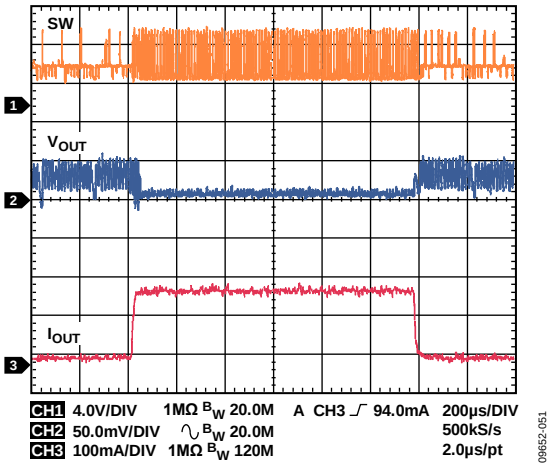


Figure 51. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.2 V, Auto Mode

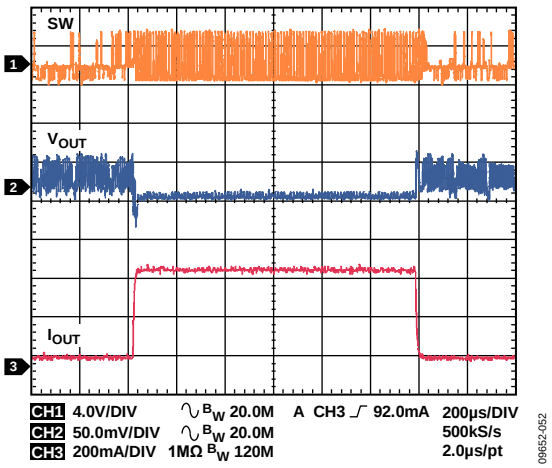


Figure 52. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.2 V, Auto Mode

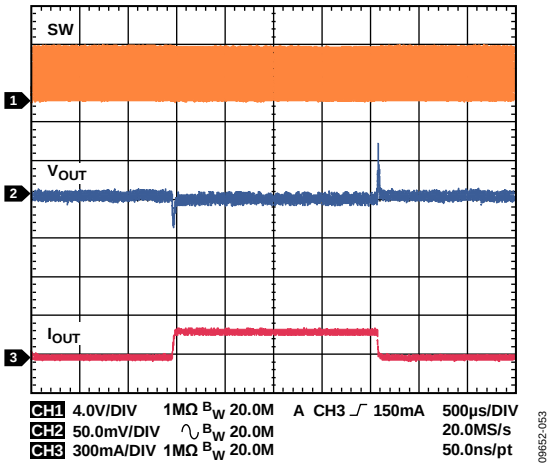


Figure 53. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 3.3 V, PWM Mode

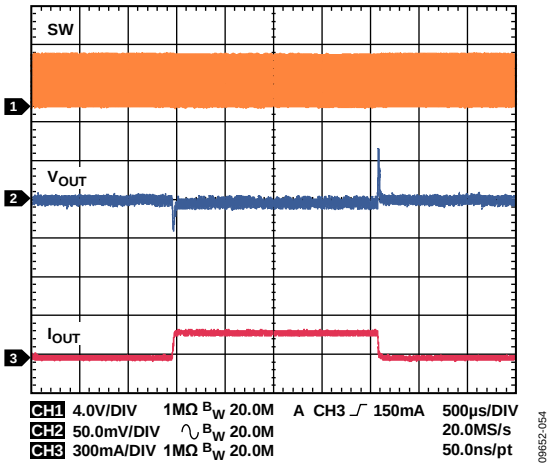


Figure 54. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 3.3 V, PWM Mode

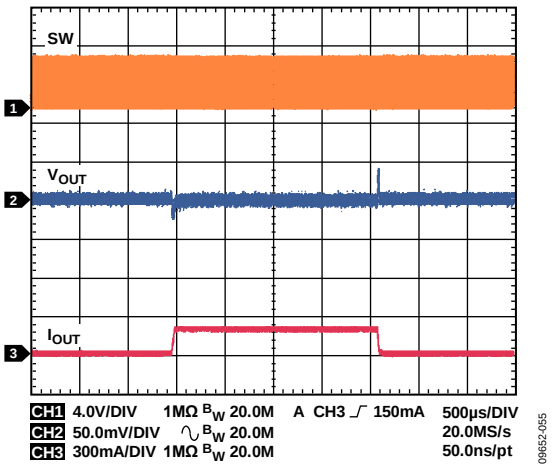


Figure 55. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.8 V, PWM Mode

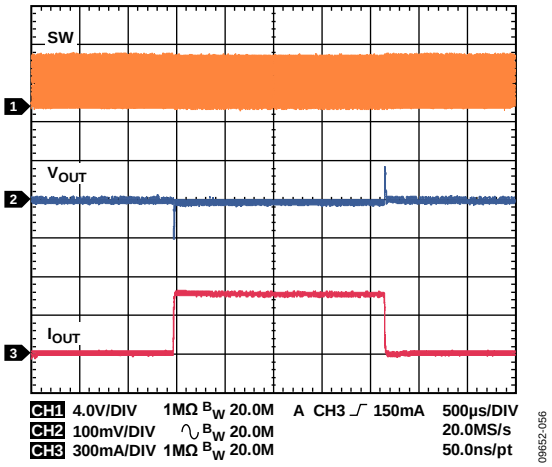


Figure 56. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.8 V, PWM Mode

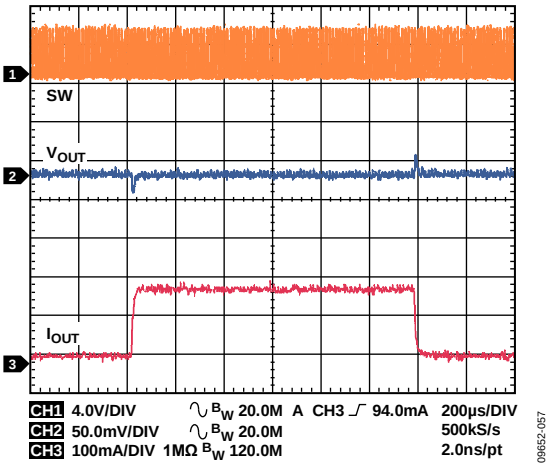


Figure 57. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.2 V, PWM Mode

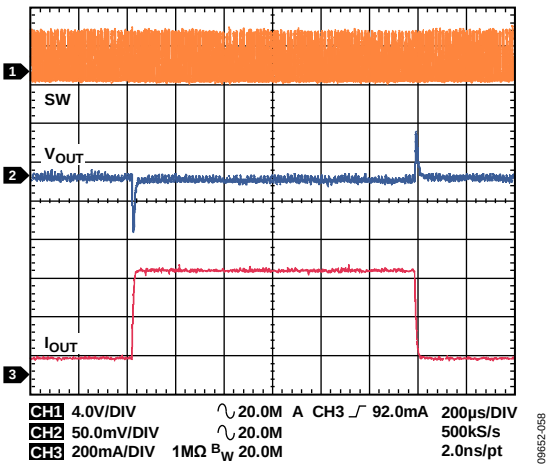


Figure 58. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.2 V, PWM Mode

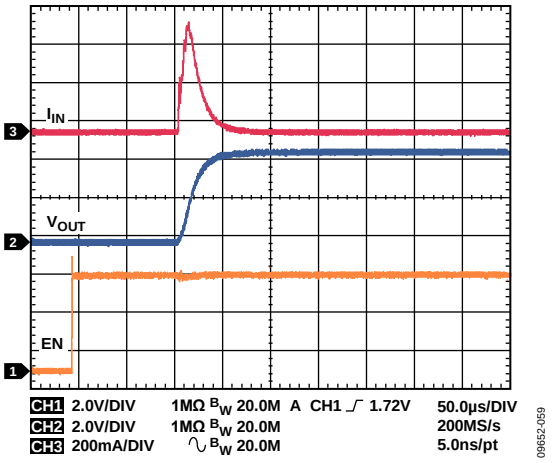


Figure 59. LDO1, LDO2 Startup, V_{OUT} = 4.7 V, I_{OUT} = 5 mA

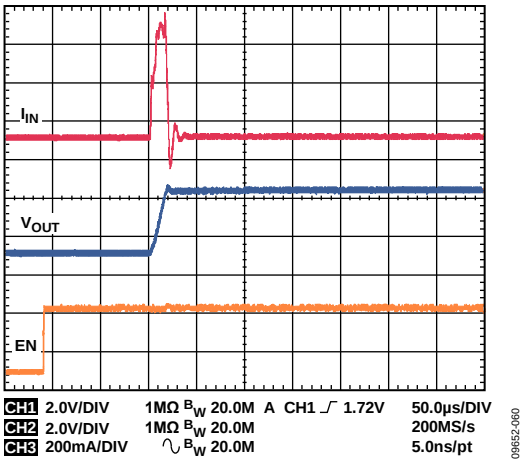


Figure 60. LDO1, LDO2 Startup, V_{OUT} = 3.3 V, I_{OUT} = 5 mA

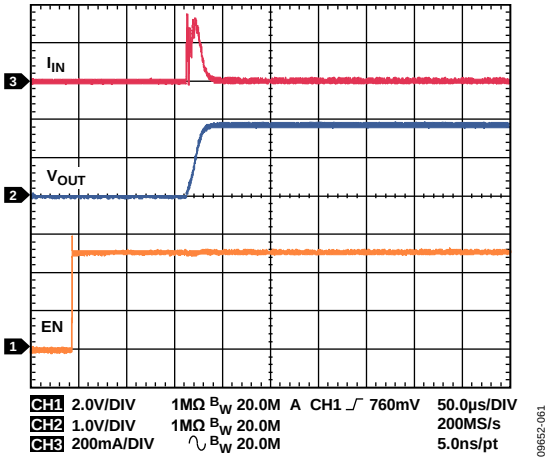


Figure 61. LDO1, LDO2 Startup, V_{OUT} = 1.8 V, I_{OUT} = 5 mA

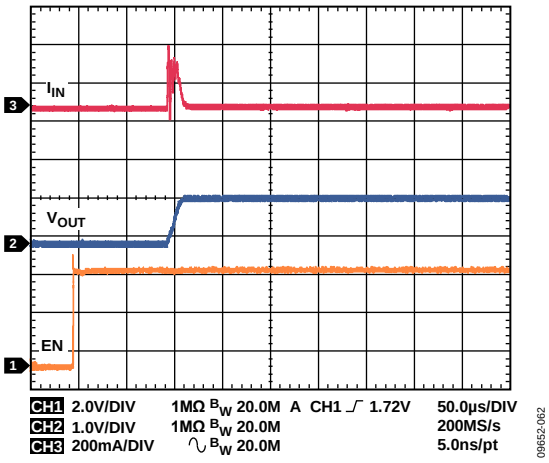


Figure 62. LDO1, LDO2 Startup, V_{OUT} = 1.2 V, I_{OUT} = 5 mA

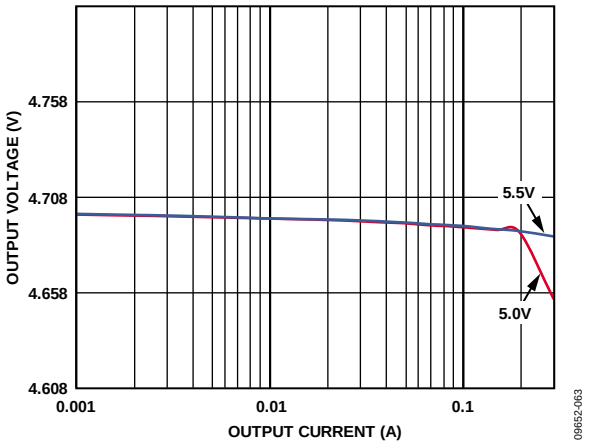


Figure 63. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 4.7 V

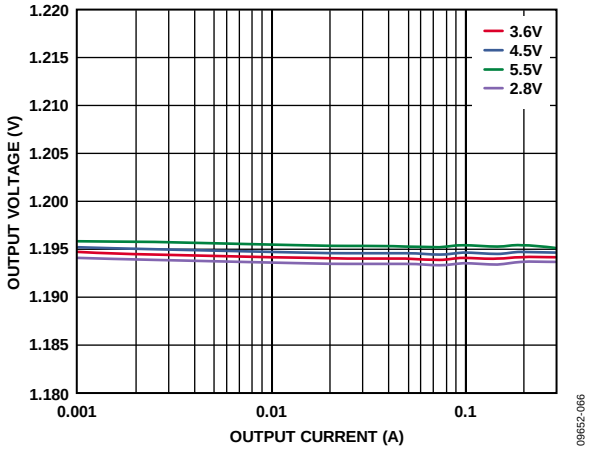


Figure 66. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 1.2 V

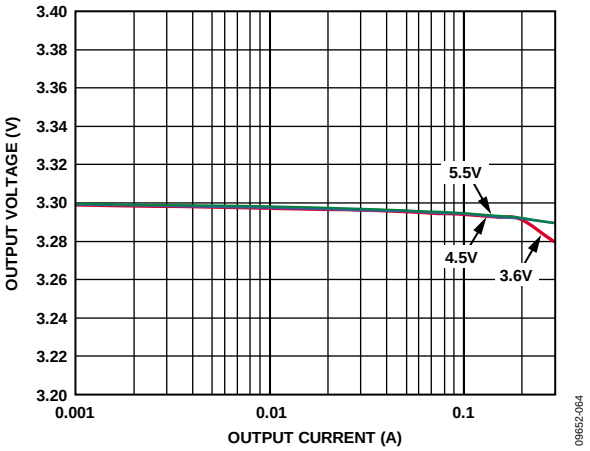


Figure 64. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 3.3 V

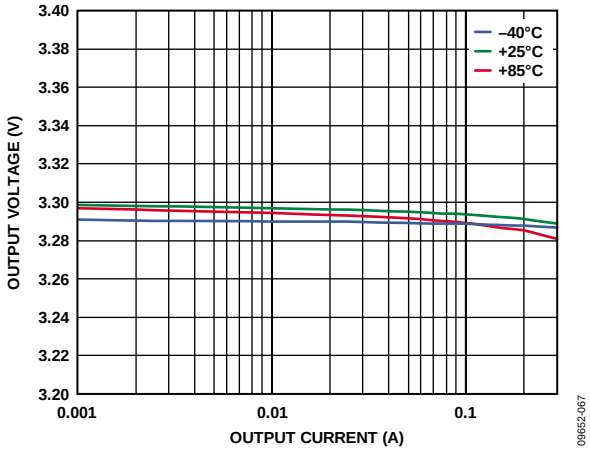


Figure 67. LDO1, LDO2 Load Regulation Across Temperature, V_{IN} = 3.6 V, V_{OUT} = 3.3 V

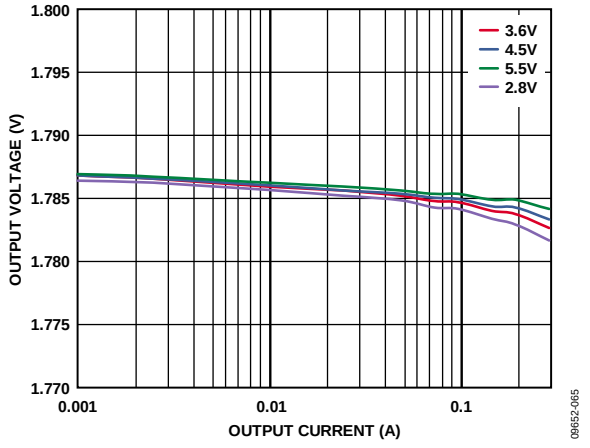


Figure 65. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 1.8 V

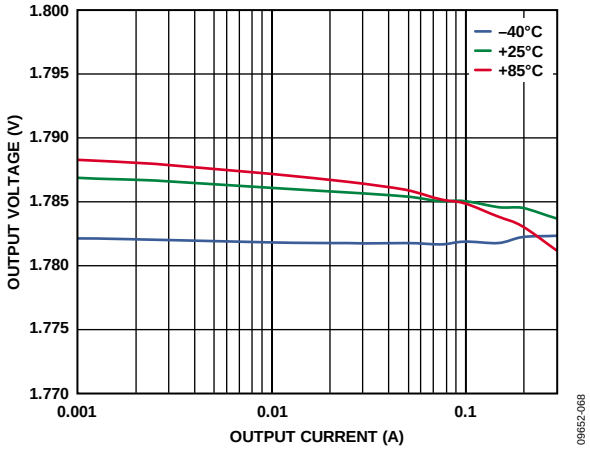


Figure 68. LDO1, LDO2 Load Regulation Across Temperature, V_{IN} = 3.6 V, V_{OUT} = 1.8 V

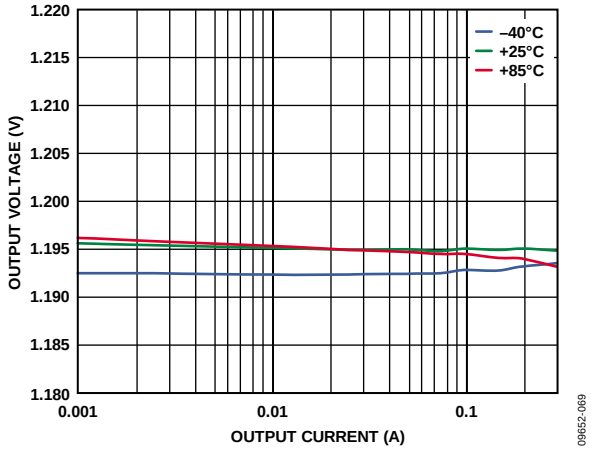


Figure 69. LDO1, LDO2 Load Regulation Across Temperature, V_{IN} = 3.6 V, V_{OUT} = 1.2 V

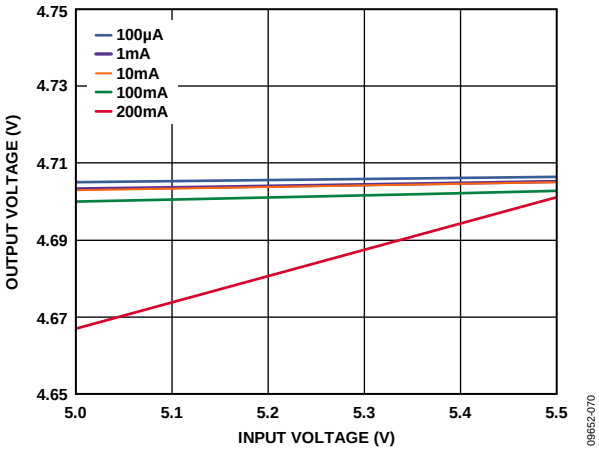


Figure 70. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 4.7 V

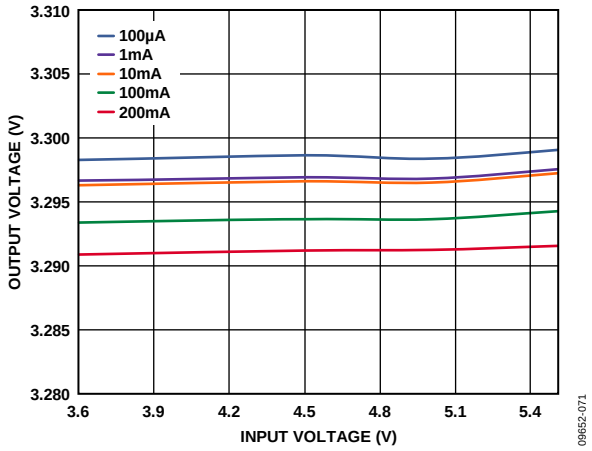


Figure 71. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 3.3 V

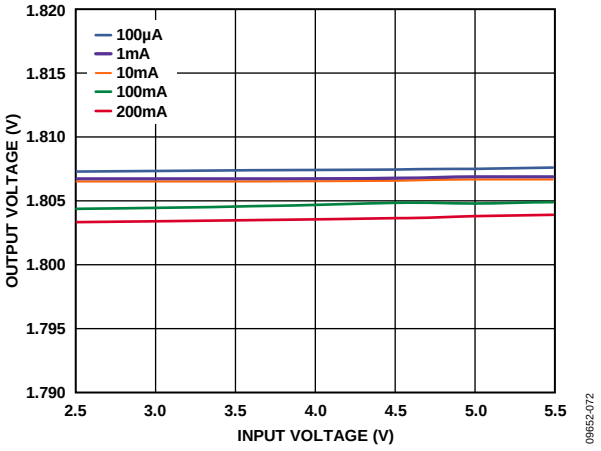


Figure 72. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 1.8 V

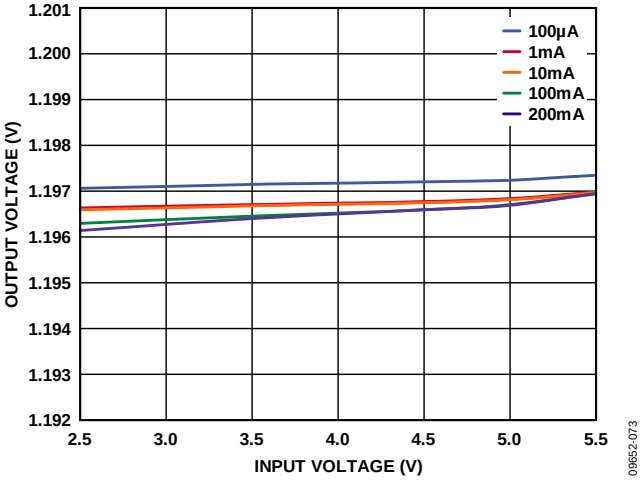


Figure 73. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 1.2 V

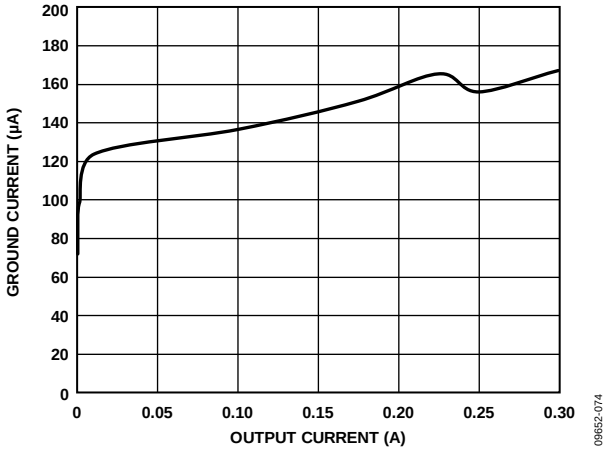


Figure 74. LDO1, LDO2 Ground Current vs. Output Current, V_{OUT} = 3.3 V

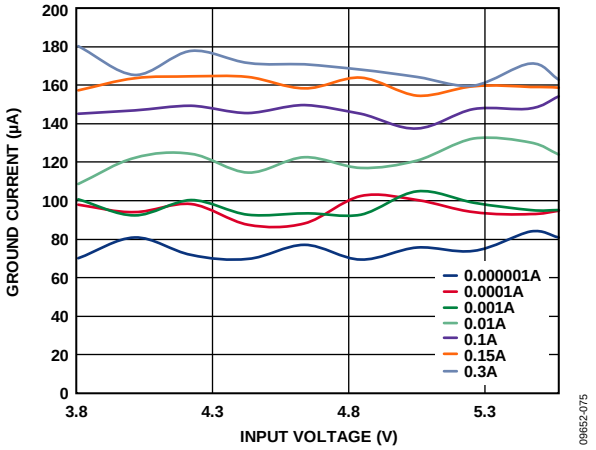


Figure 75. LDO1, LDO2 Ground Current vs. Input Voltage, Across Output Load (A), V_{OUT} = 3.3 V

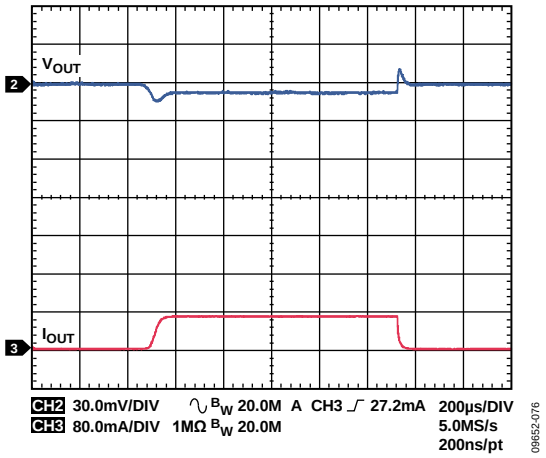


Figure 76. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 4.7 V

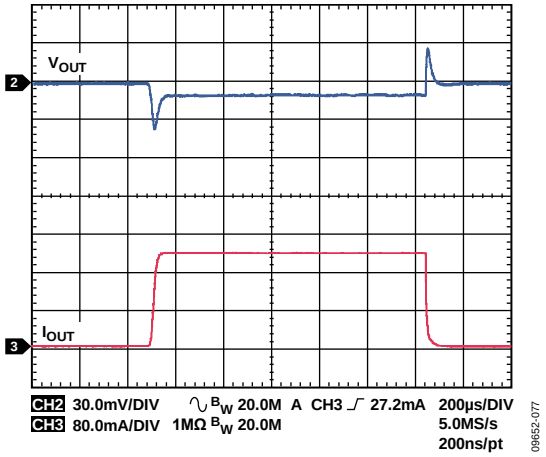


Figure 77. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 4.7 V

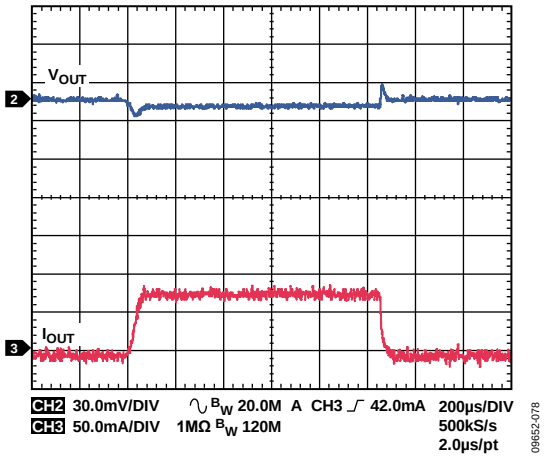


Figure 78. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 3.3 V

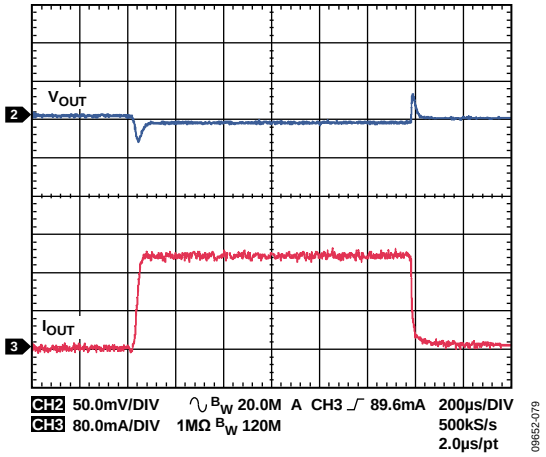


Figure 79. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 3.3 V

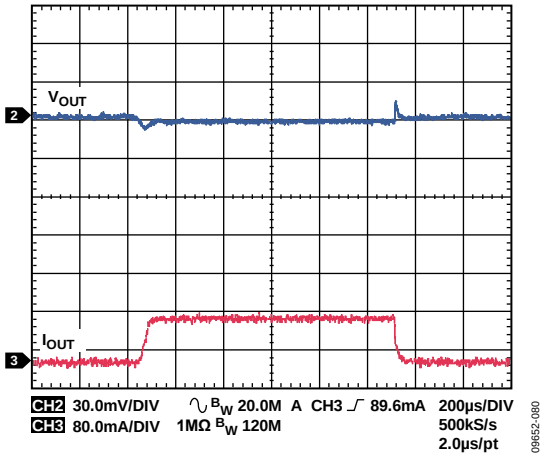


Figure 80. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 1.8 V

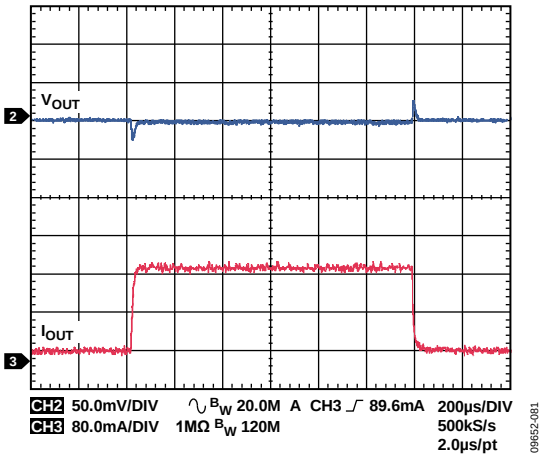


Figure 81. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 1.8 V

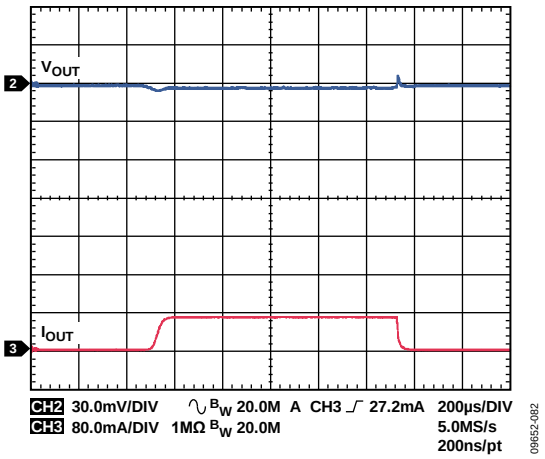


Figure 82. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 1.2 V

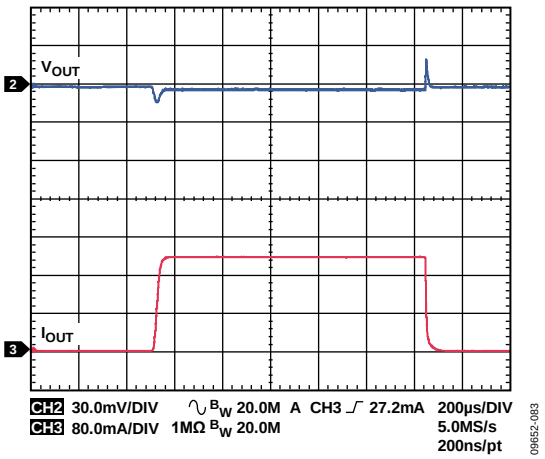


Figure 83. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 1.2 V

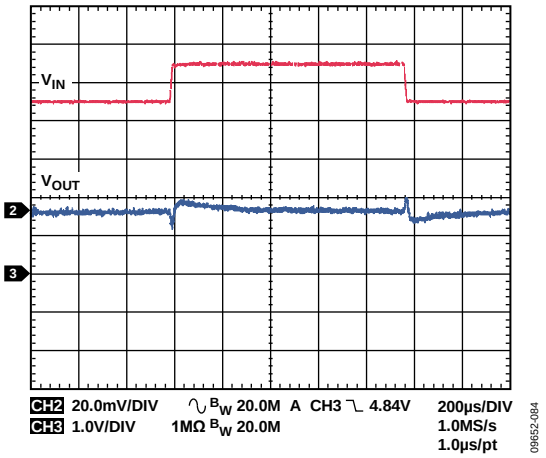


Figure 84. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, V_{OUT} = 3.3 V

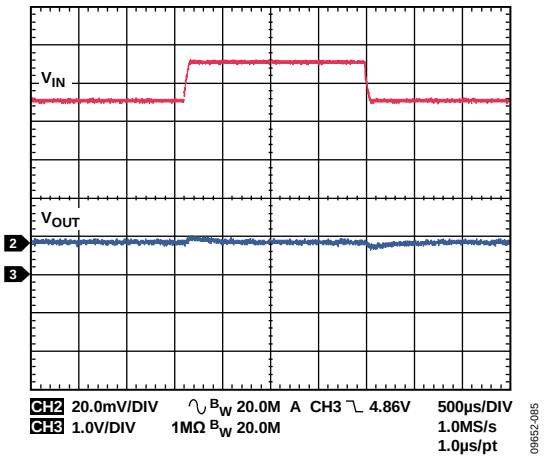


Figure 85. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, V_{OUT} = 1.8 V

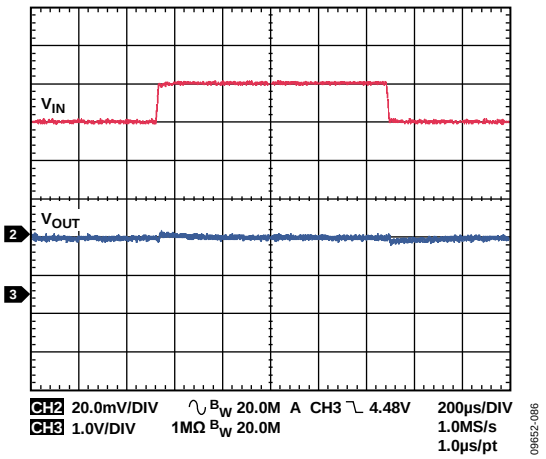


Figure 86. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, V_{OUT} = 1.2 V

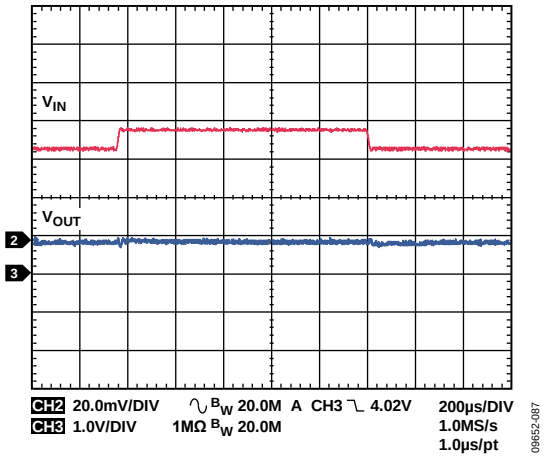


Figure 87. LDO1, LDO2 Response to Line Transient, Input Voltage from 3.3 V to 3.8 V, V_{OUT} = 1.8 V

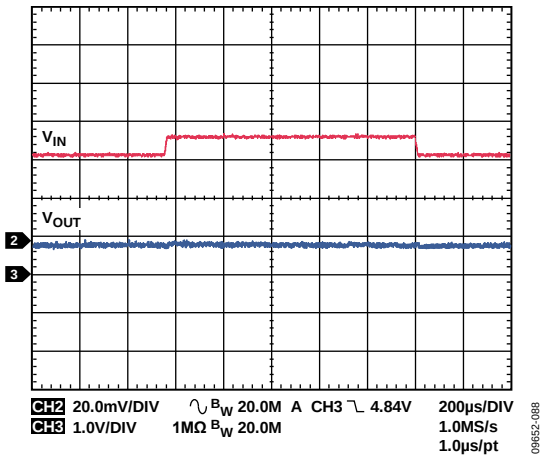


Figure 88. LDO1, LDO2 Response to Line Transient, Input Voltage from 3.3 V to 3.8 V, V_{OUT} = 1.2 V

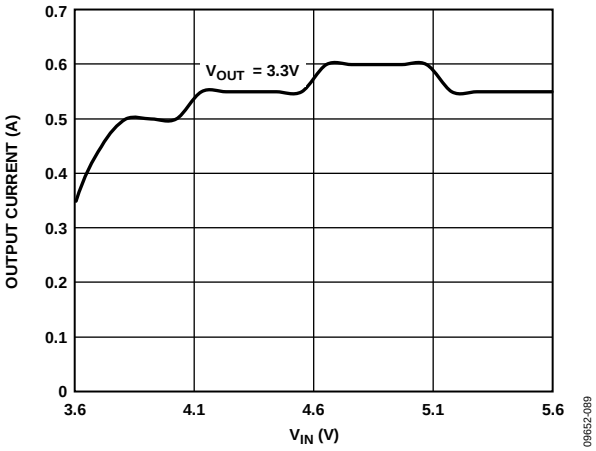


Figure 89. LDO1, LDO2 Output Current Capability vs. Input Voltage

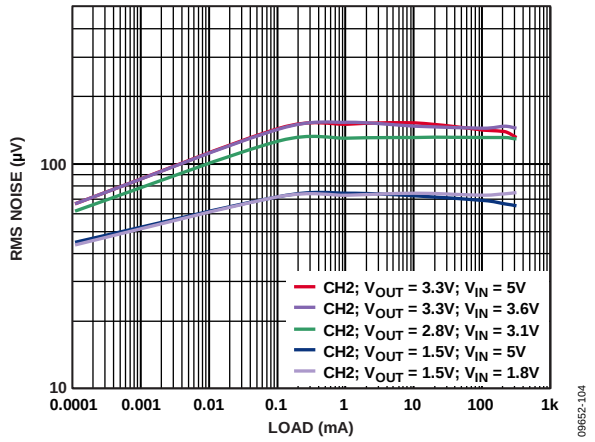


Figure 90. LDO1 Output Noise vs. Load Current, Across Input and Output Voltage

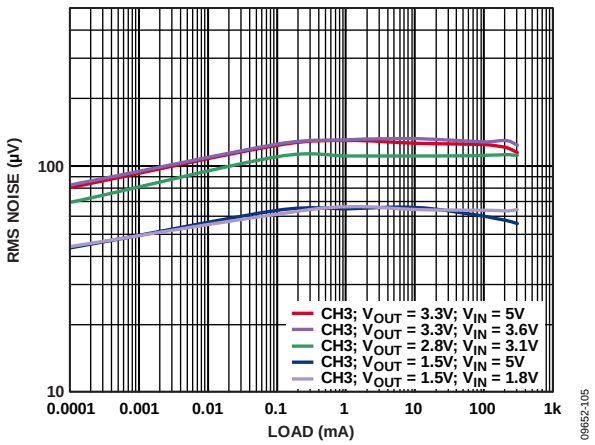


Figure 91. LDO2 Output Noise vs. Load Current, Across Input and Output Voltage

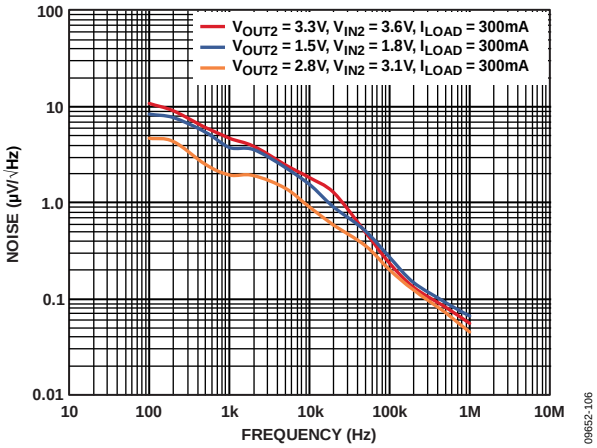


Figure 92. LDO1 Noise Spectrum Across Output Voltage, $V_{IN} = V_{OUT} + 0.3$ V

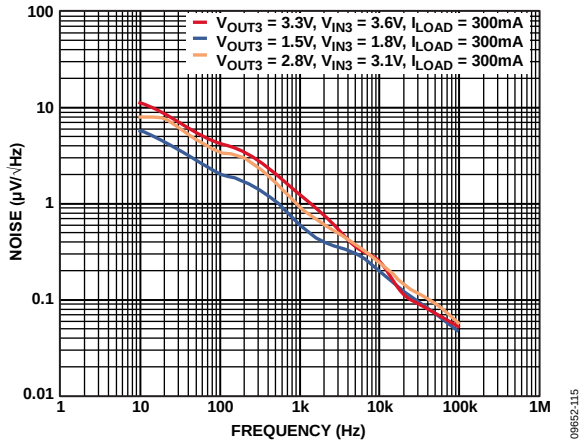


Figure 93. LDO2 Noise Spectrum Across Output Voltage, $V_{IN} = V_{OUT} + 0.3$ V

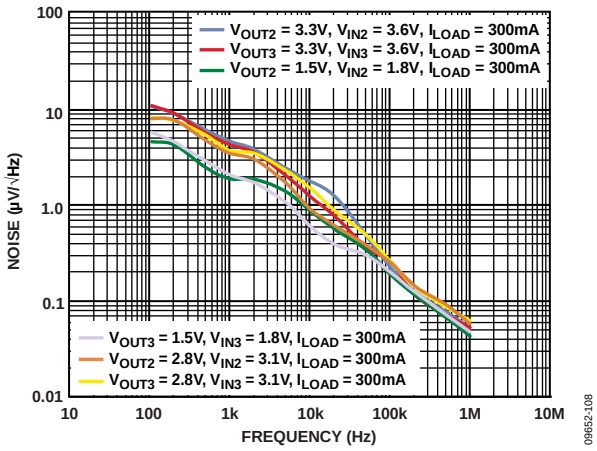


Figure 94. LDO1 vs. LDO2 Noise Spectrum

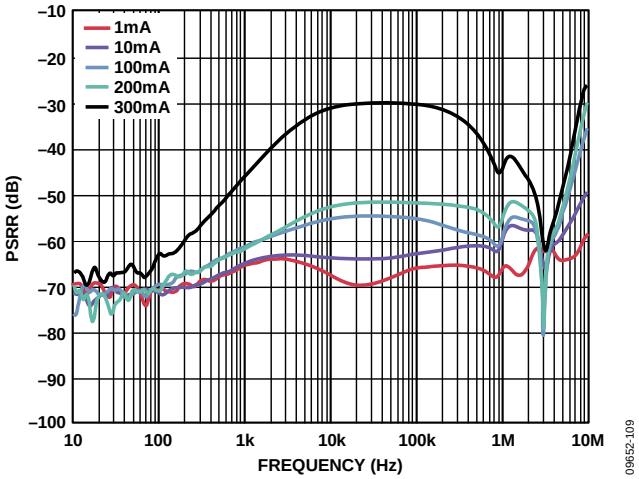


Figure 95. LDO2 PSRR Across Output Load, $V_{IN3} = 3.3$ V, $V_{OUT3} = 2.8$ V

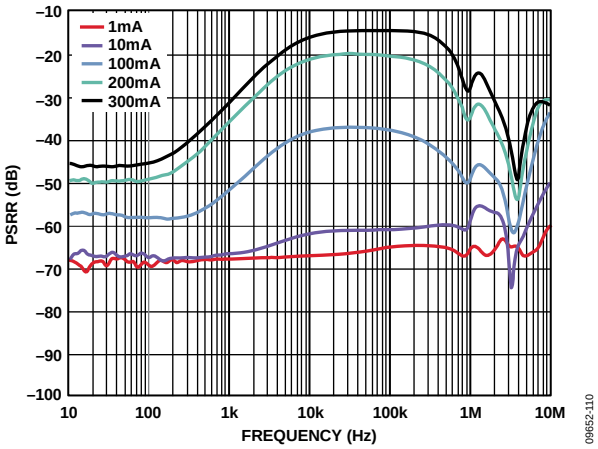


Figure 96. LDO2 PSRR Across Output Load, $V_{IN3} = 3.1$ V, $V_{OUT3} = 2.8$ V

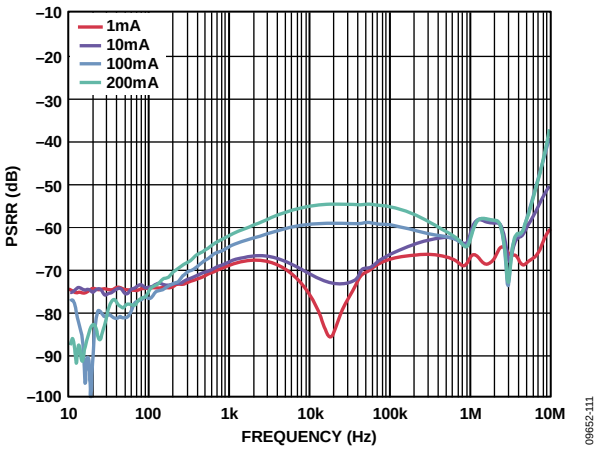


Figure 97. LDO2 PSRR Across Output Load, $V_{IN3} = 5.0$ V, $V_{OUT3} = 3.3$ V

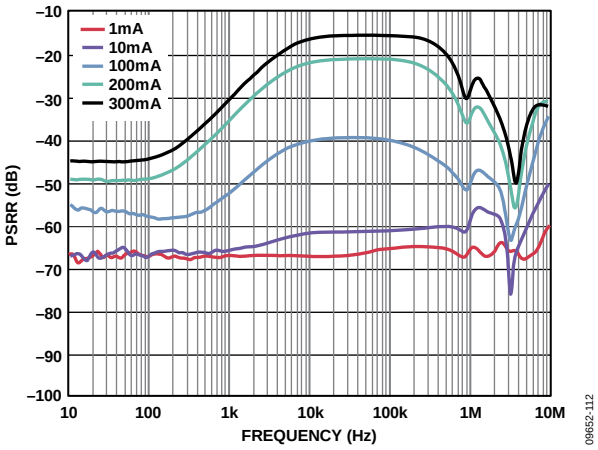


Figure 98. LDO2 PSRR Across Output Load, $V_{IN3} = 3.6$ V, $V_{OUT3} = 3.3$ V

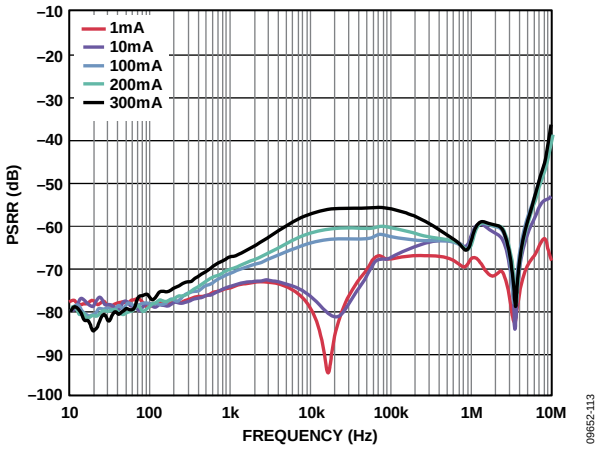


Figure 99. LDO1 PSRR Across Output Load, V_{IN2} = 5.0 V, V_{OUT2} = 1.5 V

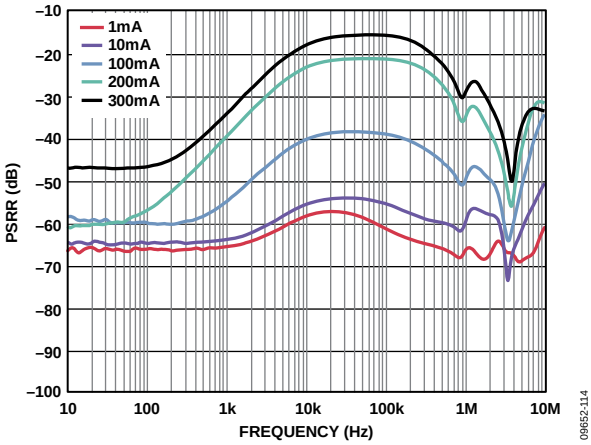


Figure 100. LDO1 PSRR Across Output Load, V_{IN2} = 1.8 V, V_{OUT2} = 1.5 V

THEORY OF OPERATION

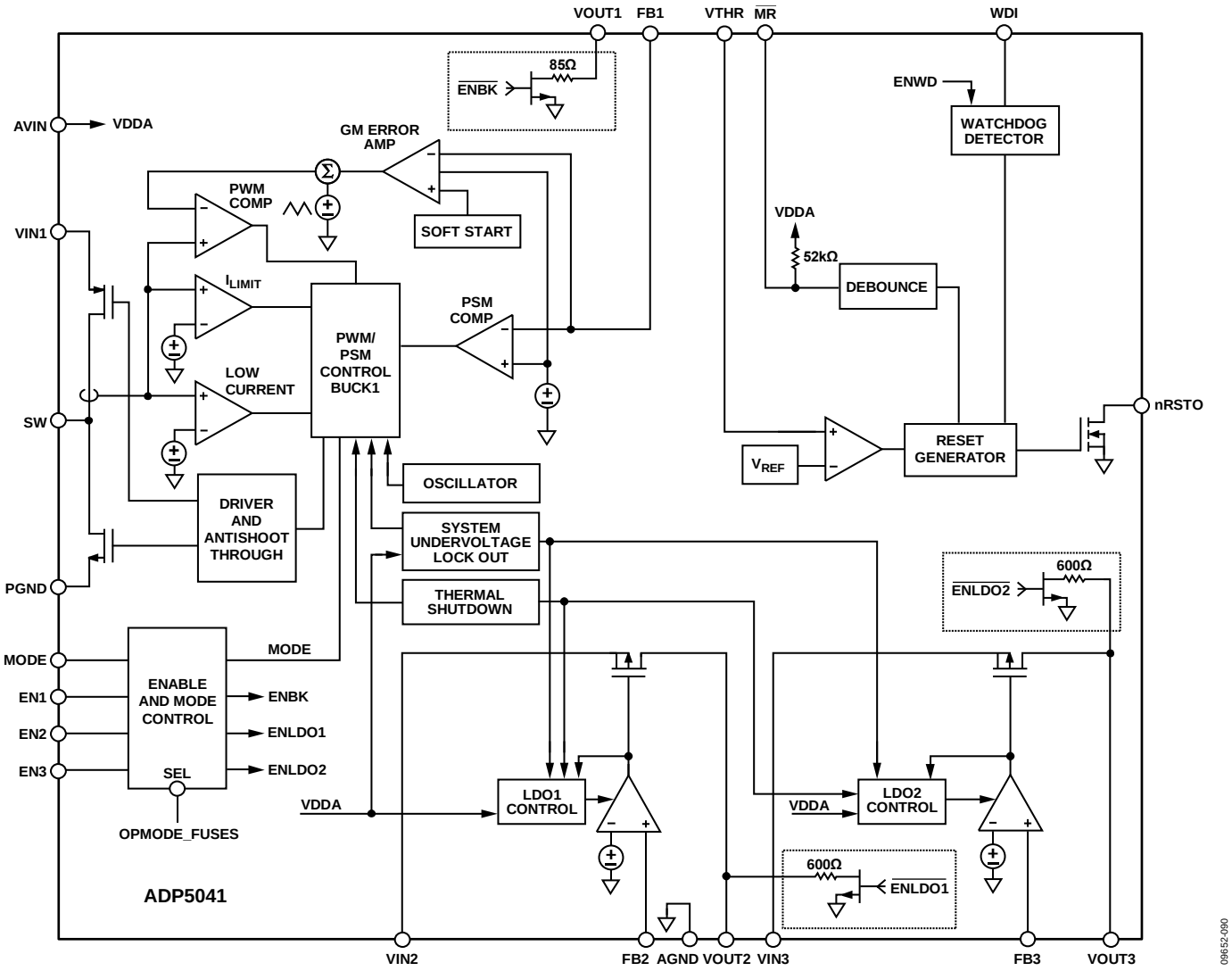


Figure 101. Functional Block Diagram

POWER MANAGEMENT UNIT

The ADP5041 is a micro power management unit (micro PMU) combing one step-down (buck) dc-to-dc regulator, two low dropout linear regulators (LDOs), and a supervisory circuit, with watchdog, for processor control. The high switching frequency and tiny 20-pin LFCSP package allow for a small power management solution.

The regulators are activated by a logic level high applied to the respective EN pin. The EN1 pin controls the buck regulator, the EN2 pin controls LDO1, and the EN3 pin controls LDO2. Other features available on this device are the MODE pin to control the buck switching operation and a push-button reset input.

The regulator output voltages and the reset threshold are set through external resistor dividers.

When a regulator is turned on, the output voltage ramp is controlled through a soft start circuit to avoid a large inrush current due to the discharged output capacitors.

The buck regulator can operate in forced PWM mode if the MODE pin is at a logic high level. In forced PWM mode, the switching frequency of the buck is always constant and does not change with the load current. If the MODE pin is at a logic low level, the switching regulator operates in auto PWM/PSM mode. In this mode, the regulator operates at fixed PWM frequency when the load current is above the power save current threshold. When the load current falls below the power saving current threshold, the regulator enters power saving mode, where the switching occurs in bursts. The burst repetition rate is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses.

Thermal Protection

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off the buck and the LDOs. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included in the thermal shutdown circuit so that when thermal shutdown occurs, the buck and the LDOs do not return to normal operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, all regulators start with soft start control.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated in the ADP5041. If the input voltage on AVIN drops below a typical 2.15 V UVLO threshold, all channels shut down. In the buck channel, both the power switch and the synchronous rectifier turn off. When the voltage on AVIN rises above the UVLO threshold, the part is enabled once more.

Alternatively, the user can select device models with a UVLO set at a higher level, suitable for 5 V applications. For these models, the device reaches the turn-off threshold when the input supply drops to 3.65 V typical.

Enable/Shutdown

The ADP5041 has individual control pins for each regulator. A logic level high applied to the ENx pin activates a regulator, whereas a logic level low turns off a regulator.

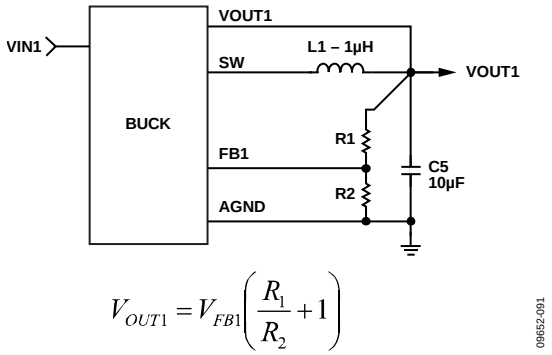
Active Pull-Down

The ADP5041 can be ordered with the active pull-down option enabled. The pull-down resistors are connected between each regulator output and AGND. The pull-downs are enabled, when the regulators are turned off. The typical value of the pull-down resistor is 600 Ω for the LDOs and 85 Ω for the buck.

BUCK SECTION

The buck uses a fixed frequency and high speed current mode architecture. The buck operates with an input voltage of 2.3 V to 5.5 V.

The buck output voltage is set through external resistor dividers, shown in Figure 102. VOUT1 must be connected to the output capacitor. V_{FB1} is internally set to 0.5 V. The output voltage can be set from 0.8 V to 3.8 V.



$$V_{OUT1} = V_{FB1}\left(\frac{R_1}{R_2} + 1\right)$$

Figure 102. Buck External Output Voltage Setting

Control Scheme

The buck operates with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency, but operation shifts to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner, with higher output voltage ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM Mode

In PWM mode, the buck operates at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

The buck smoothly transitions to PSM operation when the load current decreases below the PSM current threshold. When the buck enters power-save mode, an offset is introduced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level that is approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck enters an idle mode. The output capacitor discharges until the output voltage falls to the PWM regulation voltage, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current is below the PSM current threshold.

The ADP5041 has a dedicated MODE pin controlling the PSM and PWM operation. A high logic level applied to the MODE pin forces the buck to operate in PWM mode. A logic level low sets the buck to operate in auto PSM/PWM.

PSM Current Threshold

The PSM current threshold is set to 100 mA. The buck employs a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to, and exit from, the PSM mode. The PSM current threshold is optimized for excellent efficiency over all load currents.

Short-Circuit Protection

The buck includes frequency foldback to prevent current runaway on a hard short at the output. When the voltage at the feedback pin falls below half the internal reference voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Soft Start

The buck has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

The buck has protection circuitry to limit the amount of positive current flowing through the PFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Operation

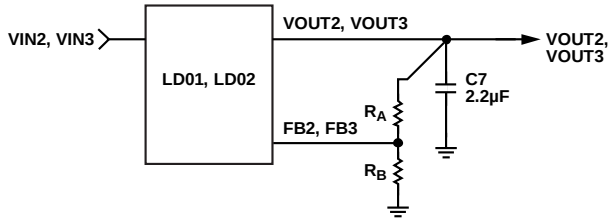
With a drop in input voltage, or with an increase in load current, the buck may reach a limit where, even with the PFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

LDO SECTION

The ADP5041 contains two LDOs with low quiescent current that provide output currents up to 300 mA. The low 10 µA typical quiescent current at no load makes the LDO ideal for battery-operated portable equipment.

The LDOs operate with an input voltage range of 1.7 V to 5.5 V. The wide operating range makes these LDOs suitable for cascade configurations where the LDO supply voltage is provided from the buck regulator.

Each LDO output voltage is set though external resistor dividers, as shown in Figure 103. V_{FB2} and V_{FB3} are internally set to 0.5 V. The output voltage can be set from 0.8 V to 5.2 V.



$$V_{OUT2,\,OUT3} = V_{FB2,\,FB3}\left(\frac{Ra}{Rb}+1\right)$$

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Figure 103. LDOs External Output Voltage Setting

The LDOs also provide high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with small ceramic 1 µF input and 2.2 µF output capacitors.

LDO2 is optimized to supply analog circuits because it offers better noise performance compared to LDO1. LDO1 should be used in applications where noise performance is not critical.

SUPERVISORY SECTION

The ADP5041 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer.

Reset Output

The ADP5041 has an active low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail that is no higher than 6 V. The resistor should comply with the logic low and logic high voltage level requirements of the microprocessor while supplying input current and leakage paths on the nRSTO pin. A 10 kΩ resistor is adequate in most situations.

The reset output is asserted when the monitored rail is below the reset threshold (V_{TH}) or when WDI is not serviced within the watchdog timeout period (t_{WDI}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after the monitored rail rises above the reset threshold or after the watchdog timer times out. Figure 104 illustrates the behavior of the reset output, nRSTO, and it assumes that VOUT2 is selected as the rail to be monitored and supplies the external pull-up connected to the nRSTO output.

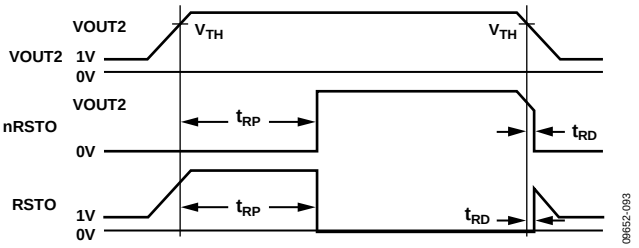

Figure 104. Reset Timing Diagram

The ADP5041 has a reset threshold programming input pin, VTHR, to monitor a supply rail.

The reset threshold voltage at VTHR input is typically 0.5 V. To monitor a voltage greater than 0.5 V, connect a resistor divider network to the device as shown in Figure 105, where

$$V_{MONITORED} = 0.5V\left(\frac{R1 + R2}{R2}\right)$$

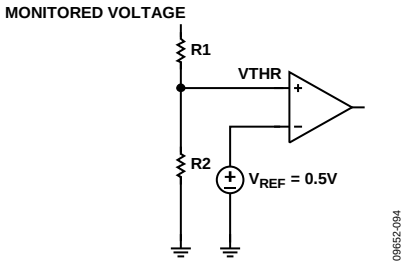

Figure 105. External Reset Threshold Programming

Do not allow the VTHR input to float or to be grounded. Connect it to a supply voltage greater than its specified threshold voltage. A small capacitor can be added on VTHR to improve the noise rejection and to prevent false reset generation.

The ADP5041 can be factory programmed to a 2.25 V or 3.6 V UVLO threshold. When monitoring the input supply voltage, if the selected reset threshold is below the UVLO level, the reset output, nRSTO, is asserted low as soon as the input voltage falls below the UVLO threshold. Below the UVLO threshold, the reset output is maintained low down to ~1 V input voltage. This is to ensure that the reset output is not released when there is sufficient voltage on the rail supplying a processor to restart the processor operations.

Manual Reset Input

The ADP5041 features a manual reset input ($\overline{MR}$) which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, the reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 kΩ, internal pull-up connected to AVIN, so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input, and fast negative-going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

Watchdog Input

The ADP5041 features a watchdog timer that monitors microprocessor activity. The watchdog timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 80 ns. If the timer counts through the preset watchdog timeout period (t_{WDI}), an output reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

As well as logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on the monitored rail. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deasserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

The ADP5041 can be factory programmed to two possible watchdog timer values as indicated in Table 18.

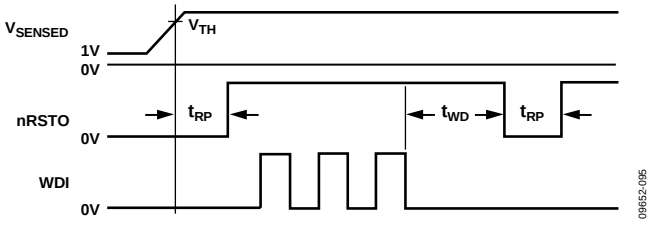

Figure 106. Watchdog Timing Diagram

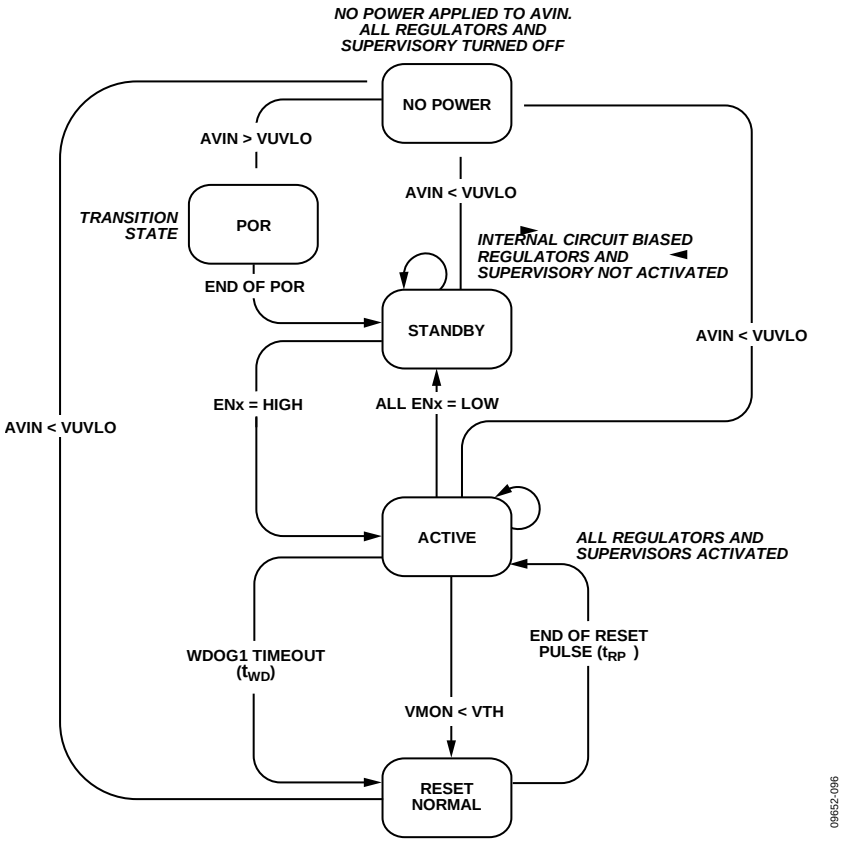

Figure 107. ADP5041 State Flow

APPLICATIONS INFORMATION

BUCK EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response are made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Feedback Resistors

Referring to Figure 102, the total combined resistance for R1 and R2 is not to exceed 400 kΩ.

Inductor

The high switching frequency of the ADP5041 buck allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3.0 µH. Suggested inductors are shown in Table 9.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Table 9. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
Murata	LQM18FN1R0M00B	3.2 × 2.5 × 1.5	2300	54
Tayo Yuden	CBC322ST1R0MR	3.2 × 2.5 × 2.5	2000	71
Coilcraft	XFL4020-102ME	4.0 × 4.0 × 2.1	5400	11
Coilcraft	XPL2010-102ML	1.9 × 2.0 × 1.0	1800	89
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1350	85

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the buck is a high switching frequency dc-to-dc converter, shielded ferrite core material is recommended for its low core losses and low EMI.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing the capacitor value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are highly recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 9.24 µF at 1.8 V, as shown in Figure 108.

Substituting these values in the equation yields

$$C_{EFF} = 9.24\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.07 \mu F$$

To guarantee the performance of the buck, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

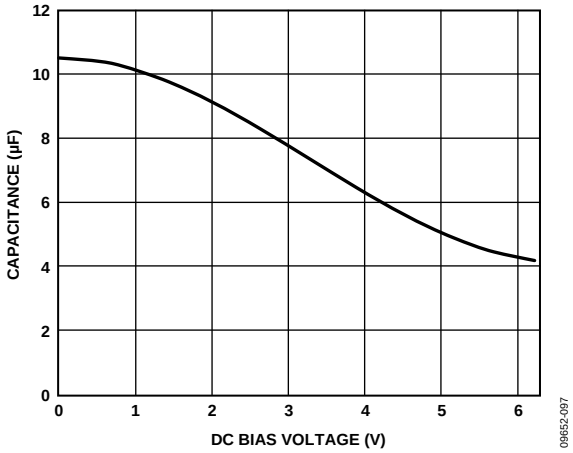

Figure 108. Typical Capacitor Performance

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \approx \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 7 µF and a maximum of 40 µF.

Table 10. Suggested 10 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
Taiyo Yuden	X5R	JMK107BJ106MA-T	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3
Panasonic	X5R	ECJ1VB0J106M	0603	6.3

The buck regulator requires 10 µF output capacitors to guarantee stability and response to rapid load variations and to transition in and out the PWM/PSM modes. In certain applications where the buck regulator powers a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 µF to 4.7 µF because the regulator does not expect a large load variation when working in PSM mode (see Figure 109).

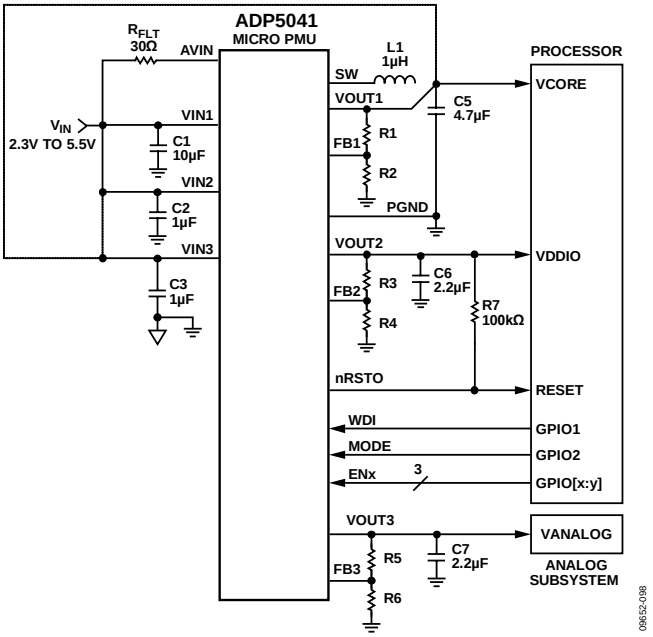

Figure 109. Processor System Power Management with PSM/PWM Control

Input Capacitor

A higher value input capacitor helps to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the buck as possible. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 µF and a maximum of 10 µF. A list of suggested capacitors is shown in Table 11.

Table 11. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475ME19D	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
Panasonic	X5R	ECJ-0EB0J475M	0402	6.3

LDO EXTERNAL COMPONENT SELECTION

Feedback Resistors

The maximum value of Rb is not to exceed 200 kΩ (see Figure 103).

OUTPUT CAPACITOR

The ADP5041 LDOs are designed for operation with small, space-saving ceramic capacitors, but they function with most commonly used capacitors as long as care is taken with the ESR value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the LDO. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the LDO to large changes in load current.

When operating at output currents higher than 200 mA a minimum of 2.2 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the LDO.

Table 12. Suggested 2.2 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188B31A225K	0402	10.0
TDK	X5R	C1608JB0J225KT	0402	6.3
Panasonic	X5R	ECJ1VB0J225K	0402	6.3
Taiyo Yuden	X5R	JMK107BJ225KK-T	0402	6.3

Input Bypass Capacitor

Connecting 1 µF capacitors from VIN2 and VIN3 to ground reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance is encountered. If greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

Table 13. Suggested 1.0 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM155B30J105K	0402	6.3
TDK	X5R	C1005JB0J105KT	0402	6.3
Panasonic	X5R	ECJ0EB0J105K	0402	6.3
Taiyo Yuden	X5R	LMK105BJ105MV-F	0402	10.0

Input and Output Capacitor Properties

Use any good quality ceramic capacitor with the ADP5041 as long as it meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

Figure 110 depicts the capacitance vs. dc voltage bias characteristic of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

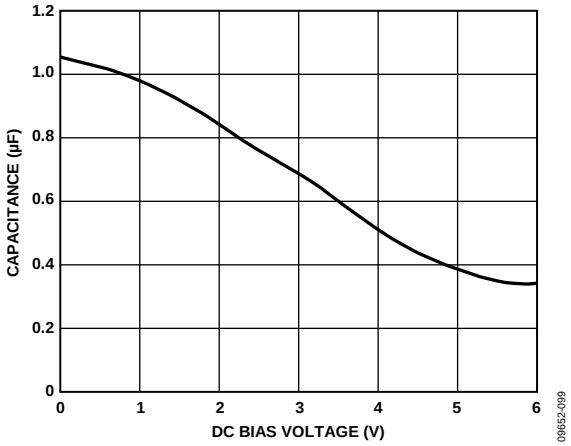

Figure 110. Capacitance vs. Voltage Characteristic

Use the following equation to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 110.

Substituting these values into the following equation yields:

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.72\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5041, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

SUPERVISORY SECTION

Threshold Setting Resistors

Referring to Figure 105, the maximum value of R2 is not to exceed 200 kΩ.

Watchdog Input Current

To minimize watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 25 µA. Pulsing WDI low-to-high-to-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

Negative-Going Transients at the Monitored Rail

To avoid unnecessary resets caused by fast power supply transients, the ADP5041 is equipped with glitch rejection circuitry. The typical performance characteristic in Figure 111 plots the monitored rail voltage, V_{TH}, transient duration vs. the transient magnitude. The curve shows combinations of transient magnitude and duration for which a reset is not generated. In this example, with the 3.00 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any larger in magnitude or duration, a reset is generated. In this example, the reset threshold programming resistor values were R2 = 200 kΩ, R1 = 1 MΩ (see Figure 105).

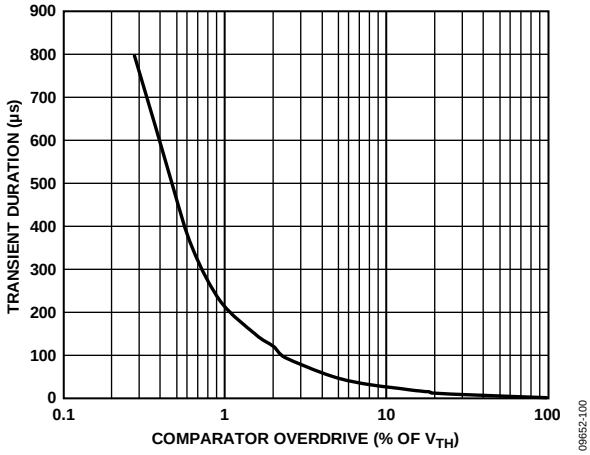

Figure 111. Maximum V_{TH} Transient Duration vs. Reset Threshold Overdrive

Watchdog Software Considerations

In implementing the watchdog strobe code of the microprocessor, quickly switching WDI low to high and then high to low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-to-high-to-low WDI pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine is held in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI.

A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset (see Figure 112).

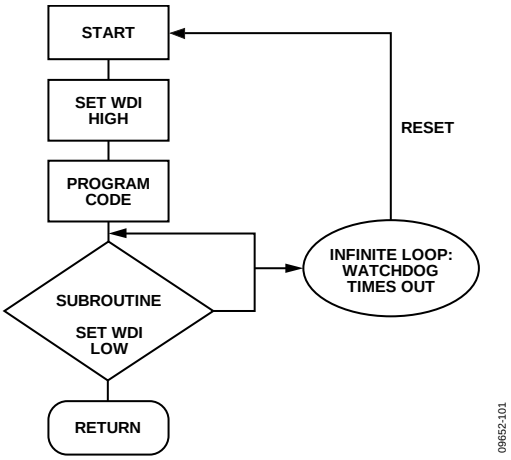

Figure 112. Watchdog Flow Diagram

POWER DISSIPATION/THERMAL CONSIDERATIONS

The ADP5041 is a highly efficient micropower management unit (micro PMU), and in most cases the power dissipated in the device is not a concern. However, if the device operates at high ambient temperatures and with maximum loading conditions, the junction temperature can reach the maximum allowable operating limit (125°C).

When the junction temperature exceeds 150°C, the ADP5041 turns off all the regulators, allowing the device to cool down. Once the die temperature falls below 135°C, the ADP5041 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device and to make sure the ADP5041 operates below the maximum allowable junction temperature.

The efficiency for each regulator on the ADP5041 is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (1)$$

where:
η is efficiency.
P_{IN} is the input power.
P_{OUT} is the output power.

Power loss is given by

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (2a)$$

or

$$P_{LOSS} = P_{OUT}\,(1\text{-}\eta)/\eta \quad (2b)$$

The power dissipation of the supervisory function is small and negligible.

Power dissipation can be calculated in several ways. The most intuitive and practical is to measure the power dissipated at the input and all the outputs. The measurements should be performed at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is dissipated in the device and the inductor. Use Equation 4 to derive the power lost in the inductor, and from this use Equation 3 to calculate the power dissipation in the ADP5041 buck regulator.

A second method to estimate the power dissipation uses the efficiency curves provided for the buck regulator, wheras the power lost on a LDO is calculated using Equation 12. When the buck efficiency is known, use Equation 2b to derive the total power lost in the buck regulator and inductor. Use Equation 4 to derive the power lost in the inductor, and then calculate the power dissipation in the buck converter using Equation 3. Add the power dissipated in the buck and in the LDOs to find the total dissipated power.

Note that the buck efficiency curves are typical values and may not be provided for all possible combinations of V_{IN}, V_{OUT}, and I_{OUT}. To account for these variations, it is necessary to include a safety margin when calculating the power dissipated in the buck.

A third way to estimate the power dissipation is analytical and involves modeling the losses in the buck circuit provided by Equation 8 to Equation 11 and the losses in the LDOs provided by Equation 12.

Buck Regulator Power Dissipation

The power loss of the buck regulator is approximated by

$$P_{LOSS} = P_{DBUCK} + P_L \quad (3)$$

where:
P_{DBUCK} is the power dissipation on the ADP5041 buck regulator.
P_L is the inductor power losses.

The inductor losses are external to the device and they do not have any effect on the die temperature.

The inductor losses are estimated (without core losses) by

$$P_L \cong I_{OUT1(RMS)}{}^2 \times DCR_L \quad (4)$$

where:

DCR_L is the inductor series resistance.
$I_{OUT1(RMS)}$ is the rms load current of the buck regulator.

$$I_{OUT1(RMS)} = I_{OUT1} \times \sqrt{1 + r/12} \quad (5)$$

where r is the normalized inductor ripple current.

$$r \approx V_{OUT1} \times (1\text{-}D)/(I_{OUT1} \times L \times f_{SW}) \quad (6)$$

where:

L is inductance.
f_{SW} is switching frequency.
D is duty cycle.

$$D = V_{OUT1}/V_{IN1} \quad (7)$$

The ADP5041 buck regulator power dissipation, P_{DBUCK}, includes the power switch conductive losses, the switch losses, and the transition losses of each channel. There are other sources of loss, but these are generally less significant at high output load currents, where the thermal limit of the application is. Equation 8 shows the calculation made to estimate the power dissipation in the buck regulator.

$$P_{DBUCK} = P_{COND} + P_{SW} + P_{TRAN} \quad (8)$$

The power switch conductive losses are due to the output current, I_{OUT1}, flowing through the PMOSFET and the NMOSFET power switches that have internal resistance, $R_{DSON\text{-}P}$ and $R_{DSON\text{-}N}$. The amount of conductive power loss is found by:

$$P_{COND} = [R_{DSON\text{-}P} \times D + R_{DSON\text{-}N} \times (1 - D)] \times I_{OUT1}{}^2 \quad (9)$$

For the ADP5041, at 125°C junction temperature and VIN1 = 3.6 V, $R_{DSON\text{-}P}$ is approximately 0.2 Ω, and $R_{DSON\text{-}N}$ is approximately 0.16 Ω. At VIN1 = 2.3 V, these values change to 0.31 Ω and 0.21 Ω respectively, and at VIN1 = 5.5 V, the values are 0.16 Ω and 0.14 Ω, respectively.

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. The amount of switching power loss is given by:

$$P_{SW} = (C_{GATE\text{-}P} + C_{GATE\text{-}N}) \times V_{IN1}{}^2 \times f_{SW} \quad (10)$$

where:

$C_{GATE\text{-}P}$ is the PMOSFET gate capacitance.
$C_{GATE\text{-}N}$ is the NMOSFET gate capacitance.

For the ADP5041, the total of ($C_{GATE\text{-}P}$ + $C_{GATE\text{-}N}$) is approximately 150 pF.

The transition losses occur because the PMOSFET cannot be turned on or off instantaneously, and the SW node takes some time to slew from near ground to near V_{OUT1} (and from V_{OUT1} to ground). The amount of transition loss is calculated by:

$$P_{TRAN} = V_{IN1} \times I_{OUT1} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (11)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node, SW. For the ADP5041, the rise and fall times of SW are in the order of 5 ns.

If the preceding equations and parameters are used for estimating the converter efficiency, it must be noted that the equations do not describe all of the converter losses, and the parameter values given are typical numbers. The converter performance also depends on the choice of passive components and board layout; therefore, a sufficient safety margin should be included in the estimate.

LDO Regulator Power Dissipation

The power loss of a LDO regulator is given by:

$$P_{DLDO} = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (12)$$

where:
I_{LOAD} is the load current of the LDO regulator.
V_{IN} and V_{OUT} are input and output voltages of the LDO, respectively.
I_{GND} is the ground current of the LDO regulator.

Power dissipation due to the ground current is small and it can be ignored.

The total power dissipation in the ADP5041 simplifies to:

$$P_D = \{[P_{DBUCK} + P_{DLDO1} + P_{DLDO2}]\} \quad (13)$$

Junction Temperature

In cases where the board temperature, T_A, is known, the thermal resistance parameter, θ_{JA}, can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (14)$$

The typical θ_{JA} value for the 20-lead, 4 mm × 4 mm LFCSP is 38°C/W (see Table 7). A very important factor to consider is that θ_{JA} is based on a 4-layer, 4 inch × 3 inch, 2.5 oz copper, as per JEDEC standard, and real applications may use different sizes and layers. To remove heat from the device, it is important to maximize the use of copper. Copper exposed to air dissipates heat better than copper used in the inner layers. The exposed pad (EP) should be connected to the ground plane with several vias as shown in Figure 114.

If the case temperature can be measured, the junction temperature is calculated by

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (15)$$

where:
T_C is the case temperature.
θ_{JC} is the junction-to-case thermal resistance provided in Table 7.

When designing an application for a particular ambient temperature range, calculate the expected ADP5041 power dissipation (P_D) due to the losses of all channels by using Equation 8 to Equation 13. From this power calculation, the junction temperature, T_J, can be estimated using Equation 14.

The reliable operation of the buck regulator and the LDO regulator can be achieved only if the estimated die junction temperature of the ADP5041 (Equation 14) is less than 125°C. Reliability and mean time between failures (MTBF) is highly affected by increasing the junction temperature. Additional information about product reliability can be found in the Analog Devices, Inc., Reliability Handbook, which is available at http://www.analog.com/reliability_handbook.

APPLICATION DIAGRAM

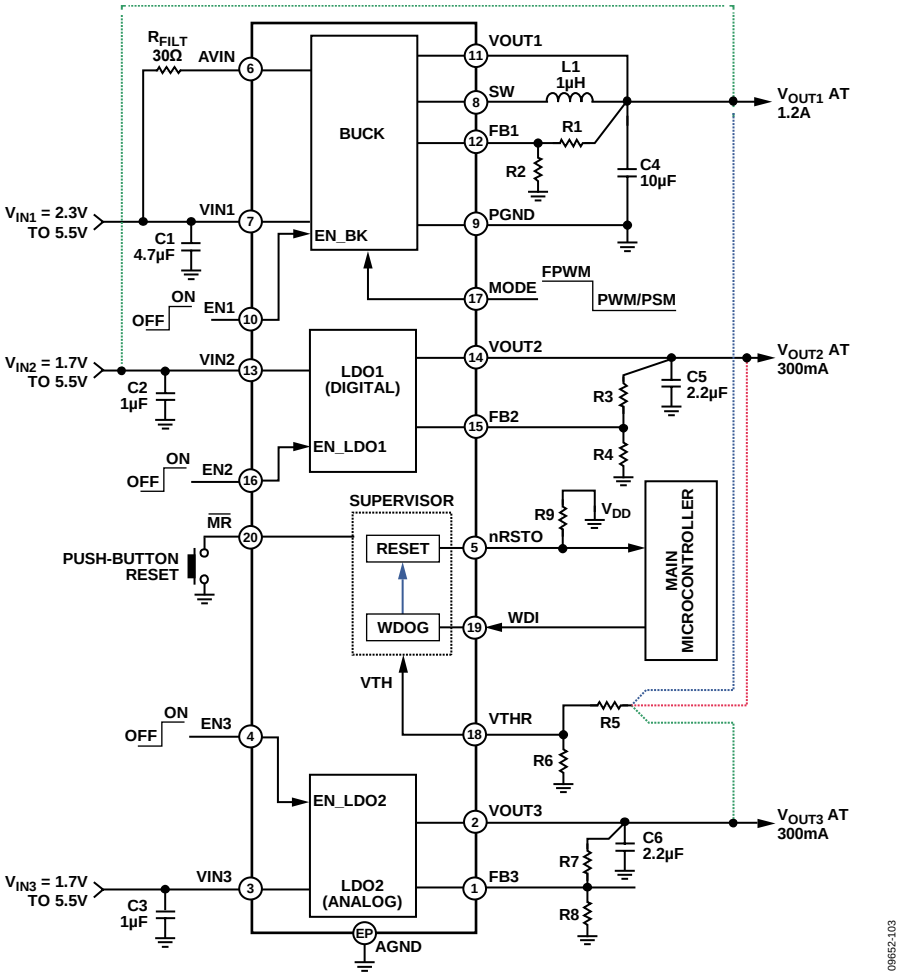

Figure 113. Application Diagram

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5041 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

SUGGESTED LAYOUT

See Figure 114 for an example layout.

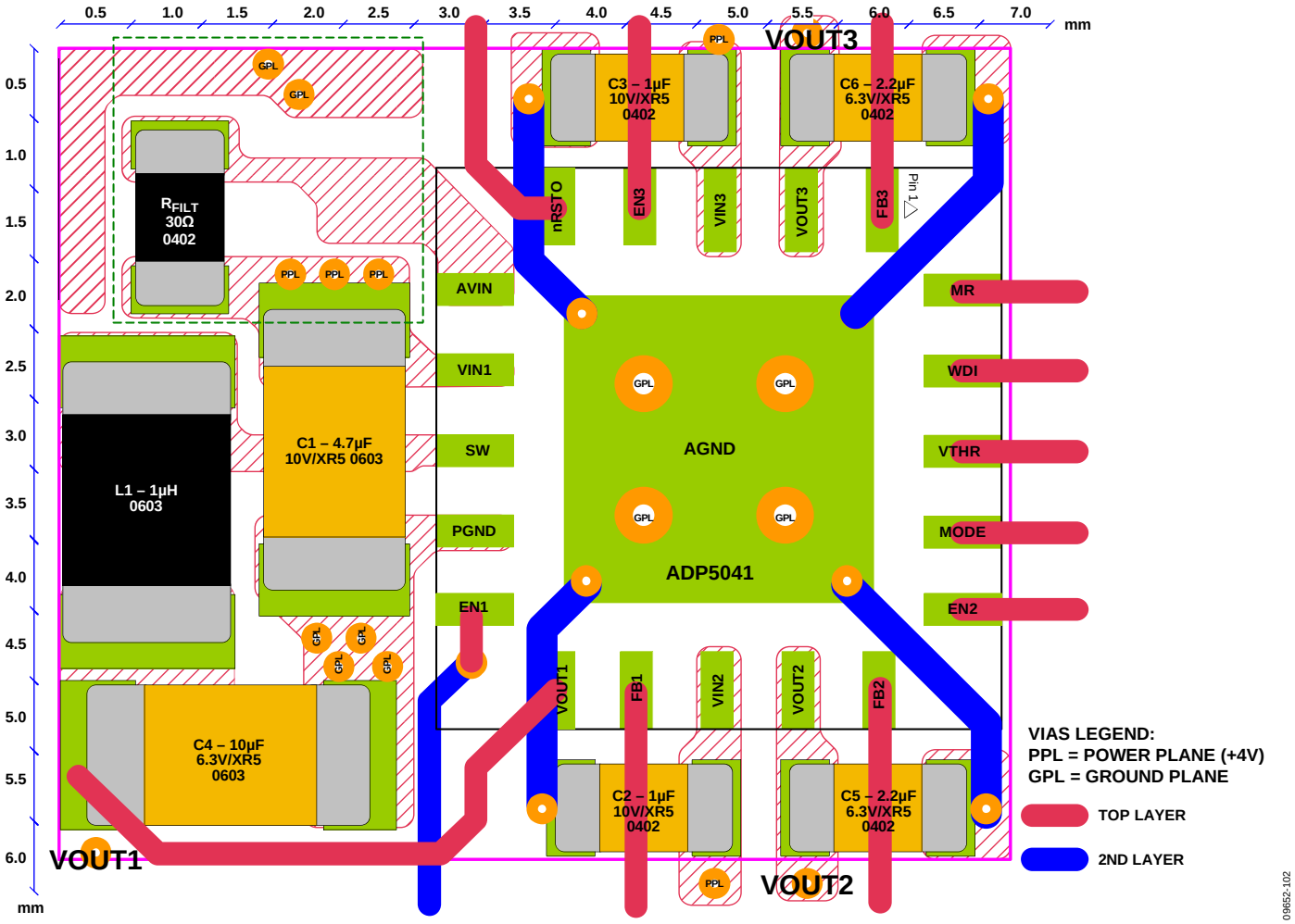

Figure 114. Suggested Board Layout

BILL OF MATERIALS

Table 14.

Reference	Value	Part Number	Vendor	Package
C1	4.7 µF, X5R, 6.3 V	JMK107BJ475	Taiyo-Yuden	0603
C2, C3	1 µF, X5R, 6.3 V	LMK105BJ105MV-F	Taiyo-Yuden	0402
C4	10 µF, X5R, 6.3 V	JMK107BJ106MA-T	Taiyo-Yuden	0603
C5,C6	2.2 µF, X5R, 6.3 V	JMK105BJ225MV-F	Taiyo-Yuden	0402
L1	1 µH, 85 mΩ, 1400 mA	LQM2MPN1R0NG0B	Murata	2.0 × 1.6 × 0.9 (mm)
	1 µH, 85 mΩ, 1350 mA	MDT2520-CN	Toko	2.5 × 2.0 × 1.2 (mm)
	1 µH, 89 mΩ, 1800 mA	XPL2010-1102ML	Coilcraft	1.9 × 2.0 × 1.0 (mm)
IC1	3-regulator micro PMU	ADP5041	Analog Devices	20-Lead LFCSP

FACTORY PROGRAMMABLE OPTIONS

Table 15. Regulator Output Discharge Resistor Options

Options	Description
Option 0	All discharge resistors disabled
Option 1	All discharge resistors enabled

Table 16. Undervoltage Lockout Options

Options	Min	Typ	Max	Unit
Option 0	1.95	2.15	2.275	V
Option 1	3.10	3.65	3.90	V

Table 17. Reset Timeout Options

Options	Min	Typ	Max	Unit
Option 0	24	30	36	ms
Option 1	160	200	240	ms

Table 18. Watchdog Timer Options

Selection	Min	Typ	Max	Unit
Option 0	81.6	102	122.4	ms
Option 1	1.28	1.6	1.92	sec

OUTLINE DIMENSIONS

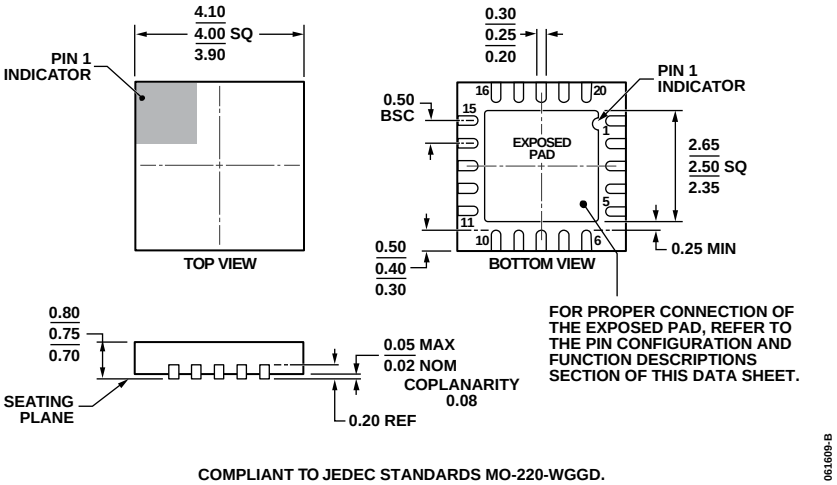

Figure 115. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Settings	Temperature Range	Package Description	Package Option
ADP5041ACPZ-1-R7	WD t_{OUT} = 1.6 sec Min reset t_{OUT} = 160 ms V_{UVLO} = 2.15 V Discharge resistors enabled	T_J = −40°C to +125°C	20-Lead LFCSP_WQ	CP-20-10
ADP5041CP-1-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.