350 mA, Low V_{IN}, Low Quiescent Current, CMOS Linear Regulator

ADP130

FEATURES

350 mA maximum output current
Input voltage supply range
V_{BIAS} = 2.3 V to 5.5 V
V_{IN} = 1.2 V to 3.6 V
2.3 V < V_{IN} < 3.6 V, VIN can be tied to VBIAS
Very low dropout voltage: 17 mV @ 100 mA load
Low quiescent current: 25 µA @ no load
Low shutdown current: <1 µA
±1% accuracy @ 25°C
Excellent PSRR performance: 70 dB @ 10 kHz
Excellent load/line transient response
Optimized for small 1 µF ceramic capacitors
Current limit and thermal overload protection
Logic controlled enable
5-lead TSOT package

APPLICATIONS

Mobile phones
Digital camera and audio devices
Portable and battery-powered equipment
Post dc-to-dc regulation

TYPICAL APPLICATION CIRCUITS

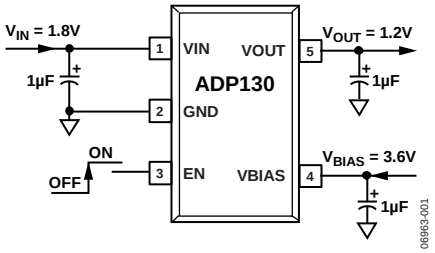

Figure 1.

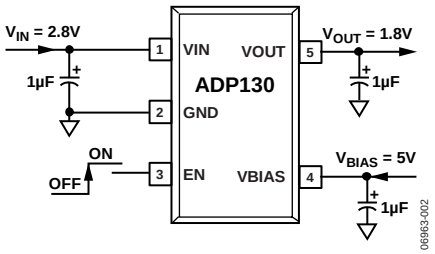

Figure 2.

GENERAL DESCRIPTION

The ADP130 is a low quiescent current, low dropout linear regulator. It is designed to operate in dual-supply mode with an input voltage as low as 1.2 V to increase efficiency and provide up to 350 mA of output current. The low 17 mV dropout voltage at a 100 mA load improves efficiency and allows operation over a wider input voltage range.

A dual-supply power solution typically improves conversion efficiency over a single-supply solution because the higher V_{BIAS} supply powers the part, and the lower V_{IN} supply delivers current to the load. The power dissipated in the device is thereby reduced.

The ADP130 is optimized for stable operation with small 1 µF ceramic output capacitors. The ADP130 delivers good transient performance with minimal board area.

The ADP130 is available in fixed output voltages ranging from : 0.80 V to 3.0 V.

The ADP130 has a typical internal soft start time of 200 µs. Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions. The ADP130 is available in a tiny 5-lead TSOT package for the smallest footprint solution to meet a variety of portable power applications.

Rev. B

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7/08—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{OUT} + 0.4 V, V_{BIAS} = 5 V, I_{OUT} = 10 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, C_{BIAS} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	1.2		3.6	V
BIAS VOLTAGE RANGE	V_{BIAS}	T_J = −40°C to +125°C	2.3		5.5	V
OPERATING SUPPLY CURRENT	I_{VIN}[1]	I_{OUT} = 0 µA		25		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			44	µA
		I_{OUT} = 1 mA		40		µA
		I_{OUT} = 1 mA, T_J = −40°C to +125°C			58	µA
		I_{OUT} = 100 mA		100		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			130	µA
		I_{OUT} = 350 mA		160		µA
		I_{OUT} = 350 mA, T_J = −40°C to +125°C			220	µA
BIAS OPERATING CURRENT	I_{BIAS}			16		µA
		T_J = −40°C to +125°C			28	µA
SHUTDOWN CURRENT	I_{SD-VIN}	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +85°C			1.0	µA
		EN = GND, T_J = +85°C to +125°C			20	µA
	$I_{SD-VBIAS}$	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		1 mA < I_{OUT} < 350 mA, V_{IN} = (V_{OUT} + 0.4 V) to 3.6 V	−2		+2	%
		1 mA < I_{OUT} < 350 mA, V_{IN} = (V_{OUT} + 0.4 V) to 3.6 V, T_J = −40°C to +125°C	−3		+3	%
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 3.6 V, T_J = −40°C to +125°C	−0.10		+0.10	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 350 mA		0.001		%/mA
		I_{OUT} = 10 mA to 350 mA, T_J = −40°C to +125°C			0.005	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 10 mA, V_{BIAS} = 2.3 V, V_{OUT} = 3 V		2		mV
		I_{OUT} = 10 mA, V_{BIAS} = 2.3 V, V_{OUT} = 3 V, T_J = −40°C to +125°C			3.5	mV
		I_{OUT} = 100 mA, V_{BIAS} = 2.3 V, V_{OUT} = 3 V		17		mV
		I_{OUT} = 100 mA, V_{BIAS} = 2.3 V, V_{OUT} = 3 V, T_J = −40°C to +125°C			28	mV
		I_{OUT} = 350 mA, V_{BIAS} = 2.3 V, V_{OUT} = 3 V		70		mV
		I_{OUT} = 350 mA, V_{BIAS} = 2.3 V, V_{OUT} = 3 V, T_J = −40°C to +125°C			100	mV
START-UP TIME[4]	$T_{START-UP}$	V_{OUT} = 1.2 V		200		µs
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		400	550	1000	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.3 V ≤ V_{BIAS} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.3 V ≤ V_{BIAS} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = BIAS or GND		0.1		µA
		EN = BIAS or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			2.1	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	1.5			V
Hysteresis	$UVLO_{HYS}$			180		mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 0.8 V		29		μV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 1.2 V		38		μV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 1.5 V		43		μV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 2.5 V		61		μV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 3.0 V		77		μV rms
POWER SUPPLY REJECTION RATIO	PSRR	Modulated bias, 10 kHz, V_{OUT} = 3.0 V, V_{IN} = 3.6 V, V_{BIAS} = 5 V		70		dB
		Modulated bias, 100 kHz, V_{OUT} = 3.0 V, V_{IN} = 3.6 V, V_{BIAS} = 5 V		53		dB
		Modulated V_{IN}, 10 kHz, V_{OUT} = 1.2 V, V_{IN} = V_{OUT} + 1 V, V_{BIAS} = 5 V		70		dB
		Modulated V_{IN}, 100 kHz, V_{OUT} = 1.2 V, V_{IN} = V_{OUT} + 1 V, V_{BIAS} = 5 V		54		dB
		Modulated V_{IN}, 10 kHz, V_{OUT} = 0.8 V, V_{IN} = V_{OUT} + 1 V, V_{BIAS} = 5 V		70		dB
		Modulated V_{IN}, 100 kHz, V_{OUT} = 0.8 V, V_{IN} = V_{OUT} + 1 V, V_{BIAS} = 5 V		55		dB

[1] $I_{VIN} = I_{GND} - I_{BIAS}$, where I_{GND} is the current flowing from the GND pin.
[2] Based on an endpoint calculation using 1 mA and 350 mA loads.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 1.3 V.
[4] Start-up time is defined as the time from the rising edge of EN to VOUT being at 90% of its nominal value.
[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 2.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 2.0 V, or 1.8 V.

INPUT AND OUTPUT CAPACITOR: RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	0.70	1		μF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		1	Ω

[1] The minimum input and output capacitance should be >0.70 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended. Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +3.6 V
VBIAS to GND	−0.3 V to +6 V
EN to GND	−0.3 V to +6 V
VOUT to GND	−0.3 V to VIN
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Operating Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply only individually, not in combination. The ADP130 may be damaged when junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). T_J is calculated using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a four-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a four-layer, 4 in × 3 in circuit board. For details about board construction, refer to JEDEC JESD51-7.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a four-layer board. The JEDEC JESD51-12 document, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path, as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D), using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to the JEDEC JESD51-8 and JESD51-12 documents for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

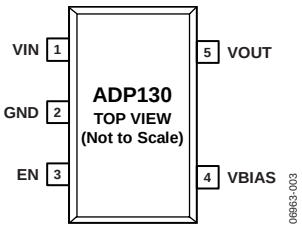

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Regulator Input Supply. Bypass VIN to GND with a capacitor of 1 µF or greater.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VBIAS
4	VBIAS	Bias Input Supply. Connect a capacitor of 1 µF or greater between VBIAS and GND.
5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a capacitor of 1 µF or greater.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{BIAS} = 5 V, V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = C_{BIAS} = 1 µF, T_A = 25°C, unless otherwise noted.

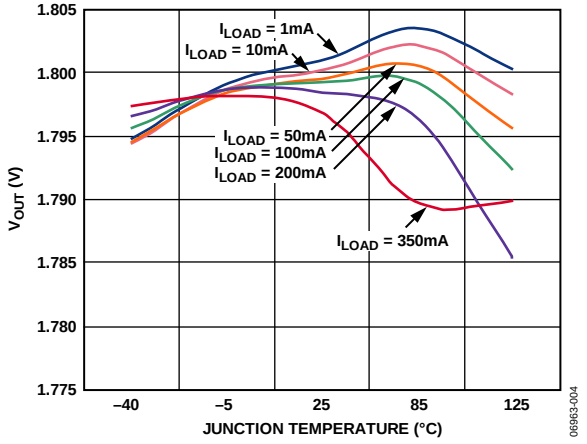

Figure 4. Output Voltage vs. Junction Temperature

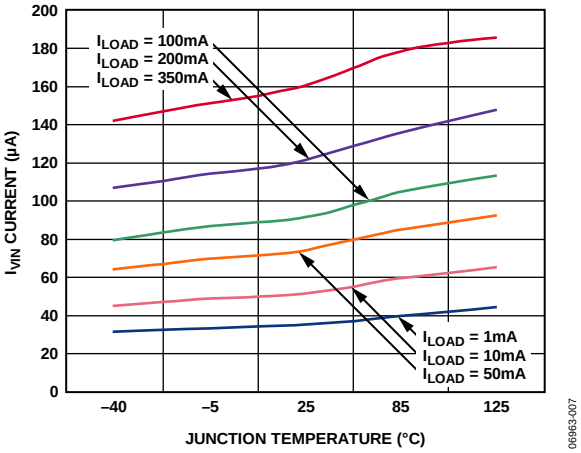

Figure 7. I_{VIN} Current vs. Junction Temperature

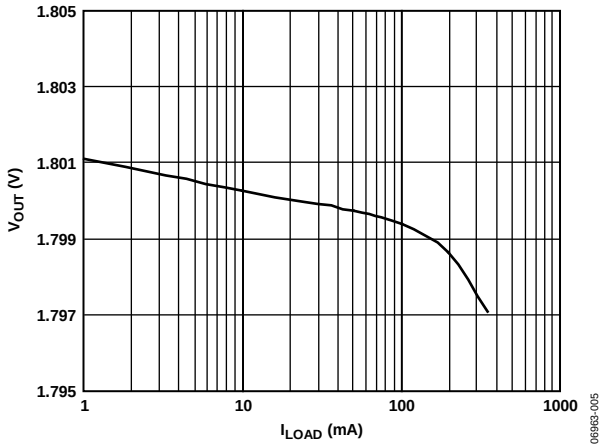

Figure 5. Output Voltage vs. Load Current

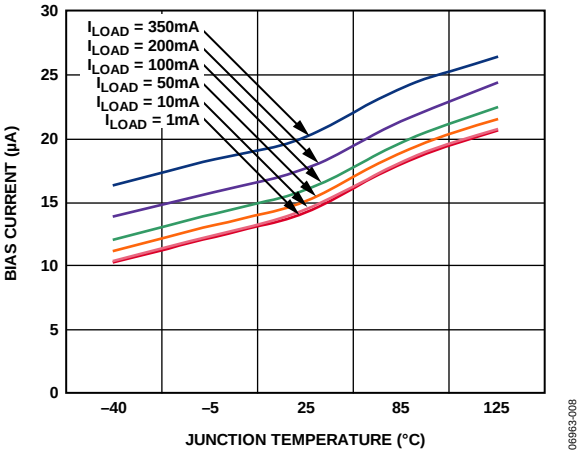

Figure 8. Bias Current vs. Junction Temperature

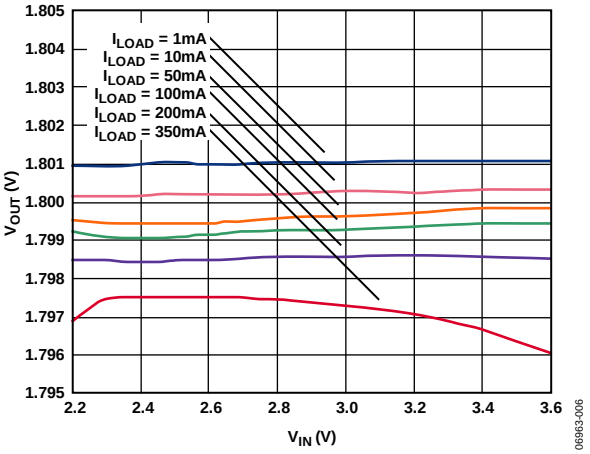

Figure 6. Output Voltage vs. Input Voltage

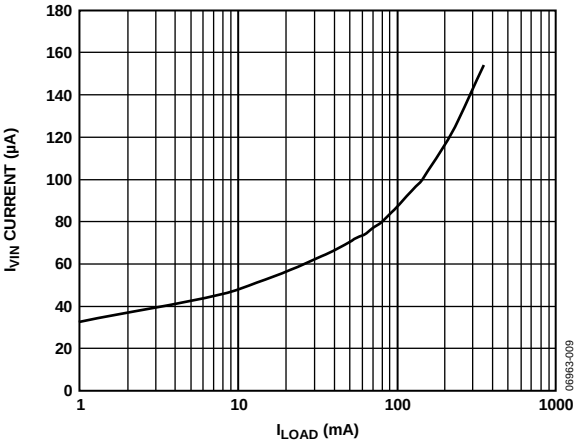

Figure 9. I_{VIN} Current vs. Load Current

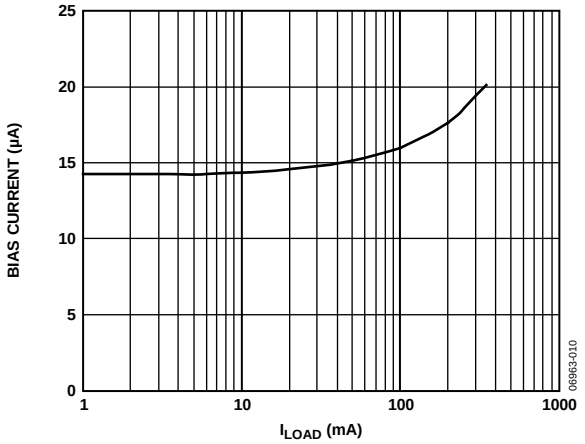

Figure 10. Bias Current vs. Load Current

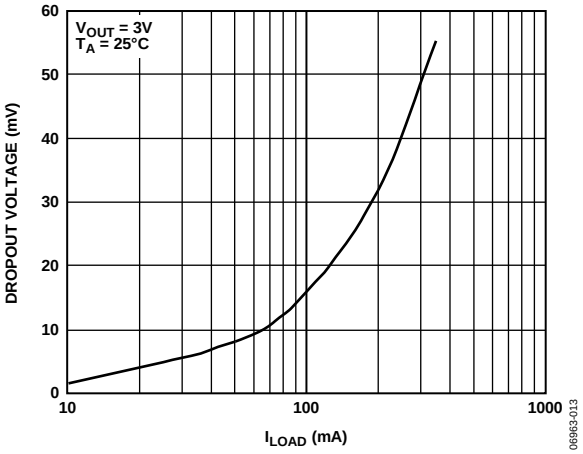

Figure 13. Dropout Voltage vs. Load Current, V_{OUT} = 3 V

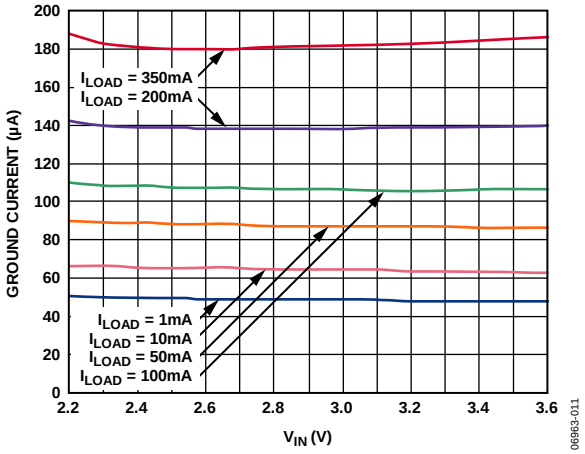

Figure 11. Ground Current vs. Input Voltage

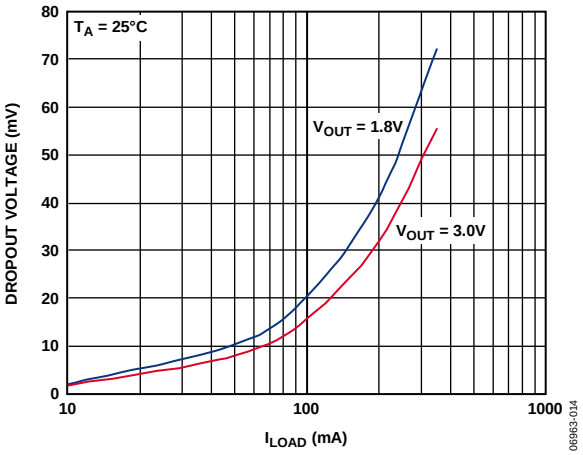

Figure 14. Dropout Voltage vs. Output Voltage and Load Current

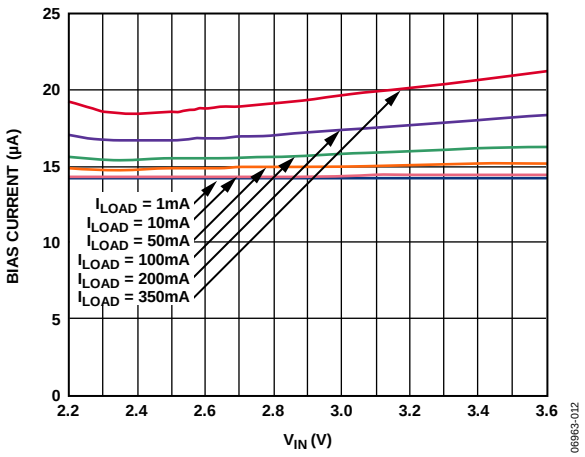

Figure 12. Bias Current vs. Input Voltage

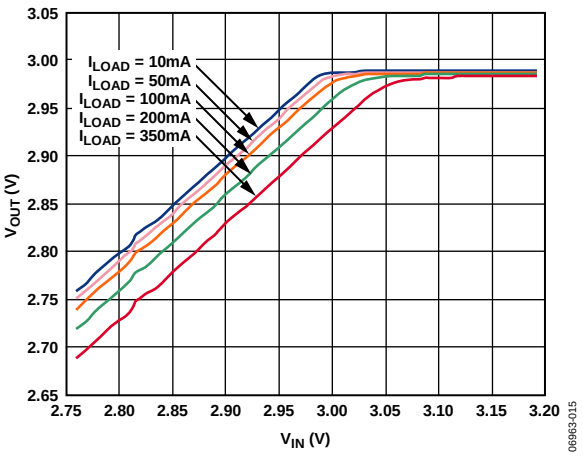

Figure 15. Output Voltage vs. Input Voltage (in Dropout), V_{OUT} = 3 V

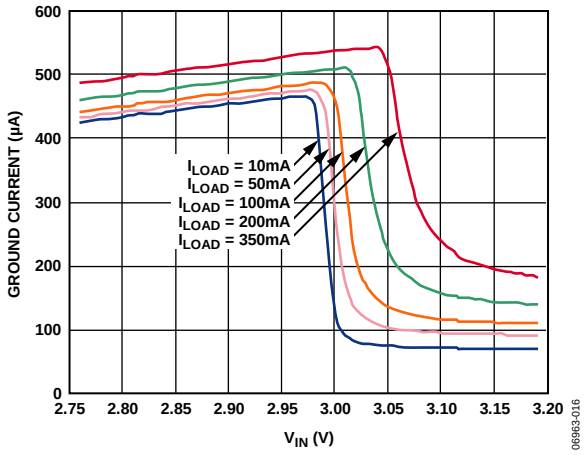

Figure 16. Ground Current vs. Input Voltage (in Dropout), V_{OUT} = 3 V

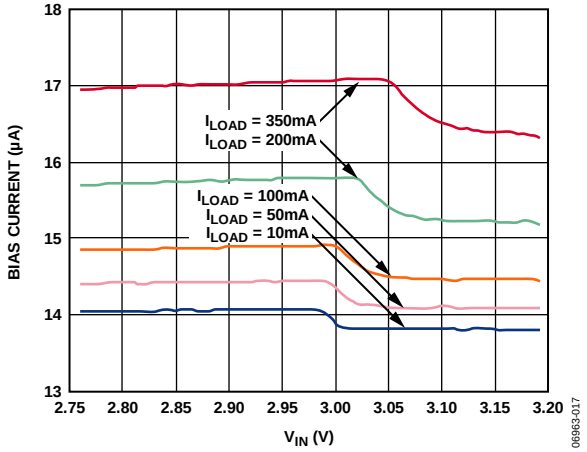

Figure 17. Bias Current vs. Input Voltage (in Dropout), V_{OUT} = 3 V

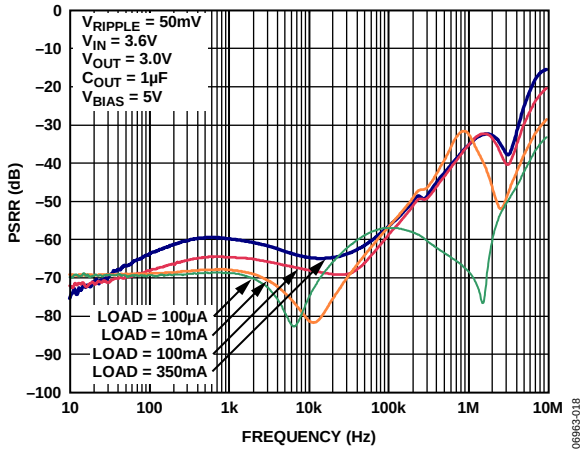

Figure 18. Power Supply Rejection Ratio vs. Frequency, V_{IN} Input

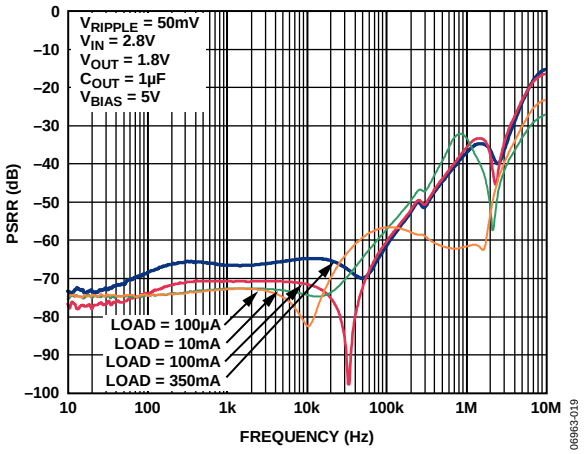

Figure 19. Power Supply Rejection Ratio vs. Frequency, V_{IN} Input

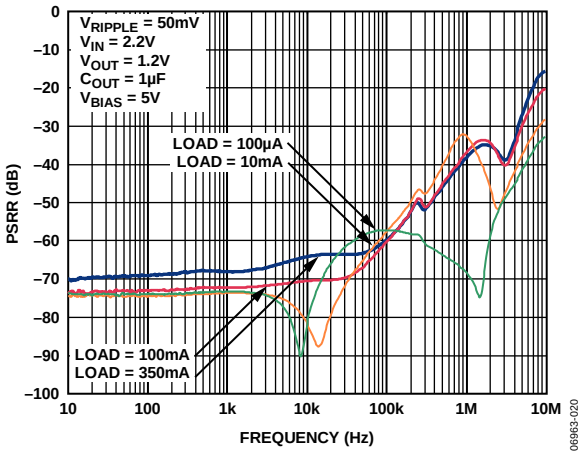

Figure 20. Power Supply Rejection Ratio vs. Frequency, V_{IN} Input

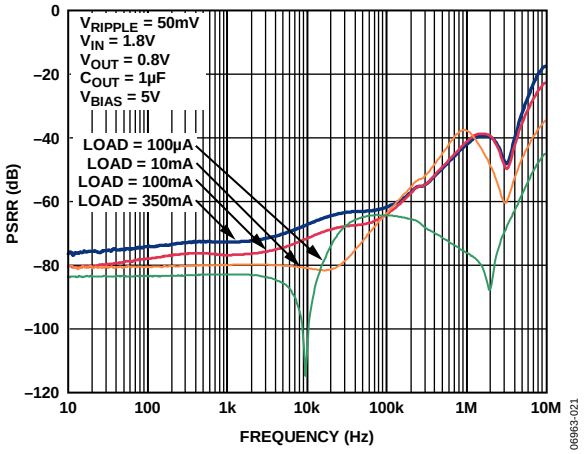

Figure 21. Power Supply Rejection Ratio vs. Frequency, V_{IN} Input

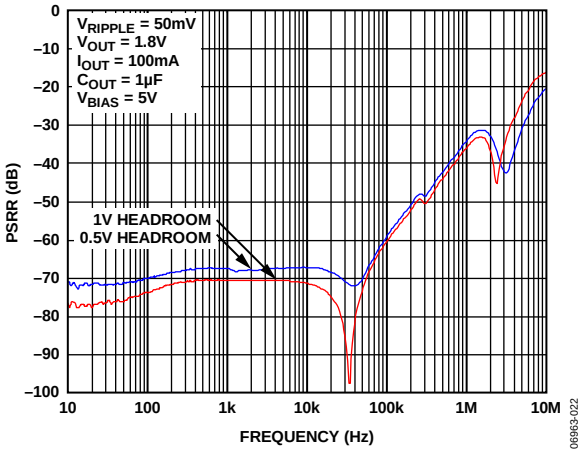

Figure 22. Power Supply Rejection Ratio vs. Headroom, V_{IN} Input

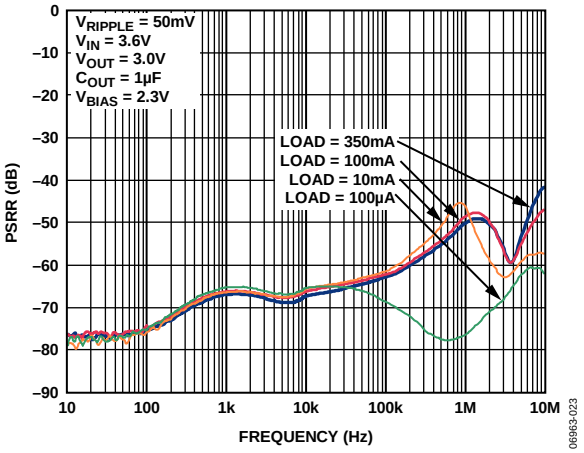

Figure 23. Power Supply Rejection Ratio vs. Frequency, V_{BIAS} Input

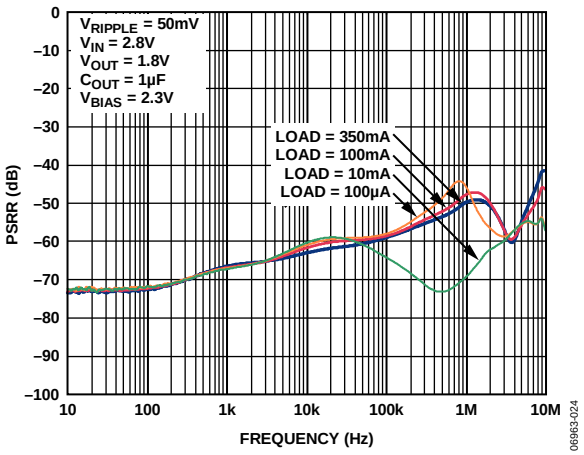

Figure 24. Power Supply Rejection Ratio vs. Frequency, V_{BIAS} Input

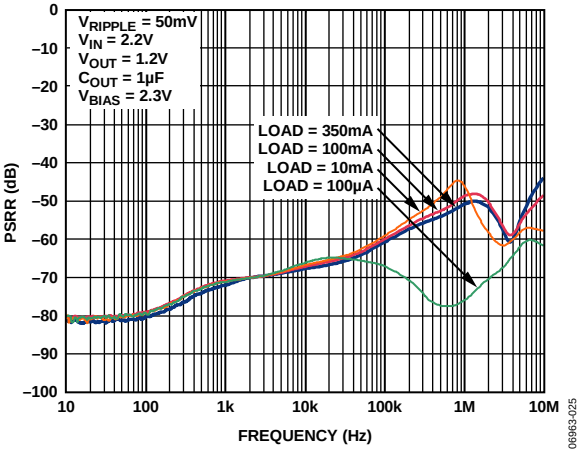

Figure 25. Power Supply Rejection Ratio vs. Frequency, V_{BIAS} Input

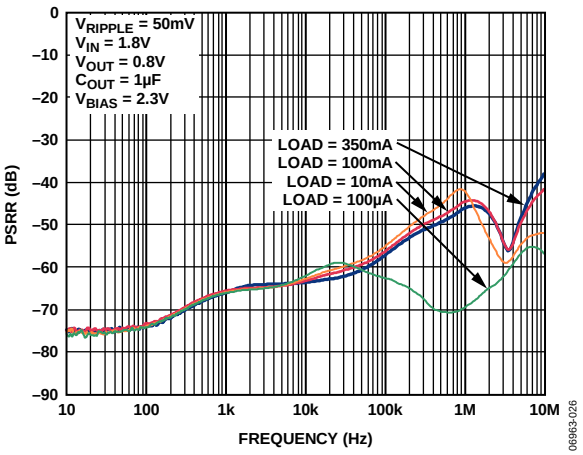

Figure 26. Power Supply Rejection Ratio vs. Frequency, V_{BIAS} Input

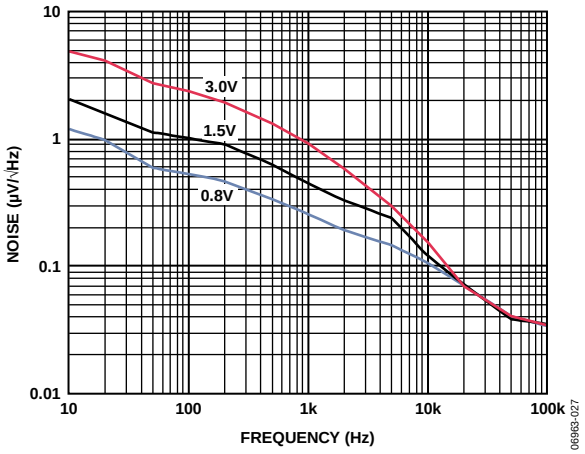

Figure 27. Noise Spectrum vs. V_{OUT}

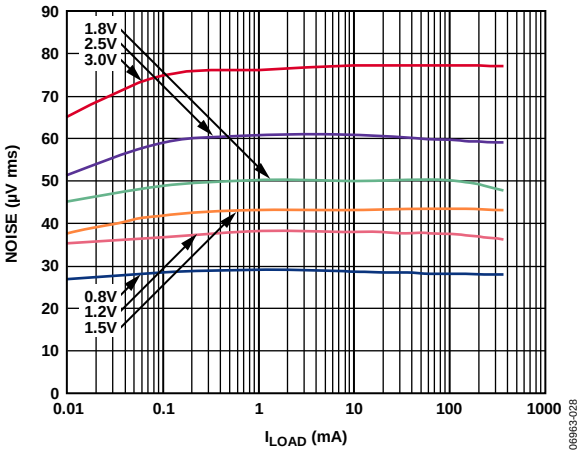

Figure 28. Output Noise vs. Load Current and Output Voltage

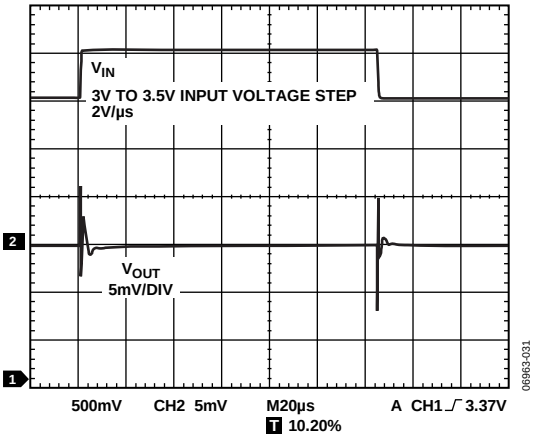

Figure 31. V_{IN} Line Transient Response, V_{BIAS} = 5 V, I_{OUT} = 1 mA

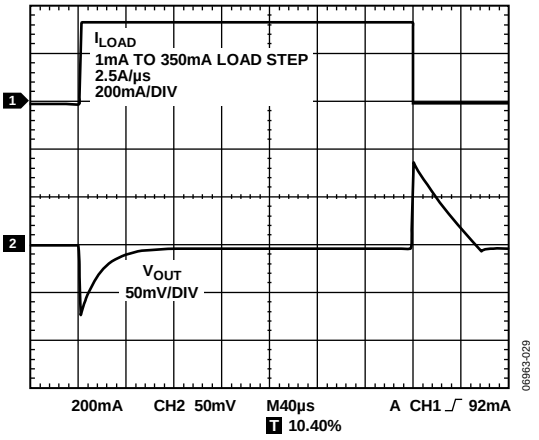

Figure 29. Load Transient Response

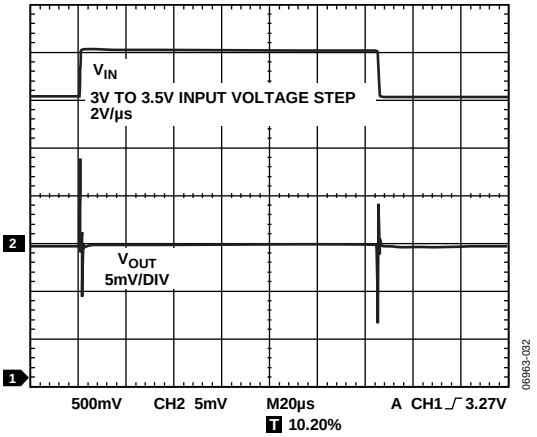

Figure 32. V_{IN} Line Transient Response, V_{BIAS} = 5 V, I_{OUT} = 350 mA

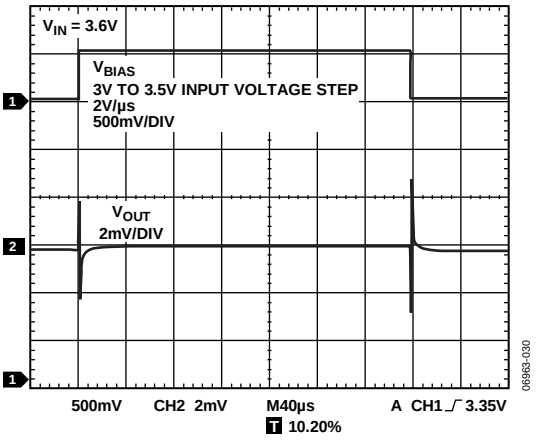

Figure 30. V_{BIAS} Line Transient Response, V_{IN} = 3.6 V, I_{OUT} = 350 mA

THEORY OF OPERATION

The ADP130 is a low dropout, linear regulator that uses an advanced proprietary architecture to achieve low quiescent current and high efficiency regulation. It also provides high power supply rejection ratio (PSRR) and excellent line and load transient response using a small 1 µF ceramic output capacitor. The device operates from a 2.3 V to 5.5 V bias rail and a 1.2 V to 3.6 V input rail to provide up to 350 mA of output current. Supply current in shutdown mode is typically less than 1 µA.

Internally, the ADP130 consists of a reference, an error amplifier, a feedback voltage divider, and a pass device. The output current is delivered via the pass device, which is controlled by the error amplifier, forming a negative feedback system that ideally drives the feedback voltage to equal the reference voltage. If the feedback voltage is lower than the reference voltage, the negative feedback drives more current, increasing the output voltage. If the feedback voltage is higher than the reference voltage, the negative feedback drives less current, decreasing the output voltage. The VBIAS pin is the positive supply for all circuitry except the pass device.

The ADP130 has an internal soft start that limits the output voltage ramp period to approximately 200 µs. All internal devices are controlled by the enable pin, EN. When EN is high, the output is on; when EN is low, the output is off.

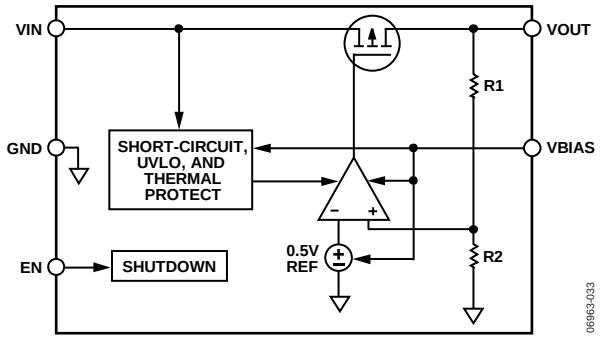

Figure 33. Internal Block Diagram

The ADP130 is available in output voltages ranging from 0.8 V to 3.0 V. The ADP130 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on. When EN is low, VOUT turns off. For automatic startup, EN can be tied to VBIAS.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP130 is designed for operation with small, space-saving ceramic capacitors, but it functions with most commonly used capacitors as long as care is taken regarding the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP130. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP130 to large changes in load current. Figure 34 and Figure 35 show the transient responses for output capacitance values of 1 µF and 10 µF, respectively.

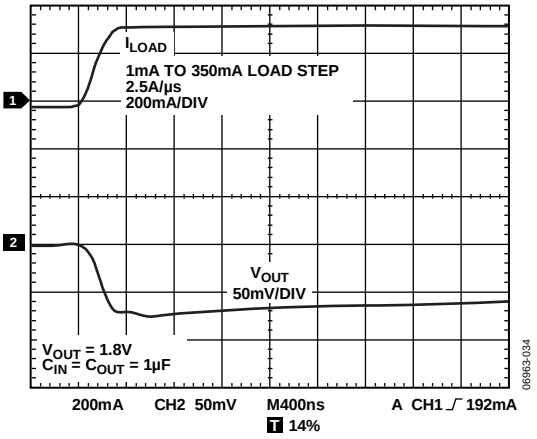

Figure 34. Output Transient Response, C_{OUT} = 1 µF

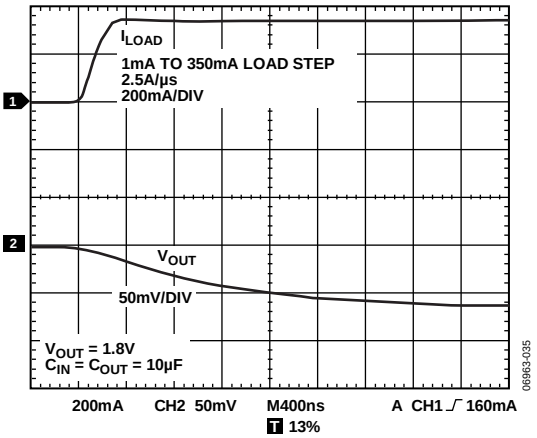

Figure 35. Output Transient Response, C_{OUT} = 10 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered. If >1 µF of output capacitance is required, the input capacitor should be increased to match it.

Bias Capacitor

Connecting a 1 µF capacitor from VBIAS to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered.

Input, Bias, and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADP130, as long as it meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended for use with any LDO, due to their poor temperature and dc bias characteristics.

Figure 36 shows the capacitance vs. voltage bias characteristics of the 0402 1µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40 to +85°C temperature range and is not a function of the package or voltage rating.

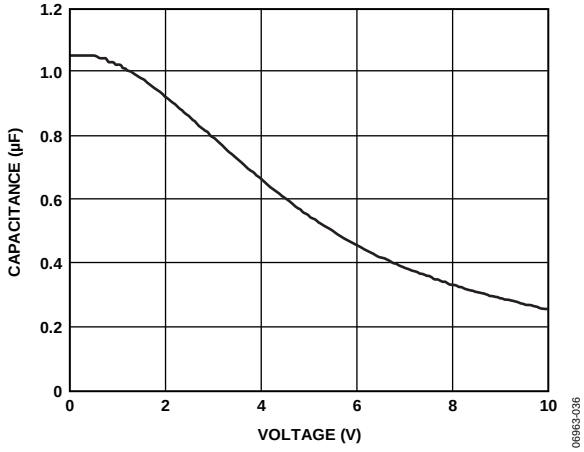

Figure 36. Capacitance vs. Voltage Characteristics

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, TEMPCO over −40°C to +85°C is assumed to be 15% for an X5R dielectric. TOL is assumed to be 10%, and C_{OUT} = 0.94 µF at 1.8 V, as shown in Figure 36.

Substituting these values in Equation 1 yields the following:

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP130, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP130 has an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 2.1 V. This ensures that the ADP130 inputs and the output behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP130 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 37, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

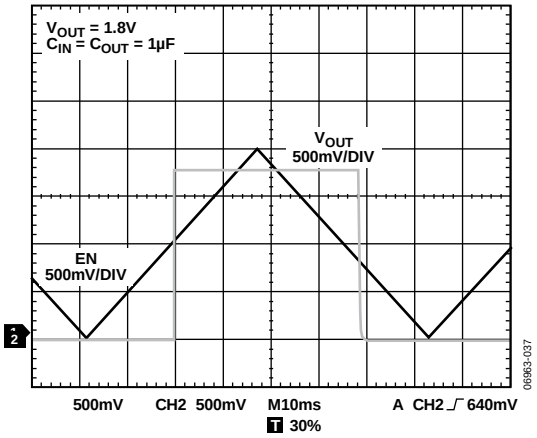

Figure 37. Typical EN Pin Operation

As shown in Figure 37, the EN pin has built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active and inactive thresholds are derived from the V_{IN} voltage. Therefore, these thresholds vary with changing input voltage. Figure 38 shows typical EN active and inactive thresholds when the V_{BIAS} voltage varies from 2.3 V to 5.5 V.

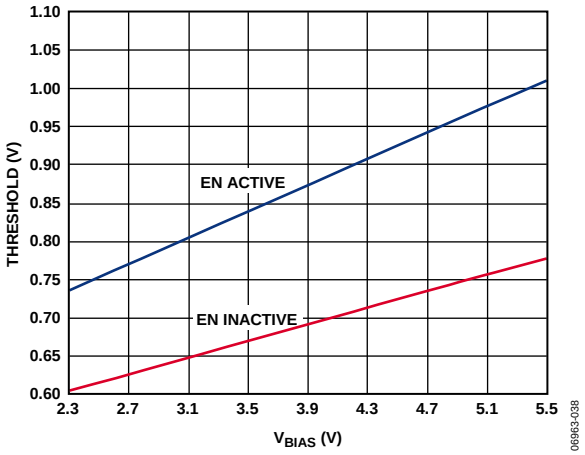

Figure 38. Typical EN Pin Thresholds vs. Input

The ADP130 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 0.8 V option is approximately 180 µs from the time at which the EN active threshold is crossed to when the output reaches 90% of its final value. The start-up time depends somewhat on the output voltage setting and increases slightly as the output voltage increases.

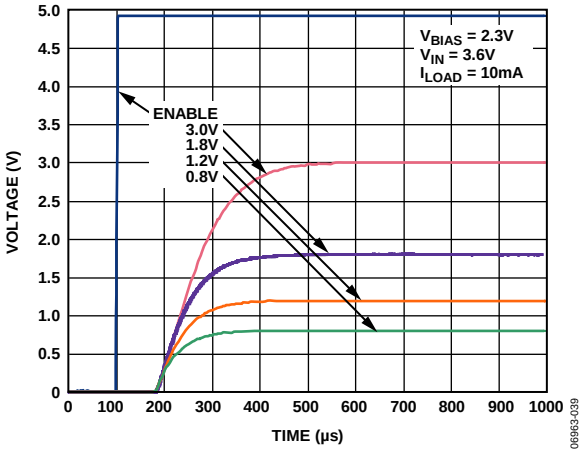

Figure 39. Typical Start-Up Time for Various Output Voltages

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP130 is protected against damage due to excessive power dissipation by current limit and thermal overload protection circuits. The ADP130 is designed to current limit when the output load reaches 550 mA (typical). When the output load exceeds 550 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection limits the junction temperature to a maximum of 150°C typical. Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing output current to zero. When the junction temperature drops below 135°C, the output is turned on again and output current is restored to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP130 current limits so that only 550 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 550 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 550 mA and 0 mA that continues as long as the short remains at the output.

Current limit and thermal overload protections protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP130 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The value of θ_{JA} is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered on the PCB. Table 6 shows typical θ_{JA} values of the 5-lead TSOT package for various PCB copper sizes.

Table 6. Typical θ_{JA} Values for Specified PCB Copper Sizes

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	170
50	152
100	146
300	134
500	131

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP130 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation can be simplified as follows:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 40 through Figure 46 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

JUNCTION TEMPERATURE CALCULATIONS

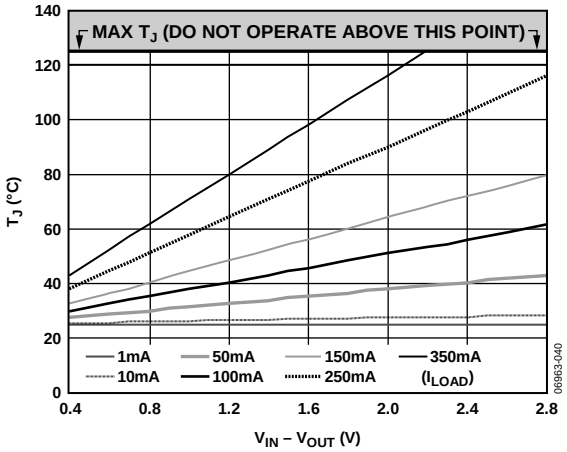

Figure 40. 500 mm² of PCB Copper, T_A = 25°C, TSOT

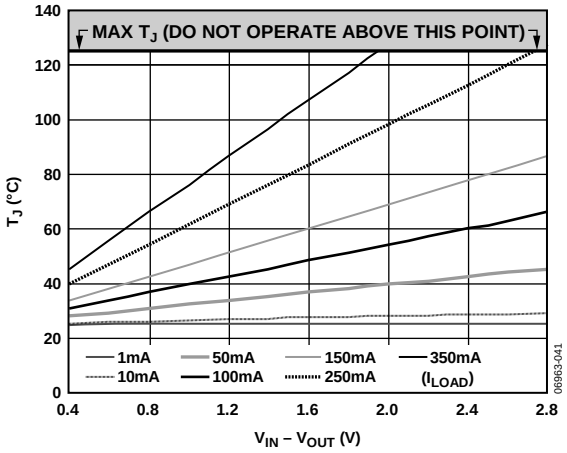

Figure 41. 100 mm² of PCB Copper, T_A = 25°C, TSOT

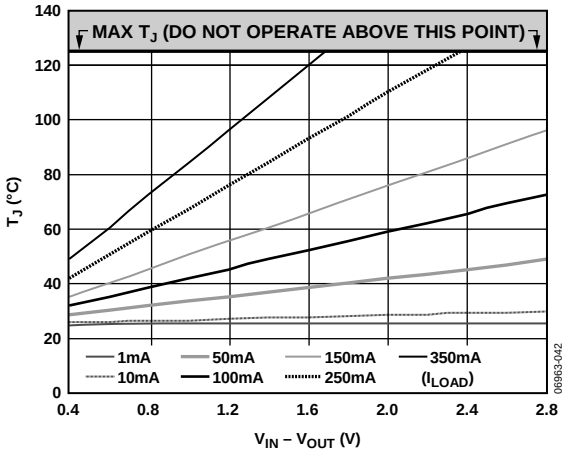

Figure 42. 0 mm² of PCB Copper, T_A = 25°C, TSOT

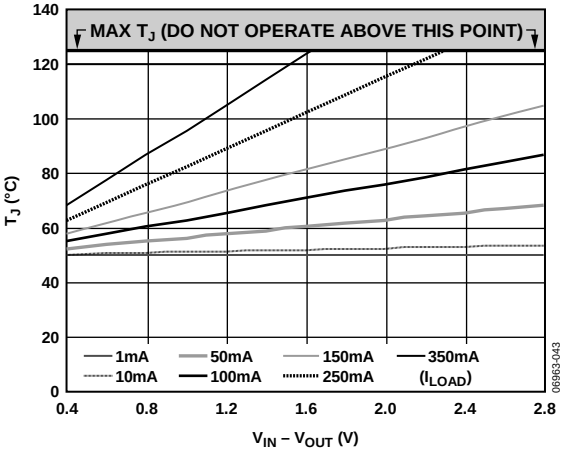

Figure 43. 500 mm² of PCB Copper, T_A = 50°C, TSOT

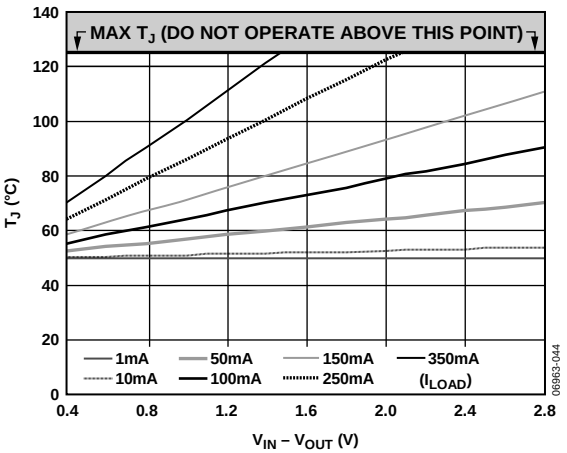

Figure 44. 100 mm² of PCB Copper, T_A = 50°C, TSOT

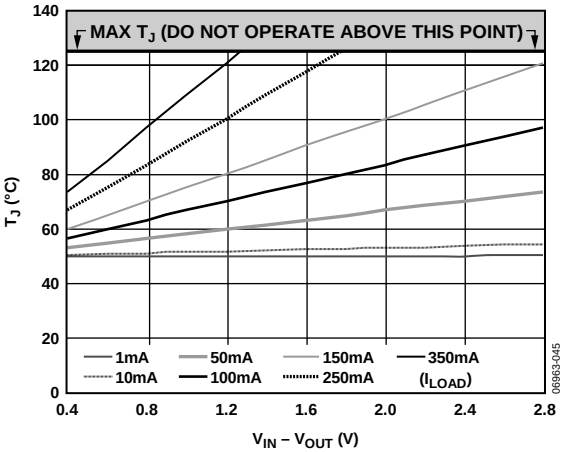

Figure 45. 0 mm² of PCB Copper, T_A = 50°C, TSOT

In cases where board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D), using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 42.8°C/W for the 5-lead TSOT package.

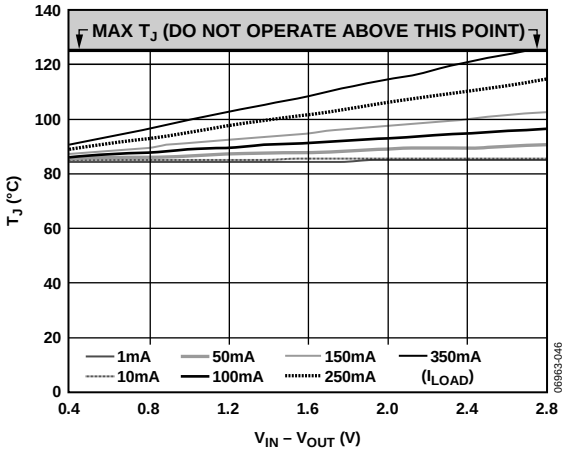

Figure 46. TSOT, T_A = 85°C

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP130. However, as shown in Table 6, a point of diminishing return is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

The input capacitor should be placed as close as possible to the VIN and GND pins. The output capacitor should be placed as close as possible to the VOUT and GND pins. Using 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where the area is limited.

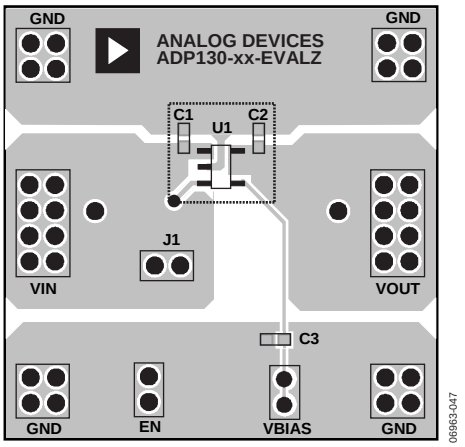

Figure 47. Example TSOT PCB Layout

OUTLINE DIMENSIONS

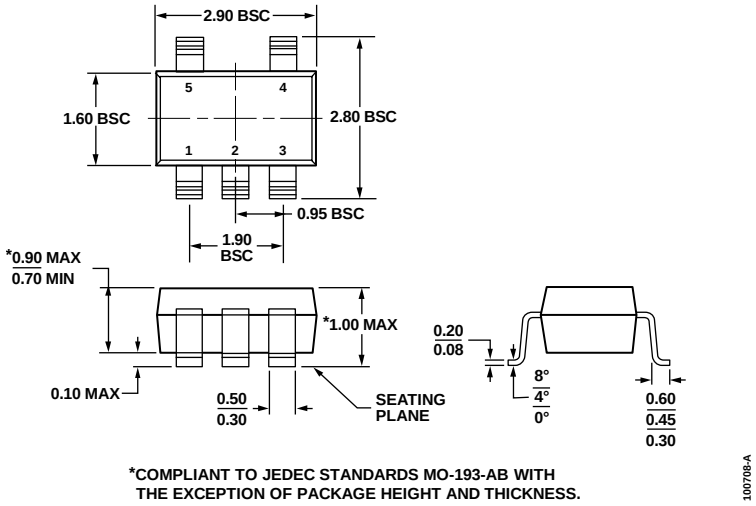

Figure 48. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP130AUJZ-0.8-R7	−40°C to +125°C	0.8	5-Lead TSOT	UJ-5	LCH
ADP130AUJZ-1.2-R7	−40°C to +125°C	1.2	5-Lead TSOT	UJ-5	LCJ
ADP130AUJZ-1.5-R7	−40°C to +125°C	1.5	5-Lead TSOT	UJ-5	LCK
ADP130AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LCL
ADP130AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LCM
ADP130-0.8-EVALZ	−40°C to +125°C	0.8	Evaluation Board		
ADP130-1.2-EVALZ	−40°C to +125°C	1.2	Evaluation Board		
ADP130-1.5-EVALZ	−40°C to +125°C	1.5	Evaluation Board		
ADP130-1.8-EVALZ	−40°C to +125°C	1.8	Evaluation Board		
ADP130-2.5-EVALZ	−40°C to +125°C	2.5	Evaluation Board		
ADP130UJZ-REDYKIT			Evaluation Board Kit		
ADP130-BL1-EVZ			Blank Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact your local Analog Devices, Inc., sales or distribution representative.

NOTES

NOTES

D06963-0-5/10(B)