

### FEATURES

- Single-supply operation: 4.5 V to 18 V
- Upper/lower buffers swing to  $V_S$ /GND
- Gamma continuous output current: >10 mA
- $V_{COM}$  peak output current: 250 mA
- Offset voltage: 12 mV
- Slew rate: 8 V/ $\mu$ s
- Unity gain stable with large capacitive loads
- Supply current: 700  $\mu$ A per amplifier
- Compact 28-lead TSSOP
- Pb-free package
- Drop-in replacement for BUF11702

### APPLICATIONS

- TFT LCD monitor panels
- TFT LCD notebook panels

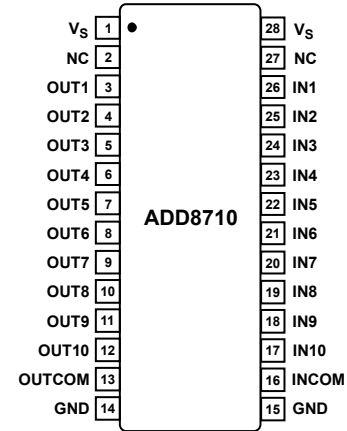
### GENERAL DESCRIPTION

The ADD8710 is a low cost, 10-channel gamma buffer with a  $V_{COM}$  driver that operates from a single supply. The part is designed for high resolution TFT LCD panels and is built on an advanced, high voltage CBCMOS process.

The gamma buffers have a high slew rate, minimum 10 mA output current, and a high capacitive load drive capability. The  $V_{COM}$  buffer is capable of delivering 250 mA of peak current and can also drive large capacitive loads. The ADD8710 offers a wide supply range and offset voltages below 12 mV.

The ADD8710 is specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range and is available in a Pb-free, 28-lead TSSOP package.

### PIN CONFIGURATION



NC = NO CONNECT

Figure 1. 28-Lead TSSOP (RU Suffix)

### FUNCTIONAL BLOCK DIAGRAM

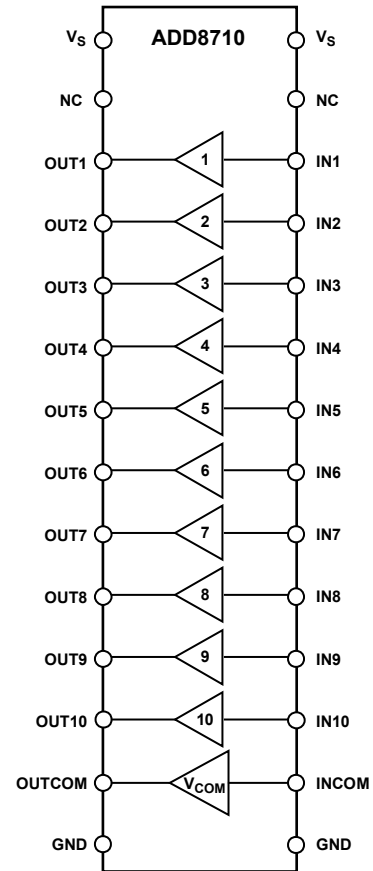


Figure 2.

### Rev. B

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## REVISION HISTORY

### 6/07—Rev. A to Rev. B

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### 3/05—Rev. 0 to Rev. A

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### 6/04—Revision 0: Initial Version

## SPECIFICATIONS

$V_S = 16\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A @ 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	Applies to all channels		4	12	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		5		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.5	1.1	$\mu\text{A}$
Input Impedance	$Z_{IN}$			400	1.5	$\mu\text{A}$
Input Capacitance	$C_{IN}$			1		pF
<b>BUFFER CHARACTERISTICS</b>						
Common-Mode Input Range	$V_{CMM}$		1.25		$V_S$	V
Buffer 1 to Buffer 5			0		$V_S - 1.25$	V
Buffer 6 to Buffer 10						V
Output Voltage High (V1)	$V_{OH}$	$V_S = 16\text{ V}, V_{IN} = 16\text{ V}, I_L = 10\text{ mA}$ $V_S = 10\text{ V}, V_{IN} = 9.8\text{ V}, I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	15.82	15.9		V
Output Voltage High (V2 to V5)	$V_{OH}$	$V_S = 10\text{ V}, V_{IN} = 8.5\text{ V}, I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	9.75	9.8		V
Output Voltage High (V6 to V10)	$V_{OH}$	$V_S = 10\text{ V}, V_{IN} = 8\text{ V}, I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	9.7			V
Output Voltage Low (V1 to V5)	$V_{OL}$	$V_S = 10\text{ V}, V_{IN} = 2\text{ V}, I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	8.45	8.5		V
Output Voltage Low (V6 to V9)	$V_{OL}$	$V_S = 10\text{ V}, V_{IN} = 1.5\text{ V}, I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	8.4			V
Output Voltage Low (V10)	$V_{OL}$	$V_S = 16\text{ V}, V_{IN} = 0\text{ V}, I_L = 10\text{ mA}$ $V_S = 10\text{ V}, V_{IN} = 0.2\text{ V}, I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	7.95	8		V
Continuous Output Current	$I_{OUT}$			2	2.05	V
Peak Output Current	$I_{PK}$	$V_S = 16\text{ V}$			2.10	V
<b><math>V_{COM}</math> CHARACTERISTICS</b>						
Common-Mode Input Range	$V_{CMM}$		0		$V_S - 1.25$	V
Output Voltage High	$V_{OH}$	$V_S = 10\text{ V}, V_{IN} = 8\text{ V}, I_L = 30\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	7.95	8		V
Output Voltage Low	$V_{OL}$	$V_S = 10\text{ V}, V_{IN} = 2\text{ V}, I_L = 30\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	7.9			V
Continuous Output Current	$I_{OUT}$			2	2.05	V
Peak Output Current	$I_{PK}$	$V_S = 16\text{ V}$			2.10	V
<b>SUPPLY CHARACTERISTICS</b>						
Supply Voltage	$V_S$		4.5		18	V
Power Supply Rejection Ratio	PSRR	$V_S = 4.5\text{ V to } 16.5\text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	70	90		dB
Total Supply Current	$I_{SY}$	$V_O = V_S/2$ , no load $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		7.7	10	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega, C_L = 200\text{ pF}$	4	8		$\text{V}/\mu\text{s}$
Bandwidth	BW	$-3\text{ dB}, R_L = 10\text{ k}\Omega, C_L = 200\text{ pF}$		5		MHz
Settling Time to 0.1% (Buffers)	$t_s$	1 V step, $R_L = 10\text{ k}\Omega, C_L = 200\text{ pF}$		1.1		$\mu\text{s}$
Settling Time to 0.1% ( $V_{COM}$ )	$t_s$	1 V step, $R_L = 10\text{ k}\Omega, C_L = 200\text{ pF}$		0.7		$\mu\text{s}$
Phase Margin	$\Phi_O$	$R_L = 10\text{ k}\Omega, C_L = 200\text{ pF}$		45		Degrees
Channel Separation				75		dB

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V <sub>s</sub> )	18.5 V
Input Voltage	-0.5 V to V <sub>s</sub> + 0.5 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature	300°C
ESD Tolerance (HBM)	±2500 V
ESD Tolerance (MM)	±200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	Unit
28-Lead TSSOP (RU)	67.7	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

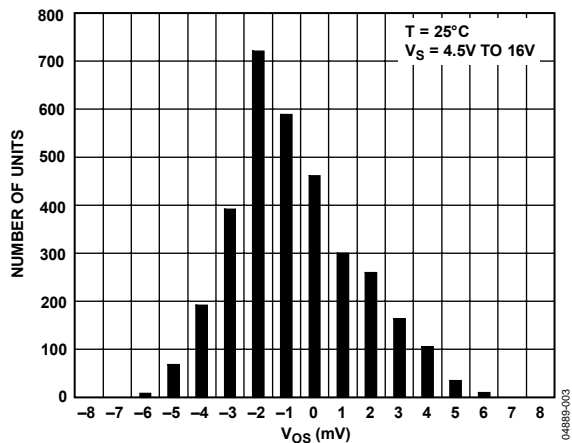


Figure 3. Input Offset Voltage Distribution

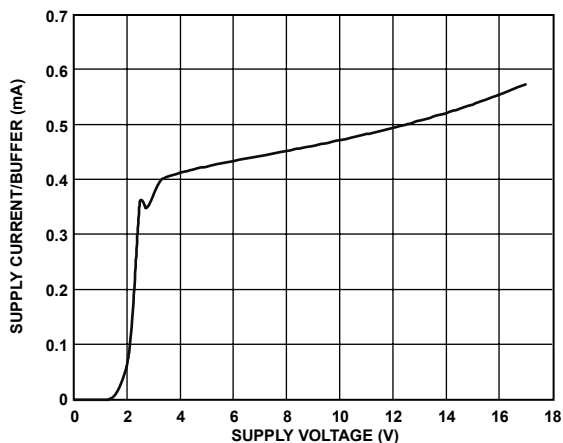


Figure 6. Supply Current/Buffer vs. Supply Voltage

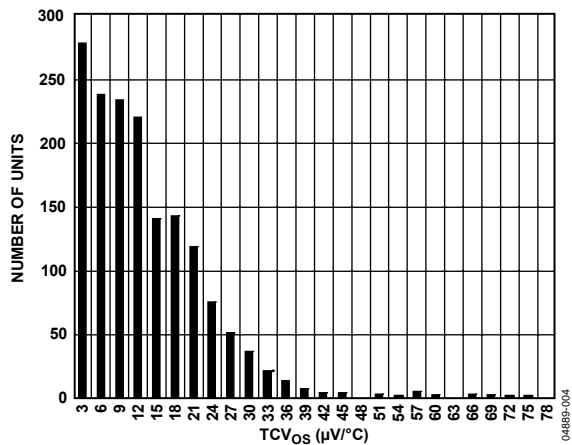


Figure 4. Input Offset Voltage Drift Distribution

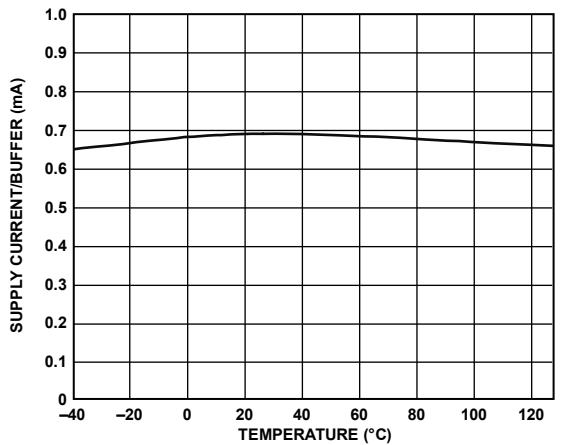


Figure 7. Supply Current/Buffer vs. Temperature

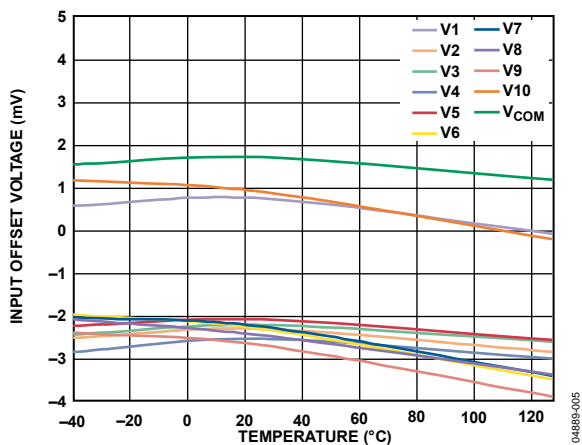


Figure 5. Input Offset Voltage vs. Temperature

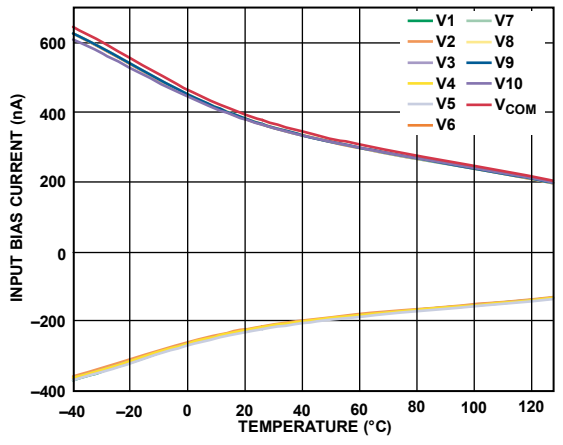


Figure 8. Input Bias Current vs. Temperature

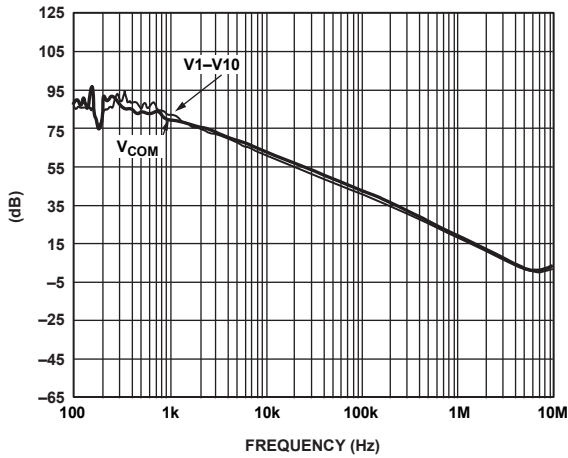


Figure 9. Power Supply Rejection Ratio vs. Frequency

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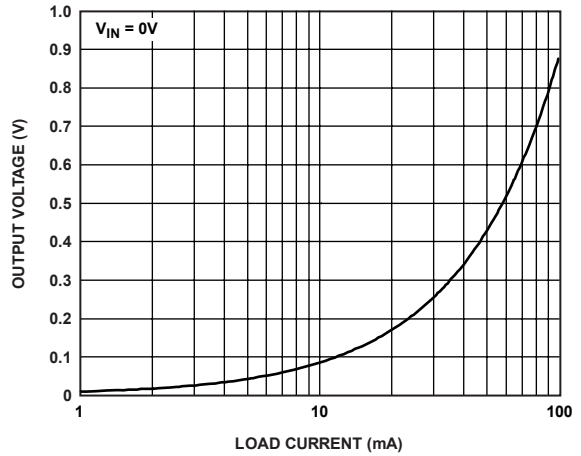


Figure 12. Channel  $V_{COM}$  Output Voltage Low vs. Load Current

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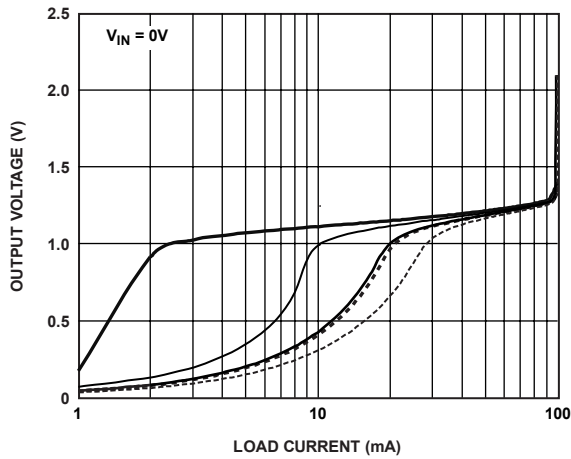


Figure 10. Channel 1 to Channel 5 Output Voltage Low vs. Load Current

04889-010

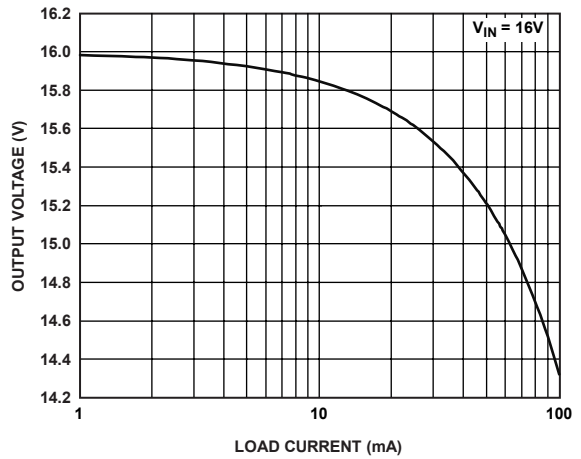


Figure 13. Channel 1 Output Voltage High vs. Load Current

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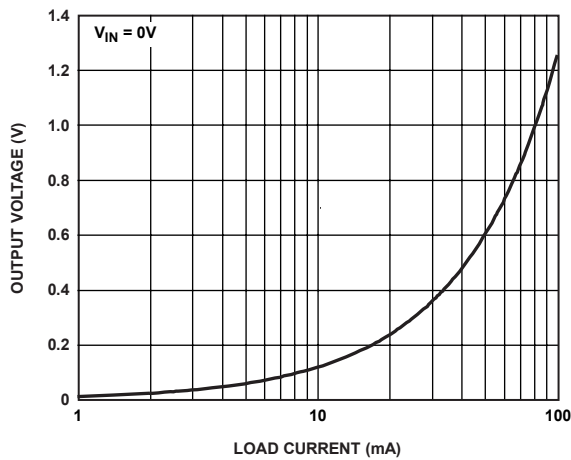


Figure 11. Channel 6 to Channel 10 Output Voltage Low vs. Load Current

04889-011

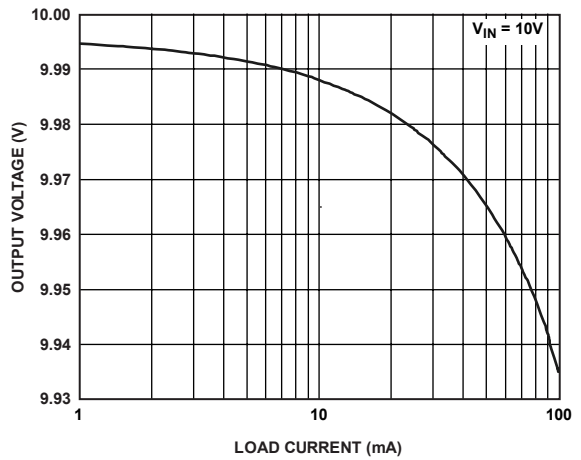


Figure 14. Channel 2 to Channel 5 Output Voltage High vs. Load Current

04889-014

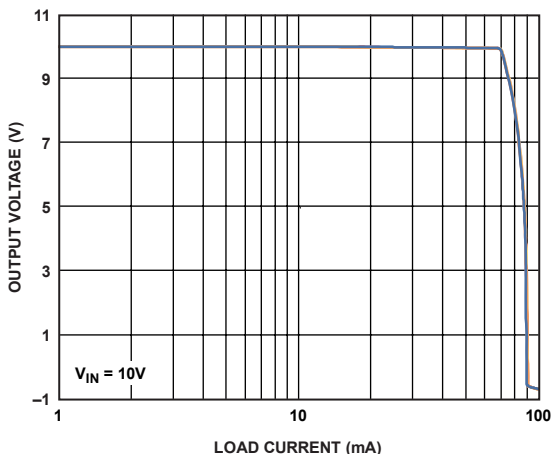


Figure 15. Channel 6 to Channel 10 Output Voltage High vs. Load Current

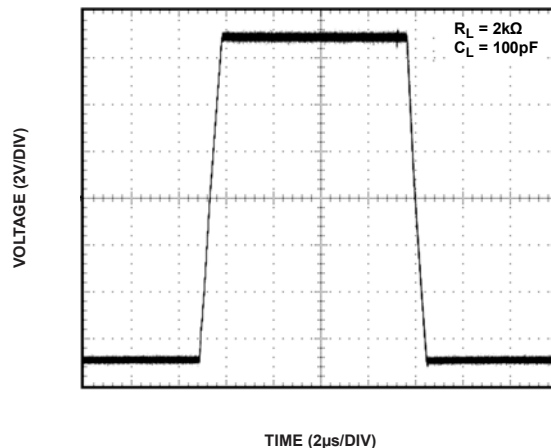


Figure 18. Large Signal Transient Response

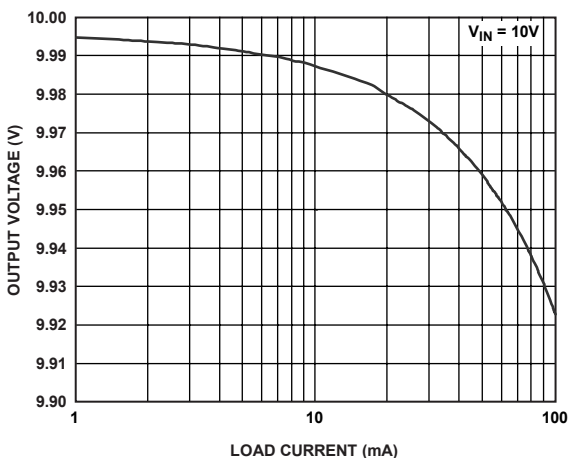


Figure 16. Channel  $V_{COM}$  Output Voltage High vs. Load Current

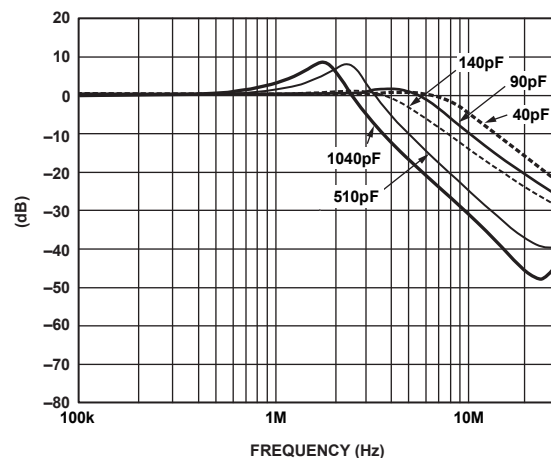


Figure 19. Channel 1 to Channel 5 Frequency Response vs. Capacitive Loading

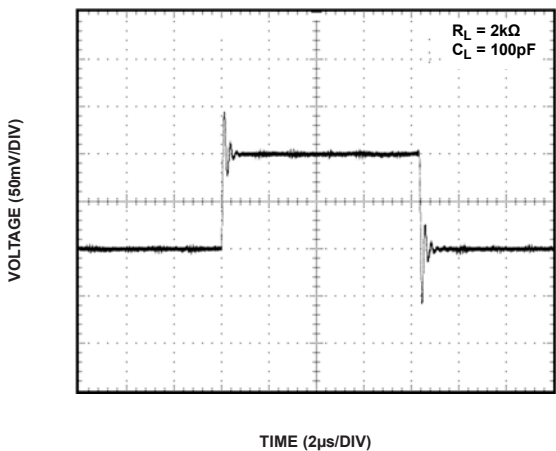


Figure 17. Small Signal Transient Response

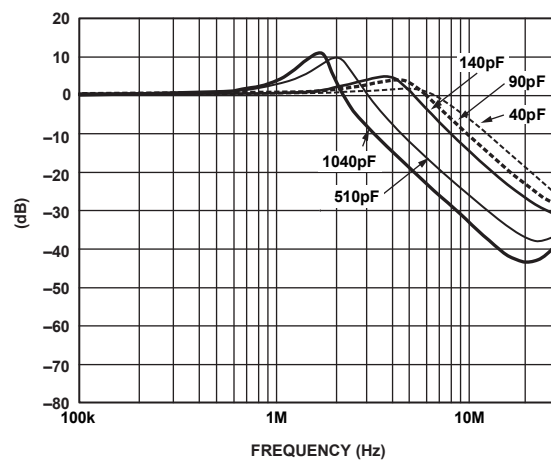


Figure 20. Channel 6 to Channel 10 Frequency Response vs. Capacitive Loading

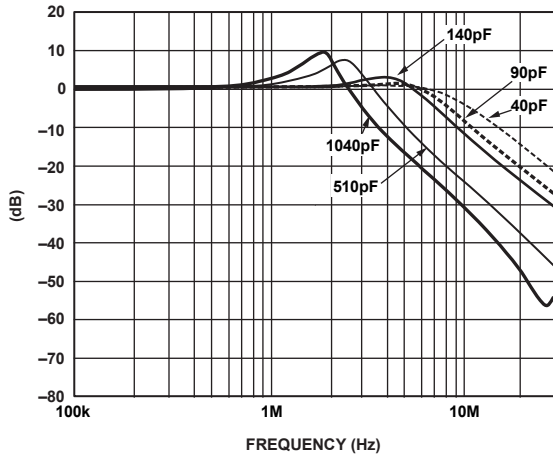


Figure 21. Channel  $V_{COM}$  Frequency Response vs. Capacitive Loading

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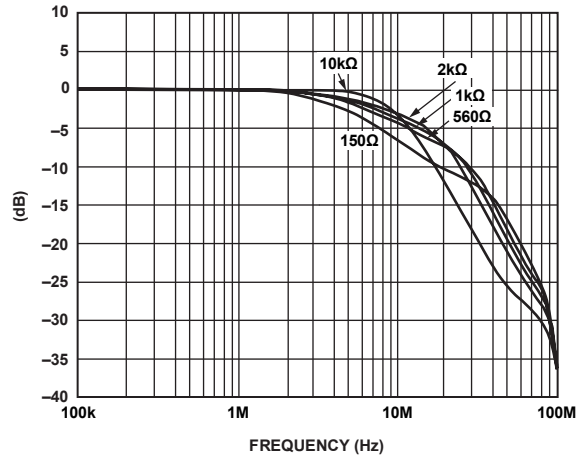


Figure 24. Channel  $V_{COM}$  Frequency Response vs. Resistive Loading

04889-024

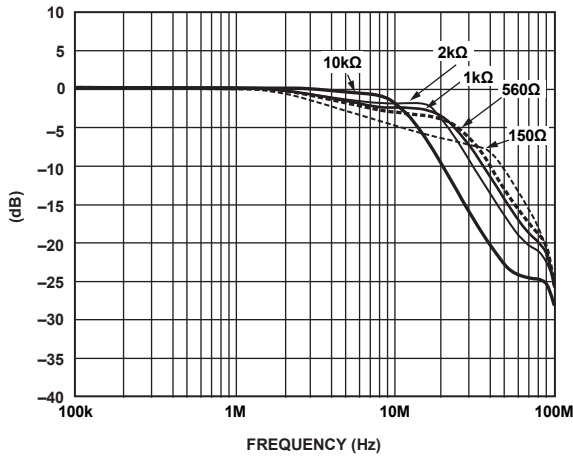


Figure 22. Channel 1 to Channel 5 Frequency Response vs. Resistive Loading

04889-022

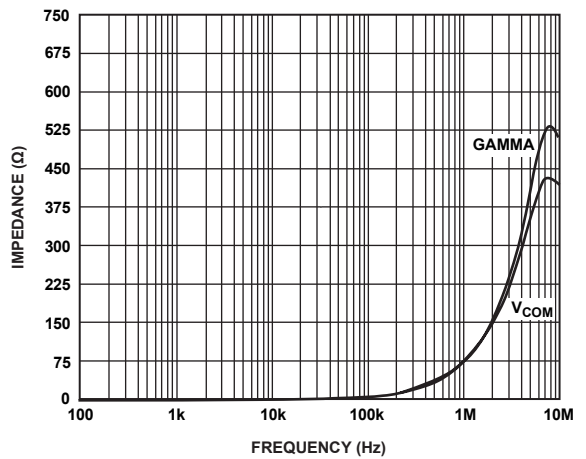


Figure 25. Closed-Loop Output Impedance vs. Frequency

04889-025

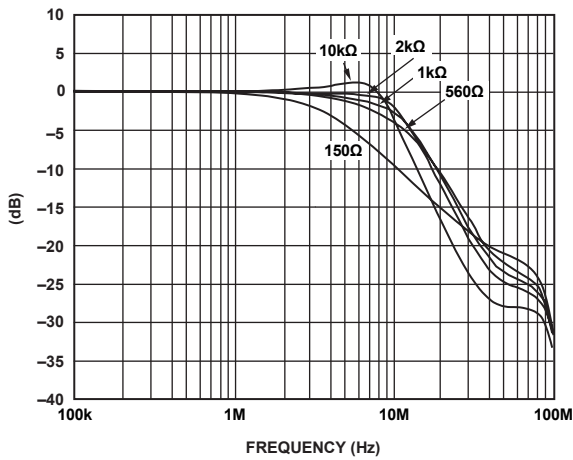


Figure 23. Channel 6 to Channel 10 Frequency Response vs. Resistive Loading

04889-023

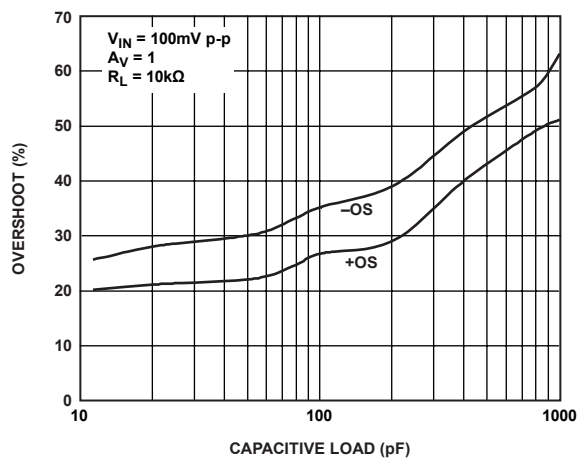
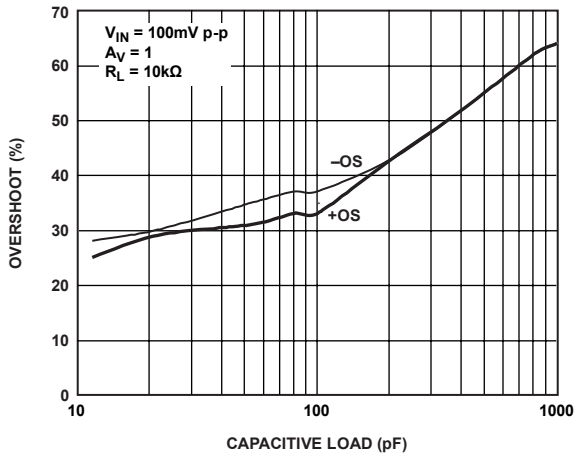


Figure 26. Channel 1 to Channel 5 Small Signal Overshoot vs. Load Capacitance

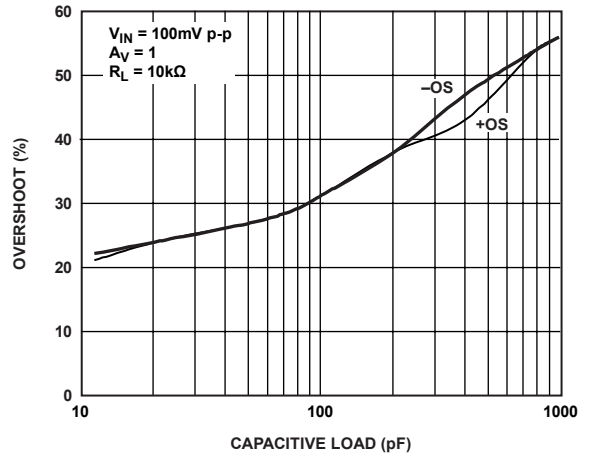
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Figure 27. Channel 6 to Channel 10 Small Signal Overshoot vs. Load Capacitance

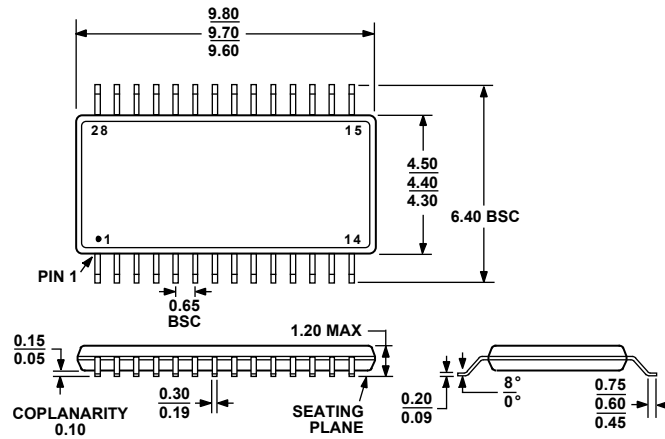


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Figure 28. Channel  $V_{COM}$  Small Signal Overshoot vs. Load Capacitance

# ADD8710

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 29. 28-Lead Thin Shrink Small Outline Package [TSSOP] (RU-28)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADD8710ARUZ <sup>1</sup>	-40°C to +85°C	28-Lead TSSOP	RU-28
ADD8710ARUZ-REEL <sup>1</sup>	-40°C to +85°C	28-Lead TSSOP	RU-28

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**ADD8710**

**NOTES**